

LIN System Basis ICs

Features

- o LIN 2.x / SAE J2602 compliant
- o Operating voltage V_{SUP} = 5 ... 27 V
- o 3 modes: Normal, Silent and Sleep
- Linear low drop voltage regulator:

MLX80030/31:

- Normal mode 3.3V/70mA ±2%
- Silent mode 3.3V/20mA ±2%

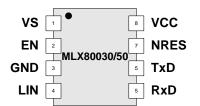
MLX80050/51:

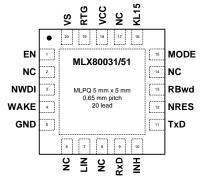
- Normal mode 5V/70mA ±2%
- Silent mode 5V/20mA ±2%
- Low current consumption (typ)
 - Sleep mode 20 μA
 - Silent mode "noload" 45 μA
- Output current limitation
- LIN-Bus Transceiver
 - Baud rate up to 20 kBaud
 - Slew rate control for best EME behaviour
 - Low slew mode for optimized SAE J2602 transmission
 - High impedance LIN pin in case of loss of ground or battery
 - Bus input voltages -24V to 30V independent from VBat
- Remote and local wake up source recognition
- VCC undervoltage detection at NRES output (start-up delay 4ms)
 - Vres threshold 3.0 V (MLX80030/31); Vres threshold 4.1V (MLX80050/51)
- o Programmable Window Watchdog (only MLX80031/51)
- o VSUP undervoltage detection (POR), Over temperature shutdown
- o TxD dominant time out function, Standby mode time out after 350ms
- Automotive temperature range of –40°C to 125°C
- Interface I/O's independent from voltage regulator output
- Enhanced ESD robustness according to IEC 61000-4-2
 - Direct discharge for pin LIN >20kV (only Lin cap connected) and for pin VBAT >15kV
 - o Indirect discharge for pin LIN >15kV
- Load dump protected (40V)

Order Code	Temp. Range	Package	Delivery	Remark
MLX80050 KDC-BAA-000-RE	-40 - 125 °C	SOIC8	Reel	Wettable Flanks Wettable Flanks
MLX80051 KLW-BAA-000-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	
MLX80030 KDC-BAA-000-RE	-40 - 125 °C	SOIC8	Reel	
MLX80031 KLW-BAA-000-RE	-40 - 125 °C	QFN_WF20/5x5	Reel	

Short Description

The MLX8005x/3x consist of a low-drop voltage regulator 5V/3.3V/70mA combined with a Reset/Watchdog unit and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 2.x and SAE J2602. The watchdog times of the integrated window watchdog can be adapted on application needs via external resistors. With the help of an external bipolar transistor it is possible to extend the output current of the integrated voltage regulator. The combination of voltage regulator and bus transceiver as well as watchdog unit makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.







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LIN System Basis ICs

1. Electrical Specification

All voltages are referenced to ground (GND), positive currents flow into the IC.

Absolute Maximum Ratings

Table 1: Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VS	Vs	Respective to GND	-0.3	40	V
Transient voltage ISO 7637/2		pulse 1, 2	-100	100	V
Transient voltage ISO 7637/2		pulse 3A; 3B, coupling 1nF	-150	100	V
DC voltage LIN	VLIN_DC	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage WAKE	Vwake_dc	Respective to GND and VS Loss of Ground (VGND = VS)	-20 -30	40 40	V
DC voltage INH	VINH_DC		-0.3	Vs+0.3	V
DC voltage VCC	Vvcc_dc		-0.3	7	V
DC voltage RTG	V_{RTG_DC}		-0.3	7	V
Input voltage at low voltage I/O's (EN, TxD, RxD, NRES, WDI, RBwD)	V _{IN}		-0.3	7	V
	Vesdiec	IEC 61000-4-2, direct ESD Pin LIN with LIN cap 220pF Pin VS to GND	20 15		kV
	V _{ESDIECind}	IEC 61000-4-2, indirect ESD Pin LIN with LIN cap 220pF	15		kV
ESD voltage	Vesdhbm	HBM (CDF-AEC-Q100-002) Pin LIN Pin WAKE, KL15, VS Other pins	±6 ±4 ±2	50 100 20 40 30 40 30 40 30 Vs+0.3 3 7 3 7 3 7 5 5 6 4 2 00 crnal limited see so chapter 9.1 150 50 10 150	kV kV kV
	VESDCDM	pulse 1, 2 -100 1 pulse 3A; 3B, coupling 1nF -150 1 Respective to GND and VS Loss of Ground (VGND = VS) -30 4 Respective to GND and VS Loss of Ground (VGND = VS) -20 4 -0.3 -30 4 -0.3 -0.3 Vs- -0.3 -0.3 -0.3 IEC 61000-4-2, direct ESD Pin LIN with LIN cap 220pF Pin VS to GND 20 15 IEC 61000-4-2, indirect ESD Pin LIN with LIN cap 220pF 15 15 HBM (CDF-AEC-Q100-002) Pin LIN Pin WAKE, KL15, VS Other pins ±6 ±4 CDM (AEC-Q100-011) ±500 Internal limited also chapter 9 JEDEC 1s0p board, no air flow 1 5 JEDEC 1s0p board, no air flow -40 1		V	
Power dissipation	P ₀				
Thermal resistance from junction to ambient	RTHJA_SOIC8			150	K/W
	RTHJA_QFN20			50	K/W
Junction temperature	TJ		-40	150	°C
Storage temperature	T _{STG}		-55	150	°C

LIN System Basis ICs

1.1. DC Characteristics

Unless otherwise specified all values in the following tables are valid for $V_S = 5$ to 27V and $T_{AMB} = -40$ to $125^{\circ}C$. All voltages are referenced to ground (GND), positive currents flow into the IC. For MLX80031/51 apply: RTG connected to VCC.

Table 2: Voltage Regulator and Reset Unit

	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T [1]
Suppl	y Voltage Pin VS							
	Nominal DC operating voltage	Vs		5		27	V	Α
1.01	Vs under voltage reset	V _{SUVR_OFF}	V _S ramp up	2.9		4.6	V	Α
1.02	Vs under voltage reset	V _{SUVR_ON}	V _S ramp down	2.4		4.2	V	Α
1.03	Vs under voltage reset hysteresis	Vsuvr_hys	V _{SUVR_OFF} - V _{SUVR_ON}	0.04	0.3	0.7	V	Α
Supp	ly currents MLX80030, MLX80	050				•		•
2.00	Supply current, normal mode	Ivs_nor	V _S ≤ 14V, V _{EN} > 2V , LIN recessive, no load at VCC	400	750	1500	μА	А
2.01	Supply current, sleep mode	I _{VS_sleep}	$V_S \le 14V$ $T_A = 25 ^{\circ}\text{C}$ $-40 ^{\circ}\text{C} \le T_A \le 125 ^{\circ}\text{C}$		20	20 30	μА	Α
2.02	Supply current, silent mode	Ivs_sil	$V_S \le$ 14V, LIN recessive no load at VCC $T_A = 25~^{\circ}\text{C}$ $-40~^{\circ}\text{C} \le T_A \le 125~^{\circ}\text{C}$	20	45	65 85	μА	Α
Supp	ly currents MLX80031, MLX80	051				•	1	
2.00	Supply current, normal mode [2]	Ivs_nor	$V_S \le 14V$, $V_{EN} > 2V$, $RB_{WD} = 60k$ LIN recessive, no load at VCC	400	750	1500	μА	А
2.01	Supply current, sleep mode	IVS_sleep	$V_S \le 14V$ $T_A = 25 ^{\circ}\text{C}$ $-40 ^{\circ}\text{C} \le T_A \le 125 ^{\circ}\text{C}$		20	20 30	μА	Α
2.02	Supply current, silent mode	Ivs_sil	$V_S \le$ 14V, LIN recessive no load at VCC $T_A = 25 ^{\circ}\text{C}$ $-40 ^{\circ}\text{C} \le T_A \le 125 ^{\circ}\text{C}$	20	45	65 85	μА	А



	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T [1]
Voltag	e Regulator Pin VCC	•					•	
MLX8	80050, MLX80051 (RTG connec	ted to VC	C)					
3.01	Output voltage VCC	Vccn5	$\begin{aligned} 6V &\leq V_S \leq 18V \\ 1mA &\leq I_{LOAD} \leq 70mA \\ T_A &= 25^{\circ}C \\ T_A &= -40^{\circ}C \text{ to } 125^{\circ}C \end{aligned}$	4.90 4.85	5.0	5.10 5.15	V	A
	Output voltage VCC under disturbances to fulfil functional state A	V _{CCndis5}	$6V \leq V_S \leq 18V, T_A = 25^{\circ}C$ $R_{LOAD} = 330 \Omega$	4.75		5.25	V	С
3.02		V _{D10_5}	V _S > 4V , I _{VCC} = 10mA		75	120	mV	Α
3.03	Drop-out voltage [3]	V _{D30_5}	V _S > 4V , I _{VCC} = 30mA		220	350	mV	Α
3.04		V _{D70_5}	$V_S > 4V$, $I_{VCC} = 70$ mA		500	800	mV	Α
3.05	Line regulation	V_{LNR5}	6V ≤ V _S ≤ 18V			20	mV	С
3.06		V _{LDR10_5}	1 mA < I _{LOAD} < 10 mA			50	mV	Α
3.07	Load regulation	V _{LDR30_5}	1 mA < I _{LOAD} < 30 mA			90	mV	Α
3.08		V _{LDR70_5}	1 mA < I _{LOAD} < 70 mA			150	mV	Α
3.09	Output current limitation	I _{VCCLIM_5}	$V_S > 6V$ $T_A = -40 \ ^{\circ}C$ $25 \ ^{\circ}C \le T_A \le 125 \ ^{\circ}C$	-135 -150	-110	-75 -80	mA	А
3.10	Load capacity	CLOAD		2.2	22		μF	D
MLX8	0030, MLX80031 (RTG connec	ted to VCC	;)				•	
3.01	Output voltage VCC	V _{CCn3}	$\begin{array}{c} 4~V \leq V_S \leq 18~V \\ 1m~A \leq I_{LOAD} \leq 70~mA \\ T_A = 25~^{\circ}C \\ T_A = -40~^{\circ}C~to~125~^{\circ}C \end{array}$	3.234 3.201	3.3	3.366 3.399	V	А
	Output voltage VCC under disturbances to fulfil functional state A	VCCndis3	$6~V \le ~V_S \le 18~V, ~T_A = 25~^{\circ}C$ $R_{LOAD} = 330~\Omega$	3.135		3.465	V	С
3.02	Drop-out voltage [3]	V _{D10_3}	V _S > 3 V , I _{VCC} = 10 mA			100	mV	Α
3.03		V _{D30_3}	$V_{\text{S}} > 3 \text{ V}$, I_{VCC} = 30 mA			300	mV	Α
3.04		V _{D70_3}	$V_S > 3 \text{ V}$, I_{VCC} = 70 mA			700	mV	Α
3.05	Line regulation	V_{LNR_3}	5 V ≤ V _S ≤ 18 V			20	mV	Α
3.06	Load regulation	V _{LDR10_3}	1 mA < I _{LOAD} < 10 mA			50	mV	Α
3.07		V _{LDR30_3}	1 mA < I _{LOAD} < 30 mA			90	mV	Α
3.08		V _{LDR70_3}	1 mA < I _{LOAD} < 70 mA			150	mV	Α
3.09	Output current limitation	Ivcclim_3	$V_S > 4 V$ $T_A = -40 \ ^{\circ}C$ $25 \ ^{\circ}C \le T_A \le 125 \ ^{\circ}C$	-135 -150	-110	-75 -80	mA	Α
3.10	Load capacity	CLOAD		2.2	22		μF	D



	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T [1]
Output	Pin NRES			-		<u> </u>		
4.01	Output voltage low	V _{OL_NRES}	I _{NRES} = 2 mA			0.4	V	Α
4.02	Leakage current low	I _{leak_RxD}	V _{NRES} = 0 V	-5		5	μΑ	Α
4.03	Leakage current high	I _{leak_RxD}	V _{NRES} = V _{CC}	-5		5	μΑ	Α
	Output voltage high NRES under disturbances to fulfil functional state A [4]	V _{OH_NRES}	R _{load} = 2.7 k to VCC	V _{CC} -1			V	С
MLX8	80050, MLX80051							
5.01	VCC reset threshold on NRES pin	V _{RES5V}	t > t _{rr}	3.9	4.10	4.3	V	Α
5.02	V _{RES} Hysteresis V _{RESHYS} = V _{RES(ON)} - V _{RES(OFF)}	V _{RESHYS5V}				200	mV	С
MLX8	80030, MLX80031							
5.01	VCC reset threshold on NRES pin	V _{RES3V}	t > t _{rr}	2.75	2.95	3.15	V	Α
5.02	V _{RES} Hysteresis V _{RESHYS} = V _{RES(ON)} - V _{RES(OFF)}	V _{RESHYS3V}				100	mV	С
Input F	Pin EN						L	
6.01	Input voltage low	VIL_EN				0.8	V	Α
6.02	Input voltage high	V _{IH_EN}		2.0			V	Α
6.03	Hysteresis	V _{HYS_EN}		50	100	700	mV	С
6.04	Pull-down resistor	R _{pd_EN}	V _{EN} =VCC	50	125	250	kΩ	Α
Input F	Pin WAKE (MLX80031, MLX80	051)		<u> </u>		-		
7.01	High level input voltage	V _{IH_WAKE}	Sleep mode	V _S -1V			V	Α
7.02	Low level input voltage	VIL_WAKE	Sleep mode			Vs-3.3V	V	Α
7.03	Pull up current WAKE	I _{WAKE_PU}	Normal & sleep	-30	-15	-1	μΑ	Α
7.04	Leakage current WAKE high	IWAKE_Ik	V _S = 18V	-5		5	μΑ	Α
Input	Pin KL15 (MLX80031, MLX800	51)						
8.01	High level input voltage	V _{IH_KL15}	Rv = 50kΩ	4		V _S +0.3V	V	Α
8.02	Low level input voltage	VIL_KL15	$Rv = 50k\Omega$	-1		2	V	Α
8.03	Pull down current KL15	I _{KL15_PD}			30	65	μΑ	Α
Input	Pin MODE (MLX80031, MLX80	051)				1		
23.01	Input voltage low	VIL_MODE				0.8	V	Α
23.02	Input voltage high	V _{IH} _MODE		2.0			V	Α
23.03	Hysteresis	V _{HYS_MODE}		50	100	700	mV	С
23.04	Pull-down resistor	R _{pd_MODE}	V _{MODE} =VCC	200		250	kΩ	Α



	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T [1]
Input P	in NWDI (MLX80031, MLX800	51)		-				
9.01	Input voltage low	V _{IL_NWDI}				0.8	V	Α
9.02	Input voltage high	V _{IH_NWDI}		2.0			V	Α
9.03	Hysteresis	V _{HYS_NWDI}		50	100	600	mV	С
9.04	Pull-up resistor to VCC	R _{pu_NWDI}	VN _{WDI} = 0V	125	250	375	kΩ	Α
Watch	dog Oscillator pin RB _{WD} (MLX8	30031, MLX	K80051)					
10.01	Voltage at RB _{WD}	V_{RBwd}	Ιουτ = -50 μΑ		1.2		V	Α
10.02	Range of RB _{WD} resistance	RB _{WD}		20		150	kΩ	В
10.03	RBwb short resistance to disable Watchdog	RBwdsh	Watchdog disabled	0		330	Ω	В
Output	INH (MLX80031, MLX80051)							
11.01	ON Resistance	R _{ON_INH}	V _S = 12V		20	50	Ω	Α
11.02	Leakage current INH high	leakH_INH	Sleep Mode, V _{INH} = 18V, V _S = 18V	-5		5	μA	Α
11.03	Leakage current INH low	I _{leakL_INH}	Sleep Mode, V _{INH} = 0V, V _S = 18V	-5		5	μA	Α
Therma	al Protection							
	Thermal shutdown	TJSHD		155	170	190	°C	D
	Thermal hysteresis	T _{JHYS}			10	30	°C	D

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Table 3: LIN DC Characteristics

Param	eter	Symbol	Condition	Min	Тур	Max	Unit	T [1]
Gener	al							
12.01	Pull up current LIN (recessive)	I _{INLINpu}	V _{LIN} = 18 V, V _S = 6V			80	μА	Α
12.02	Pull up resistor LIN	R _{LINpu}	V _S = 12V, V _{LIN} = 0V	20	30	60	kΩ	Α
12.03	Reverse current LIN (dominant)	I _{INLINdom}	V _S = 12V, V _{LIN} = 0V	-400			μΑ	Α
12.04	Reverse current LIN (recessive)	I _{INLINrec}	$ \begin{array}{l} V_{LIN \geq} V_S, 8V \leq V_{LIN} \\ \leq 18V, \\ 8V \leq V_S \leq 18V \end{array} $	0		23	μΑ	А
12.05	Reverse current LIN (loss of battery)	I _{INLIN_lob}	V_S = 0V, 0V \leq V _{LIN} \leq 18V	0		23	μΑ	Α
12.06	Reverse current LIN (loss of ground)	I _{INLIN_log}	V_S = 12V, 0V \leq V _{LIN} \leq 18V	-10		50	μΑ	Α
	Voltage drop serial Diode	V _{SerDiode}		0.4	0.7	1.0	V	D
	Battery Shift	V _{Shift_BAT}		0		11.5	%	D
	Ground Shift	V _{Shift_GND}		0		11.5	%	D
	Ground-Battery shift difference	V_{Shift_diff}		0		8	%	D
Receiv	ver		•					
12.07	Receiver dominant voltage	V _{BUSdom}				0.4*V _S		Α
12.07	Receiver recessive voltage	V _{BUSrec}		0.6*Vs				Α
12.08	Centre point of receiver threshold V _{thr_cnt} = (V _{thr_rec} +V _{thr_dom})/2	V _{thr_cnt}	$7.0 \text{ V} \le \text{V}_{\text{S}} \le 18 \text{ V}$	0.475*Vs	0.5*Vs	0.525*Vs	V	Α
12.09	Receiver Hysteresis Vhys = Vthr_rec-Vthr_dom	V_{hys}			0.15*V _S	0.175*V _S		Α
Transı	mitter		-		-			
			$R_{load} = 500\Omega$, $V_S = 5V$	0		1.2	V	D
12.10	Transmitter dominant voltage	Vol _{bus}	R_{load} = 500 Ω , V_S >= 7 V	0		0.2*Vs		Α
12.11	Current limitation LIN	I _{LIM}	$V_{LIN} = V_S$, $TxD = 0V$	40	120	200	mA	Α
12.12	Transmitter recessive voltage	Voh _{BUS}	No load, $V_{EN} = 0/5V$, $VTxD = 5V$	0,8*Vs		Vs	V	А



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Param	eter	Symbol	Condition	Min	Тур	Max	Unit	T [1]	
Input/	Input/Output Pin TxD								
13.01	Input voltage low TxD	$V_{\text{IL_TxD}}$	rising			0.8	V	Α	
13.02	Input voltage high TxD	V_{IH_TxD}		2			V	Α	
13.03	Hysteresis	$V_{\text{HYS_TxD}}$		50		700	mV	С	
13.04	Pull-up resistor to VCC	R_{pu_TxD}	$V_{TxD} = 0V$	125	250	375	kΩ	Α	
13.06	Low level output current	I _{OL_TxD}	local wake-up request; standby mode; $V_{TxD} = 0.4V$	1.5			mA	А	
Outpu	t Pin RxD						•	-	
14.01	Output voltage low RxD	V_{OL_RxD}	I _{RxD} = 2 mA			0.6	V	Α	
14.02	Pull-up resistor to VCC	R_{pu_RxD}	V _{RxD} = 0V	3	5	7	kΩ	Α	
14.03	Leakage current high	I _{leak_RxD}	V _{RxD} = VCC	-5		5	μA	Α	
	Output voltage high RxD under disturbances to fulfil functional state A [4]	V_{OH_RxD}	R _{load} = 2.7k to VCC	V _{CC} -1			V	С	

Notes:

- A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk),
 D = Value guaranteed by design
- [2] No watchdog reset; Watchdog trigger time on WDI = t.b.d.ms; Measurement of the average current of 10 watchdog periods.
- [3] The nominal V_{CC} voltage is measured at V_{SUP} =12V. If the V_{CC} voltage is 100mV below its nominal value then the voltage drop is $V_D = V_{SUP} V_{CC}$
- [4] Functionality range of current limitation at silent mode is limited by reset threshold V_{RES}. Below them the IC change to normal mode.

Validity for I_{VCC_MAXsil} : VCCn (min) \leq VCC \leq V_{RES}

1.2. AC Characteristics

 $6V \le V_S \le 27V$, $-40^{\circ}C \le T_A \le 125^{\circ}C$, RTG connected to VCC, unless otherwise specified

Table 4: AC Characteristics

	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T ^[1]		
Reset p	Reset parameter on NRES									
16.01	Reset time	t _{Res}	V _S = 14V	2.5	4	5.5	ms	Α		
16.02	Reset rising time	t _{rr}	V _S = 14V	3.0	6.5	12	μS	Α		
Watchd	log parameter on NRES (MLX80031	, MLX80051)				_	<u>-</u>			
17.01		twposc20	RB _{WD} = $20k\Omega \pm 1\%$	6.87	8.09	9.30	μ\$	Α		
17.02	Watchdog-Oscillator Period (on TM9)	twoosc60	$RB_{WD} = 51k\Omega \pm 1\%$	16.06	18.90	21.73	μ\$	Α		
17.03		twposc100	RB_{WD} = 100k Ω ±1%	30.58	35.98	41.37	μ\$	Α		



	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T ^[1]	
17.04	i didilictei	twposc150	$RB_{WD} = 150k\Omega \pm 1\%$	45.40	53.41	61.42	μs	Α	
17.04	Watchdog Close Window	tcw	twoosc	40.40	1053	01.42	cy- cles	D	
	Watchdog Open Window	tow	twoosc		1105		cy- cles	D	
17.05	Watchdog Reset Low Time	twDres		3	4	5	ms	Α	
	Watchdog Lead Window	t ldt	twposc two		7895		cy- cles	D	
17.06	Watchdog Safety Oscillator	twDsafety	RB _{WD} gnd	30	50	75	μs	Α	
Wake-u	p and Mode Control	•				-		-	
18.01	Remote Wake-up filter time	t _{wu_remote}		30	70	150	μS	Α	
18.02	Wake-up filter time on WAKE (only MLX80051,MLX80031)	t _{wu_WAKE}	Sleep or Silent Mode, WAKE falling edge	10		50	μs	А	
18.03	Wake-up filter time on KL15 (only MLX80051,MLX80031)	twu_KL15	Sleep or Silent Mode, KL15 rising edge	80	168	250	μѕ	А	
18.04	Propagation delay from Normal Mode to Sleep Mode via EN	t _{pd_sleep}	V _{EN} = 0V	5	15	20	μs	Α	
18.05	Propagation delay from Standby Mode to Normal Mode via EN	t _{pd_norm}	V _{EN} = 5V	5	15	20	μS	Α	
18.06	Propagation delay from Silent Mode to Normal Mode via EN	tpd_sil_n	V _{EN} = 5V	5	15	40	μ\$	А	
18.07	Propagation delay: go to silent mode after EN=H/L ^[3]	t _{pd_sil}	check falling edge on RBwd EN = 0V			20	μs	A	
	Setup time TxD to EN for low slew mode	t _{set_TxD_EN}		5			μS	В	
	Hold time TxD after EN for low slew mode	thold_TxD_EN		20			μS	В	
18.08	Debouncing time EN	t _{deb_EN}		2	5	20	μS	А	
18.09	TxD dominant time out	t _{TxD_to}	Normal Mode, V _{TxD} = 0V	27		60	ms	А	
18.10	Standby time out	t _{sby_to}	Standby Mode, V _{EN} = 0V	150		500	ms	А	
Genera	General LIN Parameter								
19.01	Receiver propagation delay LIN -> RxD	t _{dr_RxD}	C _{L(RXD)} = 50 pF			6	μs	А	
19.02	Symmetry prop. delay LIN->RxD	t _{dsym_RxD}	tdr_RXD - tdf_RXD	-2		2	μs	Α	
19.03	Receiver debouncing time	t _{deb_LIN}		1.5	2.8	4.0	μS	D	



	Parameter	Symbol	Condition	Min	Тур	Max	Unit	T ^[1]
19.04	slew rate rising edge LIN	dV/dTrise	Normal Mode	1.0	1.5	2.5	V/μs	С
19.05	slew rate falling edge LIN	dV/dTfall	LIN-Load: 1k0 / 1nF	-2.5	-1.5	-1.0	V/μs	С
19.06	slew rate rising edge LIN	dV/dTrise	Low Slew Mode	0.3	0.8	1.3	V/μs	С
19.07	slew rate falling edge LIN	dV/dTfall	dV/dTfall LIN-Load: 1k // 1nF		-0.8	-0.3	V/μs	С
	Internal capacity	CLIN	Pulse at LIN via 10kOhm with 0/10 V; VS = open		25	35	pF	D
LIN tra	nsceiver parameter according to L	N Physical L	ayer Spec. rev. 2.0, tak	ole 3.4 (20k	bit/s)			
Condit	ions: Normal slew mode; Vs TxD signal: t _{Bit} = 50µs			=; 660Ω/6.	8nF; 500Ω	2/10nF		
	Minimal recessive bit time [2]	t _{rec(min)}		40	50	58	μS	
	Maximum recessive bit time [2]	t _{rec(max)}		40	50	58	μS	
20.01	Duty cycle 1	D ₁	$D_1 = t_{rec(min)} / (2*t_{Bit})$	0.396				Α
20.02	Duty cycle 2	D ₂	$D_2 = t_{rec(max)} / (2*t_{Bit})$			0.581		Α
T		! a a l l	0	A /40 41-L-	41-1			
	eiver parameter according to LIN Figure ions: Low slew mode: $V_S = 7$				•)nF		
Transc Condit		.0V to 18V;	 LIN loads: 1kΩ/1nF; 6		•)nF		
	ions: Low slew mode; V _S =7	.0V to 18V;	 LIN loads: 1kΩ/1nF; 6		•)nF 113	μs	
	ions: Low slew mode; V _S =7 TxD signal: t _{Bit} = 96µs	.0V to 18V; , t _{wH} = T _{wL} =	 LIN loads: 1kΩ/1nF; 6	660Ω/6.8nl	=; 500Ω/10	T	μs μs	
	ions: Low slew mode; V _S =7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time [2]	0.0V to 18V; $t_{wH} = T_{wL} = t_{rec(min)}$	 LIN loads: 1kΩ/1nF; 6	60Ω/6.8nl	÷; 500Ω/10	113	<u> </u>	A
Condit	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time [2] Maximum recessive bit time [2]	.0V to 18V; $t_{WH} = T_{WL} = t_{rec(min)}$ $t_{rec(max)}$	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$	80 80	÷; 500Ω/10	113	<u> </u>	A
21.01 21.02	ions: Low slew mode; $V_S = 7$ TxD signal: $t_{Bit} = 96\mu s$ Minimal recessive bit time [2] Maximum recessive bit time [2] Duty cycle 1	$.0V \text{ to } 18V;$ $t_{wH} = T_{wL} =$ $t_{rec(min)}$ $t_{rec(max)}$ D_3 D_4	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$	80 80	÷; 500Ω/10	113 113	<u> </u>	
21.01 21.02	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time ^[2] Maximum recessive bit time ^[2] Duty cycle 1 Duty cycle 2 ansceiver parameter according	.0V to 18V; t _{wH} = T _{wL} = t _{rec(min)} t _{rec(max)} D ₃ D ₄ co SAE J260 .0V to 18V;	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590	<u> </u>	
21.01 21.02 LIN tra	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time ^[2] Maximum recessive bit time ^[2] Duty cycle 1 Duty cycle 2 Cansceiver parameter according sions: Low slew mode; V _S = 7	.0V to 18V; t _{wH} = T _{wL} = t _{rec(min)} t _{rec(max)} D ₃ D ₄ co SAE J260 .0V to 18V;	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590	<u> </u>	
21.01 21.02 LIN tra	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time ^[2] Maximum recessive bit time ^[2] Duty cycle 1 Duty cycle 2 ansceiver parameter according to the signal: t _{Bit} = 96µs Minimal recessive delay	.0V to 18V; $t_{WH} = T_{WL} =$ $t_{rec(min)}$ $t_{rec(max)}$ D3 D4 $co SAE J260$.0V to 18V; $t_{WH} = T_{WL} =$	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590	μs	A
21.01 21.02 LIN tra Condit	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time ^[2] Maximum recessive bit time ^[2] Duty cycle 1 Duty cycle 2 ansceiver parameter according tions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive delay TxD -> LIN ^[2] Maximum recessive delay	$.0V \text{ to } 18V;$ $t_{WH} = T_{WL} =$ $t_{rec(min)}$ $t_{rec(max)}$ D_3 D_4 $co \textbf{SAE J260}$ $.0V \text{ to } 18V;$ $t_{WH} = T_{WL} =$ $t_{x_rec_min}$	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590	μѕ	A
21.01 21.02 LIN tra Condit 22.01 22.02	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time ^[2] Maximum recessive bit time ^[2] Duty cycle 1 Duty cycle 2 ansceiver parameter according tions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive delay TxD -> LIN ^[2] Maximum recessive delay TxD -> LIN ^[2] Minimal dominant delay	$.0V \text{ to } 18V;$ $t_{WH} = T_{WL} =$ $t_{rec(min)}$ $t_{rec(max)}$ D_3 D_4 $co \text{ SAE J260}$ $.0V \text{ to } 18V;$ $t_{WH} = T_{WL} =$ $t_{x_rec_min}$ $t_{x_rec_max}$	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590 nF 48	μs μs μs	A
21.01 21.02 LIN tra Condit 22.01 22.02	ions: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive bit time [2] Maximum recessive bit time [2] Duty cycle 1 Duty cycle 2 Ansceiver parameter according signs: Low slew mode; V _S = 7 TxD signal: t _{Bit} = 96µs Minimal recessive delay TxD -> LIN [2] Maximum recessive delay TxD -> LIN [2] Minimal dominant delay TxD -> LIN [2] Maximum dominant delay Maximum dominant delay	.0V to 18V; t _{WH} = T _{WL} = trec(min) t _{rec(max)} D ₃ D ₄ co SAE J260 .0V to 18V; t _{WH} = T _{WL} = t _{x_rec_min} t _{x_rec_max}	LIN loads: $1k\Omega/1nF$; 6 t_{Bit} ; $t_{rise} = t_{fall} < 100ns$ $D_3 = t_{rec(min)} / (2*t_{Bit})$ $D_4 = t_{rec(max)} / (2*t_{Bit})$ 22 (10.4kbit/s) LIN loads: $1k\Omega/1nF$;60	80 80 0.417	96 96	113 113 0.590 nF 48 48	μs μs μs	A A A

A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk),
 D = Value guaranteed by design

LIN System Basis ICs

1.3. Timing diagrams

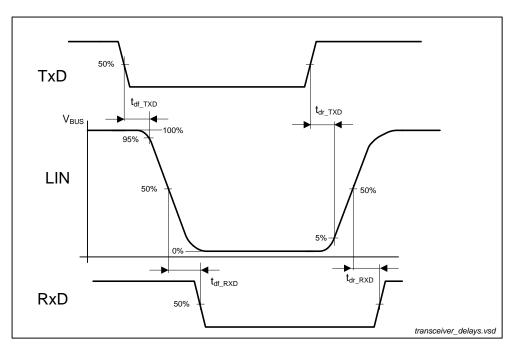


Figure 1: LIN propagation delays

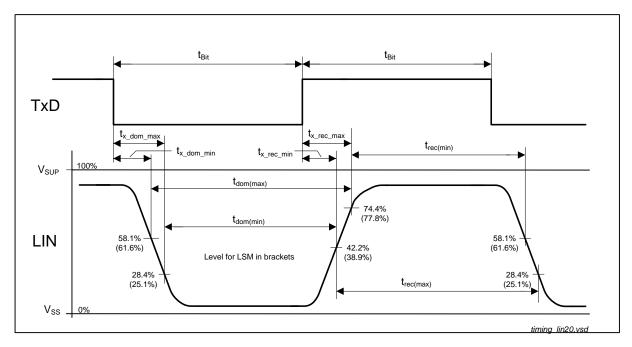


Figure 2: LIN duty cycles



LIN System Basis ICs

2. Pin Configuration

2.1. MLX80030 and MLX80050 - SOIC8

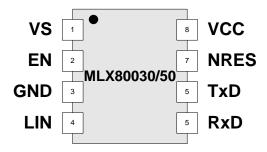


Table 5: MLX80050/30 pin list in SOIC8

Pin	Name	Ю-Тур	Description
1	VS	Р	Battery supply voltage
2	EN	I	Mode control pin, enables the normal operation mode when HIGH
3	GND	G	Ground
4	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
5	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
6	TxD	I/O	Transmit data input (low = dominant)
7	NRES	0	Undervoltage reset output (open drain), low active
8	VCC	Р	Voltage regulator output

LIN System Basis ICs

2.2. MLX80031 and MLX80051 in QFN20

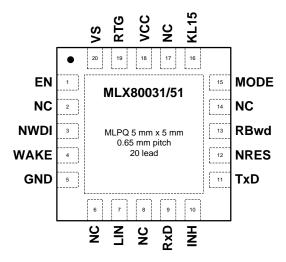


Table 6: MLX80051/31 pin list in QFN20

Pin	Name	Ю-Тур	Description
1	EN	I	Mode control pin, enables the normal operation mode when HIGH
2	NC		not connected
3	NWDI	I	Watchdog trigger input; negative edge; pull-up
4	WAKE	I	High voltage input for local wake up, negative edge triggered
5	GND	G	Ground
6	NC		not connected
7	LIN	I/O	LIN bus transmitter/receiver pin, (low = dominant)
8	NC		not connected
9	RxD	I/O	Received data from LIN bus, low in dominant state; internal pull-up resistor
10	INH	0	High side switch; High voltage
11	TxD	I/O	Transmit data input (low = dominant)
12	NRES	0	Reset output (open drain), low active
13	RB _{WD}	I/O	Bias resistor for watchdog oscillator
14	NC		not connected
15	MODE	I	Input to control window watchdog; internal pull-down resistor
16	KL15	I	High voltage input for local wake up, positive edge triggered
17	NC		not connected
18	VCC	I	Voltage regulator sense input
19	RTG	Р	Voltage regulator output
20	VS	Р	Battery supply voltage

LIN System Basis ICs

3. Functional Description

The MLX8003x/5x consists of a low drop 3.3V/5V voltage regulator capable to drive 70mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller. Additionally integrated is a Window-Watchdog/RESET unit with a fixed power-on-reset delay of 4 ms and an adjustable watchdog time defined by an external bias resistor.

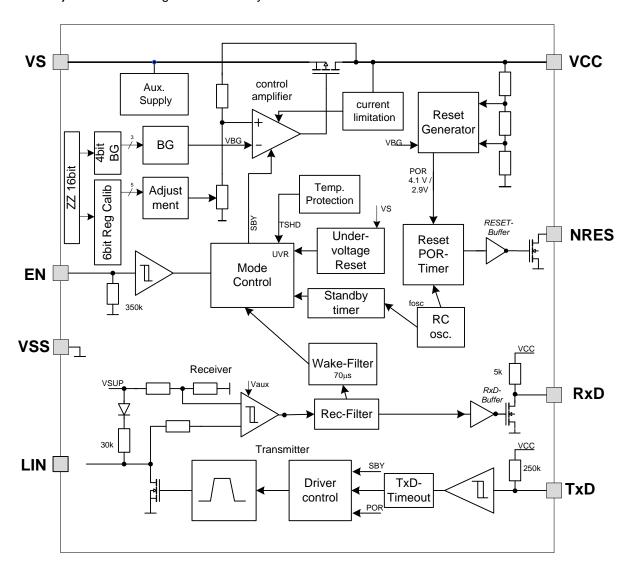


Figure 3: MLX80050/30 Block Diagram

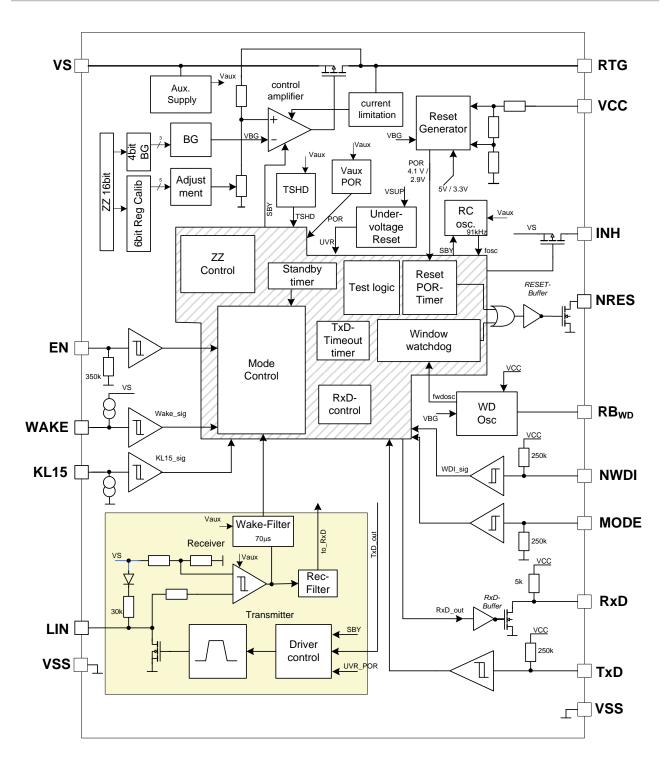


Figure 4: MLX80051/31 Block Diagram



LIN System Basis ICs

3.1. Supply Pin VS

VS is the operational voltage pin of MLX8005x/3x. The voltage range is VS = 6 to 18V. After switching on VS, the MLX8003x/5x starts at Standby Mode and the VCC voltage regulator ramps up. An undervoltage detection unit prevent an undefined operation for Vs < 4V.

VS- Power-ON

If VS is switched on, the MLX8003x/5x starts in Standby Mode. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the MLX8003x/5x on. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operate independent from each other, which secures the independence from the rise time of VS.

3.2. EN input pin

The ENable input is the mode control pin of MLX8003x/5x in combination with the TxD input.

The MLX8003x/5x is switched into the Sleep Mode with a falling edge and into normal mode with a rising edge at the EN pin. The state machine goes to Normal Mode after t_{Res} (see also Table 4: AC Characteristics). The Normal Mode will be kept as long as EN remains high.

The Normal Mode can be entered from Standby Mode, when the pin EN is driven HIGH. To prevent unwanted mode transitions, the EN input contains a debounce filter as specified ($t_{EN \ deb}$).

The pin EN contains a weak pull down resistor. The input thresholds are compatible to 3.3V and 5V supply systems.

MLX80031/51:

Additionally the positive edge on pin EN results in an immediate reset of the active low interrupt on pin RxD as well as the wake-up source recognition flag on pin TxD.

3.3. Ground pin GND

This is the reference pin of the IC. The absence of GND connection will not influence or disturb the communication between other LIN bus nodes.

3.4. *LIN*

This bidirectional pin consists of a low side driver in the output path and a high-voltage comparator in the input path. Furthermore is integrated a LIN pull-up resistor between LIN and VS pin. Low side driver consist a current limitation.

3.5. Receiver Output RxD

The pin RxD is a buffered open drain output. Output signals can be shifted by the external pull up resistor to 3.3V and 5V supply systems.

3.6. Transmit Input TxD

The transmit data stream of the LIN protocol controller applied to the pin TxD is converted into the LIN bus signal with slew rate control in order to minimize electromagnetic emissions.

The pin TxD contains a weak pull up resistor. The input thresholds are compatible to 3.3V and 5V supply systems. To enable the transmit path, the TxD pin has to be driven recessive (HIGH) after or during the normal mode has been entered.

3.6.1. TxD dominant time-out feature

With the first dominant level on pin TxD after the transmit path has been enabled, the dominant time-out counter is started. In case of a faulty blocked permanent dominant level on pin TxD the transmit path will be disabled after the specified time t_{TxD_to} . The time-out counter is reset by the first negative edge on pin TxD.



LIN System Basis ICs

3.7. Output NRES

The NRES pin outputs the reset state as well as the watchdog condition in MLX80031 and MLX80051.

3.8. Voltage regulator pins VCC and RTG

The MLX80030/50 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±2% (MLX80050/51) or 3.3V ±2% (MLX80030/31) with a load current of max. 70mA. The current limitation unit limits the output current for short circuits or overload to 130mA by decreasing the VCC voltage. This way the power dissipation is held constant at a maximum value.

The voltage regulator has two pins, output pin RTG and sense input pin VCC. For MLX80030/50 both, RTG and VCC, are commonly bonded to pin VCC on the package.

Devices MLX80031/51 has both pins bonded and provides the possibility to use an external npn transistor to boost the maximum load current. In this case the basis of the npn transistor has to be connected to the RTG pin and the emitter to the VCC pin. In case of using the internal voltage regulator, both pins have to be connected to each other.

3.9. INH Output (only MLX80031/51)

INH switches to high (VS connected to INH) in case of Standby or Normal Mode. INH is switched off at Silent and Sleep Mode. The pin will be used for switch on an external power supply or for switch off the external 1k master resistor in master node applications.

3.10. WAKE Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a falling edge on WAKE the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.

The pin WAKE provides a weak pull up current source towards Vs which provides a HIGH level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin WAKE directly to pin Vs in order to prevent influences due to EMI.

3.11. KL15 Input (only MLX80031/51)

High voltage input pin for local wake-up functionality. With a rising edge on KL15 the IC wakes-up from Silent Mode or Sleep Mode to Standby Mode.

The pin KL15 provides a weak current sink towards GND which provides a LOW level on the pin in case of open circuit failures or if no local wake-up feature is required. In such applications it is recommended to connect the pin KL15 directly to GND in order to prevent influences due to EMI. KL15 is typically connected to the ignition terminal and generates a local wake-up at start of ignition.

3.12. Watchdog Trigger Input NWDI (only MLX80031/51)

This input is used to trigger the integrated window watchdog in MLX80031/51. Every falling edge on NWDI in watchdog open window is used to reset the watchdog timer. An internal pull up resistor of 250k secures a stable high condition if this pin is open. The NWDI input is a low voltage CMOS input.

3.13. Watchdog Oscillator Resistor RB_{WD} (only MLX80031/51)

A resistor between RB_{WD} and GND defines the window watchdog times as trigger time and reset time.

3.14. Mode Input MODE (only MLX80031/51)

Special pin for to disable the window watchdog function. For normal watchdog operation connect the MODE pin to GND directly or via external resistor. With MODE pin on 3.3V/5V the window watchdog is switched off.

LIN System Basis ICs

4. Operational Modes

The MLX8003x/5x provides four main operating modes "Standby", "Normal", "Silent" and "Sleep". The main modes are fixed states defined by basic actions (VS start, EN or wake-up).

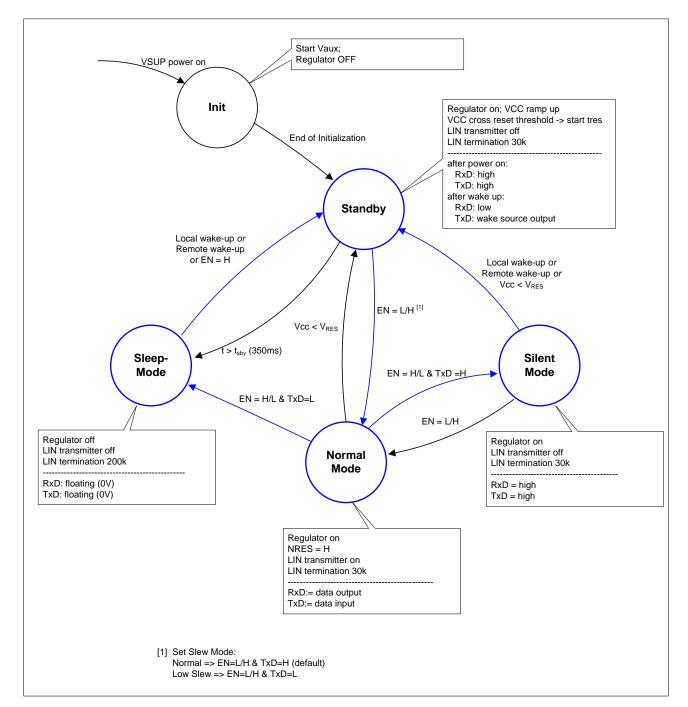


Figure 5: MLX8005x3x state diagram of modes of operation



LIN System Basis ICs

4.1. Modes Overview

Table 7: MLX80050/30 Operation Modes

Mode	VCC	TxD	RxD	LIN	remarks
Standby	3.3V/5V	high	high	recessive	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	[1]
Silent	3.3V/5V	high	high	recessive	high = 3.3V/5V
Sleep	0	floating	floating	recessive	remote wake up to enter Standby Mode, EN = H to go to Normal Mode

^[1] Normal mode will be entered form Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled

Table 8: MLX80051/31 Operation Modes

Mode	vcc	TxD	RxD	LIN	INH	Watchdog	remarks
Standby	3.3V/5V	High/ active low ^[1]	high/ active low ^[2]	recessive	ON	ON	entered after power on or wake up
Normal	3.3V/5V	input for transmit data stream	output for LIN data stream	follows TxD	ON	ON	[3] [4] [5]
Silent	3.3V/5V	high	high	recessive	OFF	OFF	
Sleep	0	floating	floating	recessive	OFF	OFF	Local or remote wake up to enter Standby Mode, EN = H to go to Normal Mode

^[1] Indicates the wake up flag in case of local wake up

^[2] After power on RxD is going high via pull-up to Vcc. If any wake up(local or remote) occurs it will be indicated by active low

^[3] Active low interrupt at pin RxD will be removed when entering normal mode

^[4] Wake up source flag at pin TxD will be removed when entering normal mode

Normal mode will be entered from Standby Mode by a low -> high transition on pin EN and from Sleep Mode by EN = H after startup of the regulator. When recessive level (high) on pin TxD is present the transmit path will be enabled



LIN System Basis ICs

4.2. Initialisation and Standby mode

When the battery supply voltage VS exceeds the specified threshold V_{SUVR_OFF} , the MLX8003x/5x automatically enters the Standby Mode. Following internal procedure is running:

First.

- Start of internal supply Vaux and POR of Vaux
- Start of internal RC oscillator

Second and parallel after POR:

> Start of voltage regulator

The output voltage V_{CC} ramps up to nominal value. The pin RxD is floating and the integrated slave pull up resistor with decoupling diode pulls the pin LIN. The transmitter as well as the receiver is disabled.

If there occurs no mode change to Normal Mode via an EN LOW to HIGH transition within the time stated (typically 350ms), the IC enters the most power saving Sleep Mode.

Furthermore the standby mode will be entered after a valid local or remote wake up event, when the MLX8003x/5x is in Sleep or Silent mode. The entering of the standby mode after wake up will be indicated by an active LOW interrupt on pin RxD.

4.3. Normal Mode

This mode is the base mode. The bus transceiver is able to send with a max baud rate of 20kbit/s.

The whole MLX8003x/5x is active. The incoming bus traffic is detected by the receiver and transferred via the RxD output pin to the microcontroller.

To exit the Normal Mode with on of the following condition:

- 1. High-to-low edge on EN pin with TxD = H -> switch to Silent Mode
- 2. High-to-low edge on EN pin with TxD = L -> switch to Sleep Mode
- Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

Low Slew Mode

The first rising edge on EN after power-on defines the slew rate of the device. With TxD = High at this point works the MLX8003x/5x with normal slew rate (default state). TxD = Low activates the Low Slew Mode, as long as $VS > V_{SUVR_OFF}$.

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

LIN System Basis ICs

4.4. Silent Mode

The Silent Mode is a special mode for application with active Sleep Mode on LIN, but the connected MCU still needs to be supplied with VCC.

With a falling edge on EN input in combination with TxD=high switches the MLX8003x/5x from Normal Mode to the Silent Mode with reduced internal current consumption.

In Silent Mode the voltage regulator is on with a 2% tolerance. The transmitter is disabled and the pin RxD is disconnected from the receive path and is floating. The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected; only a weak curernt source is applied to the LIN bus. Value is typical -75uA, limits -20...-100uA.

To exit the silent mode with on of the following condition:

- 1. Low-to-high edge on the EN pin -> switch back to normal mode
- 2. Remote wake up (all versions) or local wake up request (MLX80031/51 only) -> switch to standby mode
- 3. Undervoltage monitor on VCC detects a low voltage reset condition (VCC < V_{RES}) -> switch back to stand-by mode.

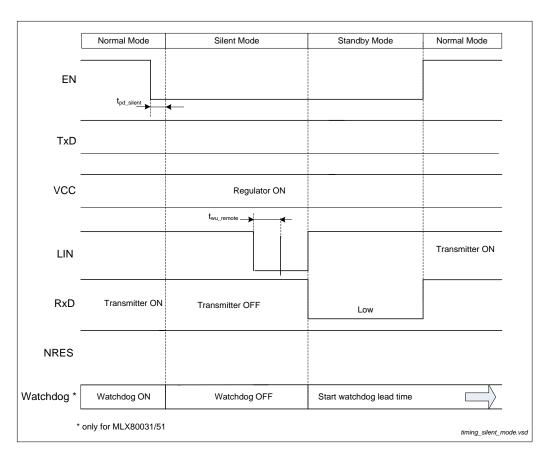


Figure 6: LIN wake-up from Silent Mode



LIN System Basis ICs

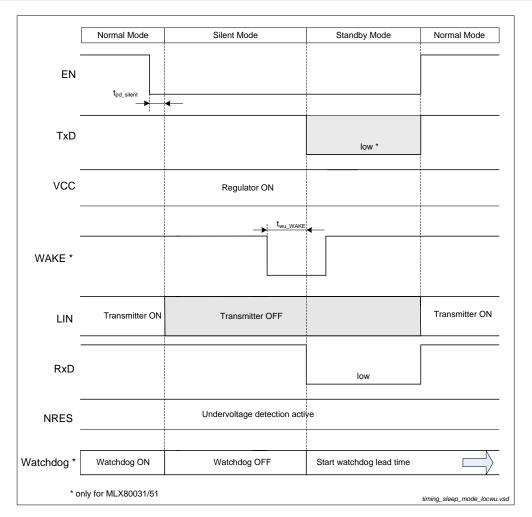


Figure 7 Local Wake-up from Silent Mode via WAKE

4.5. Sleep Mode

The most power saving mode of the MLX8003x/5x is the Sleep Mode. The MLX8003x/5x offers two procedures to enter the sleep mode:

- The mode is selected from normal mode with a falling edge on EN in combination with TxD = L.
- If the MLX8003x/5x is in Standby Mode after power-on or wake-up, a sleep counter is started and switches the transceiver into Sleep Mode after the specified time (typ. 350ms) even when the microcontroller of the ECU will not confirm the normal operation by setting the EN pin to logic HIGH. This new feature allows faulty blocked LIN nodes to reach always the most power saving mode.

Being in Sleep Mode the voltage regulator switched off in order to minimize the current consumption of the complete LIN node. The transmitter is disabled and the pin RxD is disconnected from the receive path and is low (follows VCC). The slave termination resistor (LIN pull up resistor with decoupling diode between pins LIN and VS) is disconnected, only a weak current source is applied to the LIN bus (see chapter 8 fail-safe features)

To exit the Sleep Mode with one of the following condition(s):

1. Remote (all versions) or local wake up request (MLX80031/51 only) -> Switch to Standby Mode



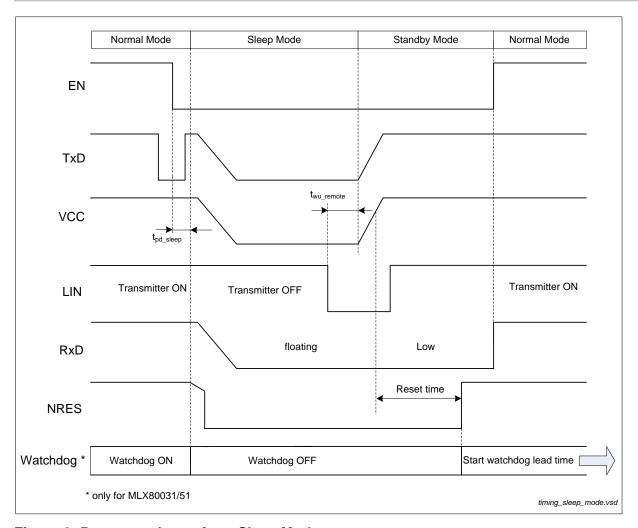


Figure 8: Remote wake-up from Sleep Mode

LIN System Basis ICs

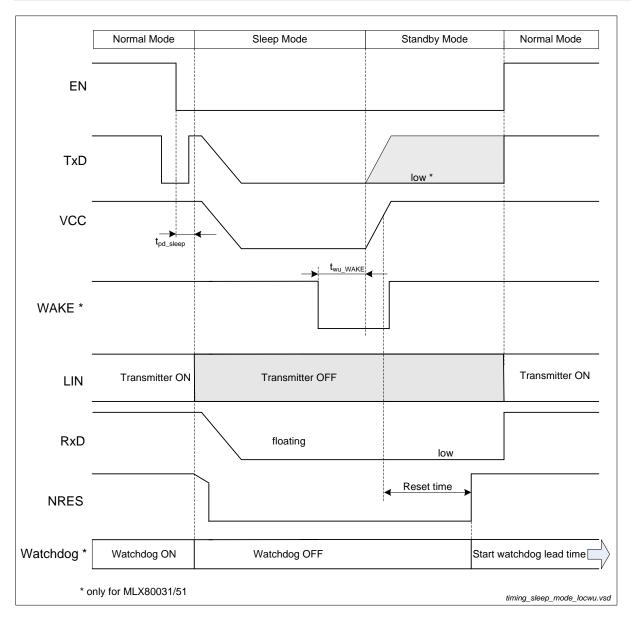


Figure 9: Local wake-up from Sleep Mode

4.6. Init-State

This is an intermediate state, which will pass through after switch on of VS or after undervoltage detection VS with VS < V_{SUVR_ON} . The internal supply voltage Vaux ramp up and the initial readout procedure off zenerzap storage are started. On the end off this phase the VCC voltage definition and the definition of MLX8003x5x version is established. This Init-State changes to Standby Mode with the start of VCC regulator.



LIN System Basis ICs

5. Wake Up Procedures

The MLX80030/50 versions offer only remote wake-up:

• After a falling edge on the LIN bus followed by a dominant voltage level for longer than the specified value (t_{wu_remote}) and a rising edge on pin LIN will cause a remote wake up. The device switches to Standby Mode and the wake-up request is indicated by an active LOW on pin RxD.

The MLX80031/51 versions offer three wake-up procedures:

- In applications with continuously powered ECU a wake up via mode transition to normal mode is possible (see chapter 4.3 Normal Mode)
- Remote wake-up via LIN bus traffic
 After a falling edge on the LIN bus followed by a dominant voltage level for longer than the specified value(t_{wu_remote}) and a rising edge on pin LIN will cause a remote wake up (see)
- Local wake-up via a negative edge on pin WAKE
 A negative edge on the pin WAKE and a dominant voltage level for longer than the specified time (t_{wu_WAKE}) will cause a local wake-up. The current for an external switch has to be provided by an external pull up resistor R_{WK}. For a reverse current limitation in case of a closed external switch and a negative ground shift or an ECU loss of ground a protection resistor R_{WK_prot} between pin WAKE and the switch is recommended.
- Local wake-up via a positive edge on pin KL15 A positive edge on the pin KL15 followed by a high voltage level for a time period t_{wu_KL15} > 250μs results in a local wake-up request. The MLX80031/51 switches to the Standby Mode. The long debouncing time on KL15 suppress unintentional transients in a certainly way. A high level on KL15 has no influence of switching between modes with EN input. Before a new local wake-up request via KL15 can be started, KL15 have to be switched to low level for a time > 250μs.

5.1. Wake Up Source Recognition in MLX80031/51

The device can distinguish between a local wake-up event (pin WAKE or pin KL15) and a remote wake-up event. The wake-up source flag is set after a local wake-up event and is indicated by an active LOW on pin TxD.

The wake-up flag can be read if an external pull up resistor towards the microcontroller supply voltage has been added and the MLX80031/51 is still in standby mode:

- LOW level indicates a local wake-up event
- HIGH level indicates a remote wake up event

The wake-up request is indicated by an active LOW on pin RxD and can be used for an interrupt. When the microcontroller confirms a normal mode operation by setting the pin EN to HIGH, both the wake-up request on pin RxD as well as the wake-up source flag on pin TxD are reset immediately.

LIN System Basis ICs

6. Functionality

6.1. RESET behaviour of MLX8003x/5x

The MLX8003x/5x contains a reset unit which secures the correct initialization and generation of the reset signal. The *NRES* pin outputs the reset state of the MLX8003x/5x. The POR timer will be started if V_S is switched on and $V_{CC} > V_{RES}$ threshold. After the time t_{Res} the *NRES* output is switched from low to high.

The reset unit combines a VCC low voltage detection unit with fixed reset timer. This output is switched from low to high if V_S is switched on and after the time t_{Res} is $V_{CC} > V_{RES}$.

All conditions which cause a drop of the V_{CC} voltage will be detected from the low voltage reset unit which generates a reset signal. The MLX8003x/5x will be reinitialized if the V_{CC} voltage rises above the low voltage limit

If the voltage V_{CC} drops below V_{RES} then the *NRES* output is switched from high to low after the time t_{rr} has been reached. For these reason short breaks of the V_{CC} voltage and uncontrolled reset generations will be inhibited.

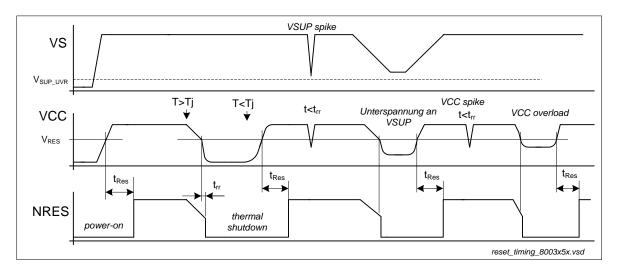


Figure 10: VCC reset behavior

The MLX80031/51 version combines the reset behaviour described at point above with a window-watchdog unit.

The NRES pin outputs the reset state as well as the watchdog condition. The POR timer will be started if V_{SUP} is switched on and V_{CC} > POR threshold. After the time t_{Res} the RESET output is switched from low to high. The watchdog is disabled during this POR procedure. After the POR delay the NRES output is switched from low to high and the watchdog starts. In normal mode the NRES pin outputs the status of the window watchdog.

6.2. **Thermal Shutdown**

If the junction temperature T_J is higher than T_{JSHD} , the MLX8003x/5x will be switched from any mode into Standby Mode. During TSD all functions are switched-off. The transceiver is completely disabled; no wake-up functionality is available.

If T_J falls below the thermal recovery temperature T_{JREC} , the MLX8003x/5x will resume operation starting from Standby Mode. If EN=H at recovery, chip switches to NORMAL after VCC>VRES and tres. SBY-timeout timer is disabled during TSD.



LIN System Basis ICs

6.3. VS under voltage reset

The under voltage detection unit prevents an undefined behaviour of the MLX8003x/5x under low voltage condition (VS < V_{SUVR_ON}). If VS drops below V_{SUVR_ON} , the under voltage detection becomes active and the IC will be switched from every state to Init-State followed by Standby Mode with the same behaviour like after VS power-on. With the following increase of VS above V_{SUVR_OFF} the MLX8003x5x remains in Standby Mode and the voltage regulator starts with the initialization sequence (Vcc available). If EN=H at power-up, the chip switches to NORMAL after VCC>VRES and tres.

Remark: In case Vs drops below 5V but still remains above V_{SUVR_ON} , Vcc follows Vs. Vcc is switched off during Vs Undervoltage reset.

6.4. LIN-Transceiver

The MLX8003x/5x has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.

The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a debouncing unit.

Transmit Mode

During transmission the data at the pin TxD will be transferred to the LIN driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the LIN driver has an integrated slew rate control and wave shaping unit.

Transmitting will be interrupted in the following cases:

- Sleep Mode
- Silent Mode
- Thermal Shutdown active
- Power on Reset

The recessive LIN bus level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of V_{LIN} during differential voltage between VS and LIN ($V_{LIN}>V_S$). No additional termination resistor is necessary to use the MLX8003x/5x in LIN slave nodes. If this ICs are used for LIN master nodes it is necessary that the LIN pin is terminated via an external $1k\Omega$ resistor in series with a diode to VBAT.

Receive Mode

The data signals from the LIN pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

Slew Modes and Data rates

The MLX8003x/5x consists a *constant slew rate* transceiver which means that the bus driver works with a mode depended slew rate. In normal mode the slew rate is typical 1.6 V/µs (max. baud rate 20kbit/s) and in low slew mode typical 0.8 V/µs. The lower slew rate in low slew mode associated with a baud rate of 10.4kbit/s improves the EME behaviour.

The LIN transceiver of MLX8003x/5x is compatible to the physical layer specification according to LIN 2.x specification for data rates up to 20kbit/s and the SAE specification J2602 for data rates up to 10.4kbit/s.

The constant slew rate principle is very robust against voltage drops and can operate with RC- oscillator systems with a clock tolerance up to $\pm 2\%$ between 2 nodes.



LIN System Basis ICs

Low Slew Mode

In this mode the slew rate is switched from the normal value of typical $1.6V/\mu s$ to a low value of typical $0.8V/\mu s$. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10 MHz.

6.5. Voltage Regulator

The MLX8003x/5x has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 3.3V/5V $\pm 2\%$ and a current of ≤ 70 mA within an input voltage range of 6V \leq V_{SUP} \leq 18V. The current limitation unit limits the output current for short circuits or overload to 130mA respectively drop-down of the V_{CC} voltage.

LIN System Basis ICs

7. Window-Watchdog (only MLX80031/51)

The integrated window watchdog unit observes the correct function of the connected Microcontroller. The required timing can be programmed with an external resistor connected to the pin RB_{WD} . This resistor defines together with an internal capacitor the watchdog oscillator frequency. The watchdog is re-triggered by the Microcontroller via the NWDI input. The watchdog status is represented by the NRES pin.

Negative edges on NWDI reset the watchdog timer. If no pulse is received at NWDI, the MLX80051/31 generates low pulses on the NRES output with a pulse width of twDres and a period of twDres.

7.1. MLX80031/51 Watchdog Behaviour

After power-on and elapsed reset time t_{res} , the window watchdog starts operation with a rising edge on pin NRES. This start is independent from Standby or Normal Mode.

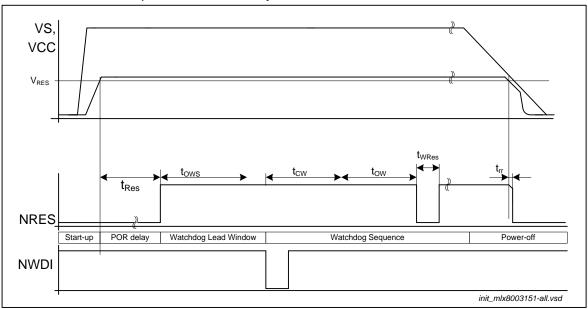


Figure 11: MLX80031/51 Watchdog behavior

In case of Silent or Sleep Mode are left via remote wake-up (LIN) or local wake-up (WAKE or KL15), the window watchdog starts immediately after entering Standby Mode.

After t_{res} the window watchdog unit starts with the Lead Time State. At this state the watchdog clock periods $(1/f_{wdosc})$ are counted 7895(=nlead) times. A negative edge on NWDI pin within this lead time stops the lead counter and activates the Close Window State with ncw=1053. Thereafter follows the Open Window State with counter start value of now=1105. In case the lead counter elapses, the watchdog enters the Reset State and starts the reset timer with time tres.

Close Window State and Open Window State are the normal states of the window watchdog. At each of these states runs a counter with the watchdog clock signal. The CWT counter runs always to the end. The watchdog will only trigger correctly if the NWDI trigger signal arrives within the Open Window State.

A NWDI trigger pulse outside the open window generates a reset condition and the NRES output switches to low for the time t_{WDres} (see Figure 12).



LIN System Basis ICs

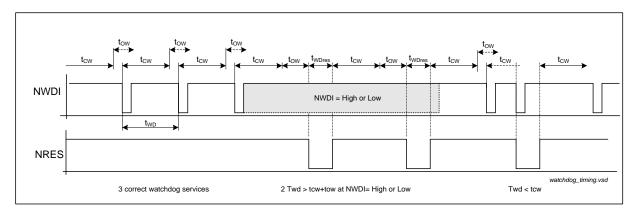


Figure 12: Watchdog timing

7.2. All watchdog start-up scenarios

7.2.1. After power-on and initialization

Watchdog started after VCC ramp up and the finishing of reset timer (typ. 4ms) with Lead Time State. MLX80031/51 is in Standby or Normal Mode

7.2.2. Wake up indicated transition to Standby Mode from Sleep or Silent Mode

Watchdog started immediately with activating of Standby Mode (SBY_MODE = 1). By transition from Sleep Mode the VCC regulator ramps up also and the reset timer starts. The reset timer has in this case no influence for the watchdog start.

7.2.3. Undervoltage reset on VCC on Normal Mode or Silent Mode

MLX80031/51 goes to Standby Mode. Running watchdog process is stopped and cleared. With active undervoltage reset the signal the output pin NRES goes to low. With leaving of undervoltage reset start the reset timer (4ms) and after them start a new watchdog procedure.

7.2.4. EN indicated transition from Silent Mode to Normal Mode

Mode control goes from Silent Mode to Normal Mode. Watchdog started immediately with activating of Normal Mode with Close Window State.



LIN System Basis ICs

7.3. Calculation of Watchdog Period

The RC-oscillator of MLX80031/51 which generates the responsible timing of the watchdog has a tolerance of $\pm 15\%$. This has the consequence that also the watchdog window times t_{CW} and t_{OW} variants with this tolerance.

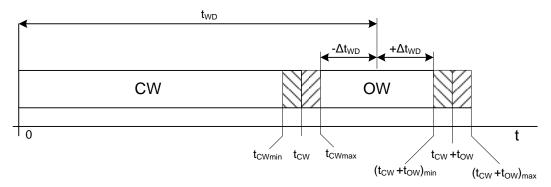


Figure 13: Watchdog open and close window tolerances

The ideal watchdog period can be calculated with:

$$twD_{-id} = t_{cw} + \frac{1}{2} * tow$$

The average value t_{WD} of the real usable watchdog trigger time under consideration of the oscillator tolerance is:

$$twD = (tCW min + tOW min + tCW max)/2$$
 [EQ1]

The allowed tolerance Δt_{WD} is:

$$\Delta t_{WD} = (t_{CW min} + t_{OW min} - t_{CW max})/2$$
 [EQ2]

With the definition of t_{CW} = ncw * (1± TOL) * t_{WDOSC} and t_{OW} = now * (1± TOL) * t_{WDOSC} from [EQ1] t_{WD} can be calculated with:

$$twD = twDOSC(2 \cdot ncw + now \cdot (1 - TOL))/2$$
 [EQ3]

and with [EQ2]:

$$\Delta t_{WD} = t_{WDOSC} (now \cdot (1 - TOL) - 2 \cdot TOL \cdot ncw)/2$$
 [EQ4]

The variation Δt_{WD} will be normalized to the mean value t_{WD} and both counter values set in a relationship of a=now/ncw, then follows for the relative deviation:

$$twDTOL = \frac{a \cdot (1 - TOL) - 2 \cdot TOL}{2 + a \cdot (1 - TOL)}$$
 [EQ5]

The watchdog trigger time as well as the tolerance depends only on the oscillator frequency respectively the period t_{WDOSC} , if the there are fixed values for both counters (ncw and now) and oscillator tolerance.

Implemented in MLX80031/51 is a precision RC oscillator with a tolerance of TOL = $\pm 15\%$. Combined with the relation of counter values a=1.04 reached them a tolerance of trigger time of $\pm 20\%$.

LIN System Basis ICs

Table 9: Parameters of Window Watchdog

Symbol	Parameter	Value
TOL	Tolerance WD oscillator	±15%
ncw	Close window counter	1053
now	Open window counter	1105
t _{WDTOL}	Tolerance WD-trigger time	±20%

With the predefined counter values (ncw and now) and the oscillator tolerance TOL are the trigger time of watchdog and them tolerance only be calculated by the selection of oscillator frequency, or their period t_{WDOSC} .

Fort the used precision RC-oscillator the oscillator period is shown as a linear function of the external resistor RB_{WD} .

$$twDOSC[\mu s] = 0.3486 \cdot RBwD[k\Omega] + 1.117$$
 [EQ6]

The trigger period can be calculated with the help of EQ3 together with Table 9 – Parameter of Window Watchdog

$$twD[ms] = 0.53078 \cdot RBwD[k\Omega] + 1.70$$
 [EQ7]

Or convert to RB_{WD}:

$$RB_{WD}[k\Omega] = 1.883 \cdot tWD[ms] - 3.20$$
 [EQ8]

Some samples of different RD_{WD} values and the corresponding watchdog times:

Table 10: Window Watchdog Timing Selection

RB_{WD} [k Ω]	t _{wDOSC} [μ s]	Lead Time t _{LEAD} [ms]	Close Window t _{CW} [ms]	Open Window tow [ms]	Trigger Period t _{WD} [ms]
20	8.09	63.9	8.52	8.94	12.32
30	11.58	91.4	12.19	12.79	17.62
51	18.90	149.2	19.90	20.88	28.77
75	27.26	215.2	28.71	30.12	41.51
100	35.98	284.0	37.88	39.75	54.78
120	42.95	339.1	45.23	47.46	65.40
150	53.41	421.6	56.24	59.01	81.32

Short or open circuit on RB_{WD}

The MLX80031/51 can detect a short circuit against GND on the RB_{WD} pin or an open RB_{WD} pin. If on pin a resistor RB_{WD} <330 Ω or RB_{WD} >10M Ω detected, then the MLX80031/51 checks during the initialization phase a fail-safe state. The watchdog oscillator will be set in a fail-safe mode with an oscillator period of about 50 μ s.



LIN System Basis ICs

8. Fail-safe features

Loss of battery

If the ECU is disconnected from the battery, the LIN bus pin is in high impedance state. There is no impact to the bus traffic and to the ECU itself. Reverse current is limited to $< 20\mu A$

Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus line. The current from the ECU to the LIN bus is limited by the weak pull up resistor of the pin LIN. The slave termination resistor is disconnected in order to fulfil the SAE J2602 requirements for the loss of ground current (<100µA @12V).

Short circuit to battery

The transmitter output current is limited to the specified value in case of short circuit to battery in order to prevent high current densities and thermal hot spots in the LIN driver.

Short circuit to ground

If the LIN bus wiring is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the bus and no distortion of the bus traffic occurs.

If the controller detects a short circuit of the LIN bus to ground the transceiver can be set into sleep mode. Additionally the internal slave termination resistor is switched off and only a weak pull up termination is applied to the LIN bus (typ. 50µA). If the failure disappears, the bus level will become recessive again and will wake up the system even if no local wake up occurs or is possible.

Thermal overload

All MLX8003x/5x versions are protected against thermal overloads. If the chip temperature exceeds the specified value, the transmitter is disabled until thermal recovery and the following recessive to dominant transition on pin TxD. The receiver is still working while thermal shutdown.

Undervoltage lock out

If the battery supply voltage is missing or decreases below the specified value (VS_UV), the transmitter is disabled to prevent undefined bus traffic. While in sleep mode, the MLX8003x/5x enters the Standby Mode if Vs drops below the internal power on reset threshold.

Open Circuit protection

- The pin TxD provides a pull up resistor to VCC. The transmitter can not be enabled.
- The pin EN provides a pull down resistor to prevent undefined normal mode transitions.
- The pin NWDI provides a pull up resistor to VCC. The window watchdog generates NRES pulse.
- The pin MODE provides a pull down resistor to GND. No influence on window watchdog.
- If the battery supply voltage is disconnected, the pin RxD is floating.
- The pin WAKE provides a weak pull up current towards supply voltage Vs to prevent local wake-up requests.
- The pin KL15 provides a weak pull down current towards GND to prevent local wake-up requests.

Short circuit RxD, NRES against GND or VCC

Both outputs are short circuit proof to VCC and ground.

RBWD short circuit against GND or open

The watchdog oscillator runs with an internal controlled frequency and guarantees a reset.

LIN System Basis ICs

9. Application Hints

9.1. Safe Operating Area

The linear regulator of the MLX8003x/5x operates with input voltages up to 27 V and can output a current of 70 mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 70 mA at an ambient temperature of $T_A = 125$ °C is only possible with small voltage differences between V_S and V_{CC} .

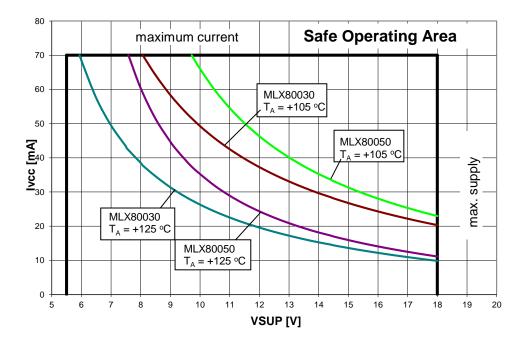


Figure 14: Safe operating area for MLX80030/50 in SOIC-8 for Vsup up to 18V

LIN System Basis ICs

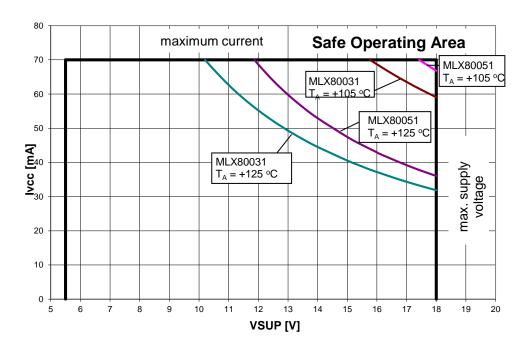


Figure 15: Safe operating area for MLX80031/51 in QFN20 for Vsup up to 18V

9.2. Application Circuitry

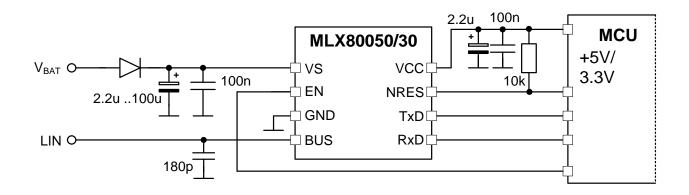


Figure 16: Application circuit with MLX80050 or MLX80030 (slave node)



LIN System Basis ICs

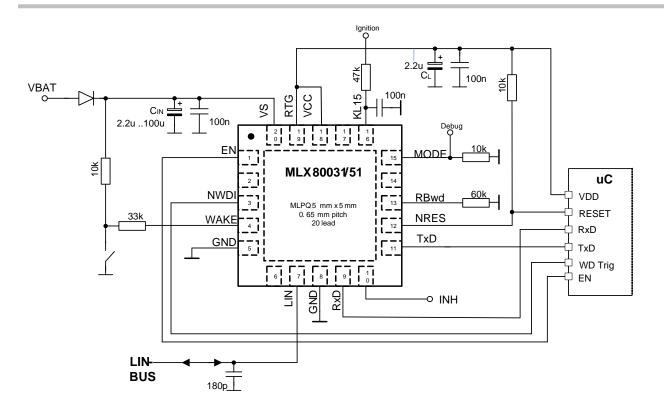


Figure 17: Application circuit with MLX80031 or MLX80051 (slave node)

9.2.1. EMI Suppressing

To minimize the influence of EMI on the bus line an 180pF capacitor should be connected directly to the LIN pin (see 0). This EMI-Filter assures that the RF injection into the IC from the LIN bus line has no effect or will be limited.

It is also possible to use LC- or RC-filters. The dimensions of C-L or R-L depend on the corner frequency, the maximum LIN bus capacitance (10nF) and the compliance with the DC- and AC LIN bus parameters.

9.2.2. EMC disturbances using the example of MLX80030/50

The MLX80030/50 complies with the standards ISO 7637 part1 and 2 (immunity against transients) and IEC 62132 part 1 and 4 (immunity against RF). The check bases on the document: "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications" V1.0 from 2008-12-10, chapter 5 "EMC Requirements". The tests will be performed on a common test PCB.



LIN System Basis ICs

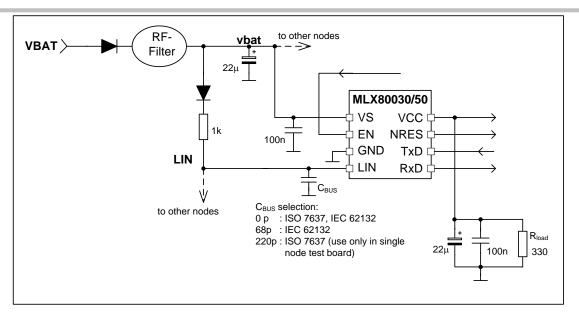


Figure 18: Part of test circuitry for EMC tests with MLX80030/50

The standard test board includes 3 LIN nodes with MLX80030/50. The load condition at VCC pin is a compromise between the requirements described in the document named before and the use of MLX80030/50 in practical applications.

The demand of 80% of max load condition means at Normal Mode and Silent Mode 56mA (max. 70mA). In practical application both modes will be used under consideration of save operating area. This leads to a max load value of 15mA or 330 Ohm for Rload.

Failure criterion for all EMC tests is functional status class A. The following table defines the parameter ranges for the pins RxD (dig out), NRES (dig out), VCC (supply out) to fulfil the functional state A at each operating mode.

Table 11: Parameter ranges for function state A (MLX80050)

Mode	Transmitter	VCC	RxD	NRES
Normal	ON	Supply ON: 4.75V 5.25V	High and Low state with Vcc ±0.9V	High state: min level: Vcc – 1V
Silent	OFF	Supply ON with reduced load 4.75V 5.25V	High state: min level: Vcc – 1V	High state: min level: Vcc – 1V
Sleep	OFF	Supply OFF: 0V 0.9V	no evaluation	no evaluation

LIN System Basis ICs

10. Mechanical Specification

10.1. SOIC8 package

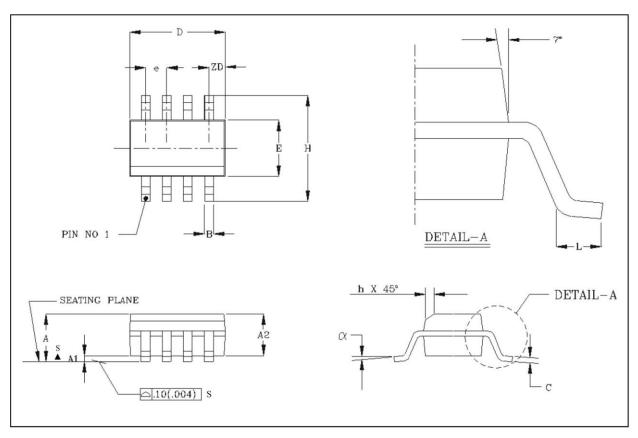


Figure 19: SOIC8 Drawing

Table 12: SOIC8 dimensions

Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

	A1	В	С	D	Е	е	Н	h	L	Α	α	ZD	A2
All Dime	nsion in m	ım, copla	narity < 0	.1 mm									
min max	0.10 0.25	0.36 0.46	0.19 0.25	4.80 4.98	3.81 3.99	1.27	5.80 6.20	0.25 0.50	0.41 1.27	1.52 1.72	0° 8°	0.53	1.37 1.57

LIN System Basis ICs

10.2. **QFN20 5x5 package**

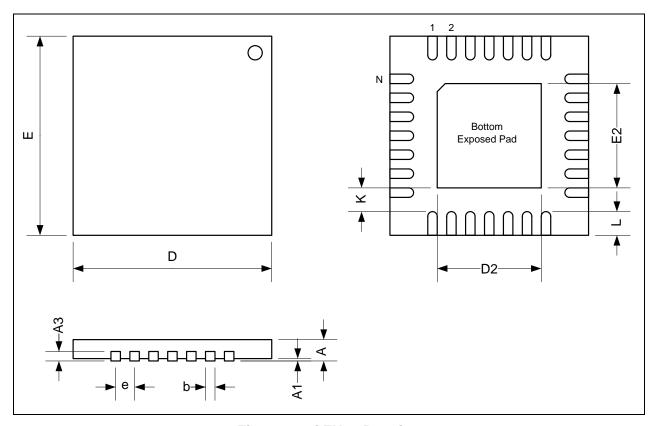


Figure 20: QFN20 Drawing

Table 13: QFN20 Package Dimensions

Symbol	Α	A 1	A3	b	D	D2	E	E2	е	K	L	N [3]	ND [4]	NE [4]	
min	0.80	0	0.20	0.25	E 00	3.00	5.00	3.00	0.65	0.20	0.45	20	E	E	[1] [2]
max	1.00	0.05	0.20	0.35	5.00	3.25	5.00	3.25	0.05	0.20	0.65	20	j j	3	

^[1] Dimensions and tolerances conform to ASME Y14.5M-1994

^[2] All dimensions are in Millimeters. All angels are in degrees

^[3] N is the total number of terminals
[4] ND and NE refer to the number of terminals on each D and E side respectively



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11. Revision History

Version	Changes	Remark	Date
001	First Release	1st Release	April 2012
002	 For TSD added: "If EN=H at recovery, chip switches to NORMAL after VCC>VRES and tres" and "SBY-timeout timer is disabled during TSD" For TSD removed explicit values and kept parameter name only. For Vs_uvr added: "If EN=H at power-up, chip switches to NORMAL after VCC>VRES and tres" Changed state diagram: sleep mode can be left with EN = H (was a L-H transition in A version of the device), refers to Errata 80050AA-07. 		June 2012
003	 ESD robustness level adapted to Conformance Test Report Static Characteristics adapted to CPK-Values Block Diagram updated Corrected short description of product 		Dec 2012
004	 Removed 06.05, 09.05, 13.05 Changed 05.02 to 200mV (5V) and 100mV (3.3V) Changed 06.03 and 13.03 to 700mV Changed 09.03 to 600mV Added MODE pin to parameter list Changed 15.05 to LL = 2.7V and UL to 3.3V Changed 14.01 to 0.6V at 2mA Changed 08.03 to LL = 30 Changed 02.00 to LL = 400 and UL to 1500 Changed Tjshd to 155/170/190°C Changed 12.04 and 12.05 UL to 20uA Changed 03.05 to relevance "C" (only for characterization) Added 17.06 Watchdog safety oscillator Changed 3.01 for 80030/31 to UL = 3.201 and UL = 3.399 		Mar 2013
005	Corrected value "e" of QFN package data to "0.65"		Apr 2013
006	 Changed 15.01 Changed 1.03 LL to 40mV Changed 3.09 LL to -135mA and UL to -75mA Changed ESD capability of LIN pin to +/-6kV 		July 2013
007	 Changed operating voltage to max. 27V Changed table 2, nominal operating voltage, max to 27V Update 3.09: split temperature ranges Changed 12.03 to min: -400μA Changed 12.06 to min: -10μA, max: 50μA Changed 6.04 to typ: 125 kΩ, max: 250 kΩ Changed 12.01 to 80μA 		Feb 2014
800	Added condition for thermal resistance		April 2014



	 Updated chapter 4.1, tables 7 and 8 for TxD and RxD values depending on the mode and EN = H transition from Sleep Mode to Normal Mode Changed operating voltage to 27V max in application hints 9.1 Re-phrased information to EMC compliance in 9.2.2 LIN: Changed parameter 12.10 and added parameter 12.12 to Lin spec 2.x and compatible to SAE J2602, split parameter 12.07 into dominant and recessive 	
009	Updated product codes to "wettable flanks"	Nov 2014



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12. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
 Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
 Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

EN60749-15
 Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

 EIA/JEDEC JESD22-B102 and EN60749-21 Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines <u>soldering recommendation</u> (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx



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13. Disclaimer

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