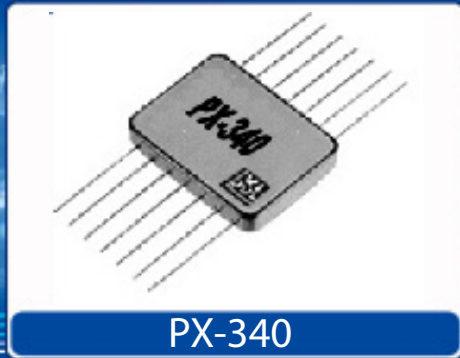


Helping Customers Innovate, Improve & Grow



Features

- Miniature Hybrid Design
- 14 Pin Flatpack
- Frequency Range: 1 HZ to 700 MHZ
- Previous Model: CO-407, CO-447, CO-437, CO-457
- Output Options Available AC MOS, TTL, PECL, ECL

Applications

Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Frequency Stabilities¹					
vs. operating temperature range (referenced to +25°C)	-5		+5	ppm	0... +50°C
	-10		+10	ppm	0... +50°C
	-25		+25	ppm	0... +70°C (standard)
	-50		+50	ppm	-55... +85°C
	-50		+50	ppm	-55... +125°C
	-100		+100	ppm	-55... +125°C
	-300		+300	ppm	-55... +200°C (custom number required)
Initial tolerance	-50		+50	ppm	@+25°C
	-25		+25	ppm	@+25°C
	-15		+15	ppm	@+25°C
	-10		+10	ppm	@+25°C
	-1		+1	ppm	Set via external capacitor (custom number required)
vs. aging / 1 year	-3		+3	ppm	after 30 days of operation
vs. aging / year (following years)	-2		+2	ppm	
Supply Voltage (Vs)					
Supply voltage (Standard)	4.75	5.0	5.25	VDC	
Supply voltage (Option)	3.135	3.3	3.465	VDC	below 20 MHz
Supply voltage		-5.2		VDC	@< 45 mA to 110 MHz, @< 70 mA above 110 MHz
Supply voltage		-4.5		VDC	@< 60 mA

Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
RF Output					
Signal	ACMOS				
Load		15	50	pF	
Signal Level (Vol)			0.5 .3	VDC VDC	with Vs=5.0V and 15pF load with Vs=3.3V and 15pF load
Signal Level (Voh)	4.5 3.0			VDC VDC	with Vs=5.0V and 15pF load with Vs=3.3V and 15pF load
Rise and fall times for ACMOS (measured 10% to 90%)			10 6 3	ns ns ns	1.0 to 23.9 MHz 24.0 to 79.9 MHz 80.0 to 125.0 MHz
Duty cycle	45 40		55 60	% %	@ 50% < 15 MHz @ 50% => 15 MHz

Signal	TTL				
"0" Level			0.4	V	
"1" Level	+2.4			V	
Rise / Fall Time	2		15 5	ns ns	@ (0.5-2.4V), <= 20 MHz @ (0.5-2.4V), > 20 MHz
Symmetry	45 40		55 60	% %	@+1.5 V, < 4 MHz @+1.5 V, >= 4 MHz

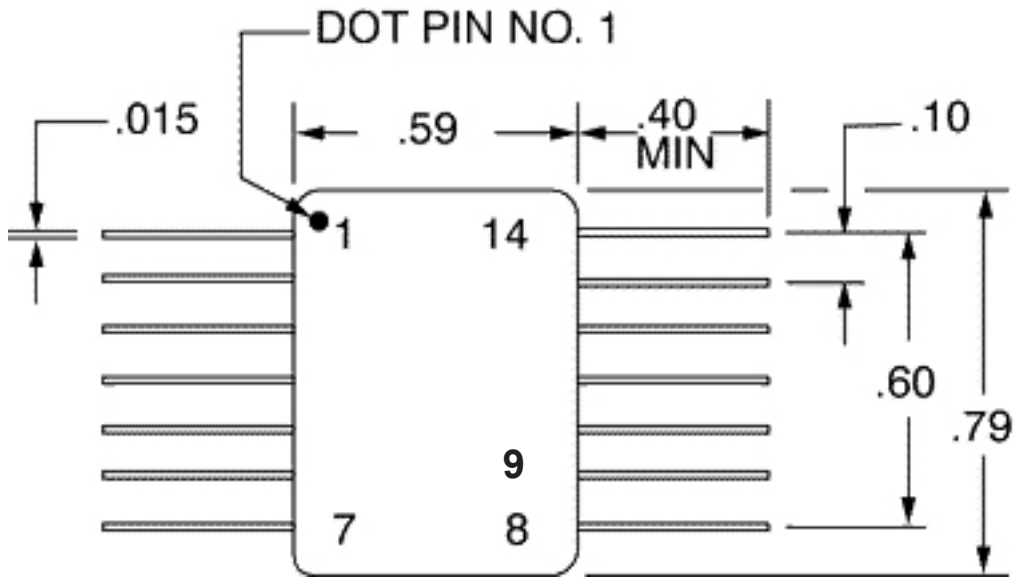
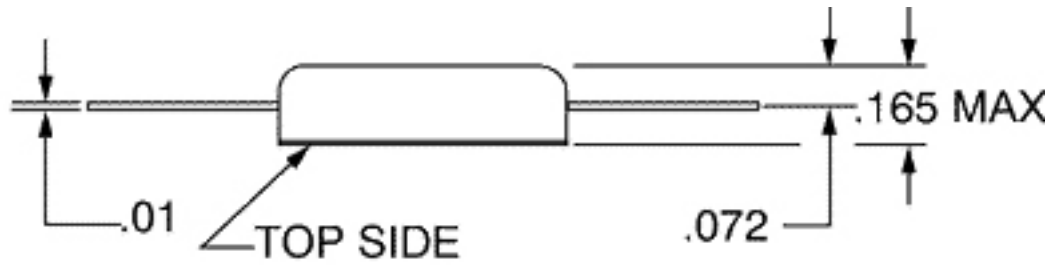
Signal	PECL				
Load			50	ohm	into Vcc-2V or There in Equivalent
Signal Level (Vol)			Vs -1.62	VDC	-40....+85°C operating temp
Signal Level (Voh)	Vs- 1.025			VDC	-40....+85°C operating temp
Rise and fall times for ACMOS (measured 20% to 80%)			1000 600	ps ps	< 100 MHz >= 100 MHz
Duty cycle	45		55	%	@ 50% Vdd

Signal	ECL				
Output					Output taken directly from 10K, 10KH, 100K, ECLinPS or ECLinPS Lite gate, depending on temperature and frequency range. Complementary outputs optional.

Screen Testing of Above Models

SCREEN TEST	MIL-STD-883 METHOD	Standard	Options	
		CLASS X	CLASS B	CLASS S
Stabilization Bake (150°C)	—	X	X	Class S screen test requirements include 24 hour additional bake-out, 80 hour additional burn-in, thermal shock, PIND test and radiographic inspection in addition to Class B Screening. Has major cost impact.
Seal Test (Gross and Fine)	1014, Cond A2	X	X	
Temperature Cycling (Thermal Shock)	1010, Cond B		X	
Burn-in, operating 160 hours @125°C	—		X	
Acceleration (5000g in Y1 axis)	2001, Cond A		X	

Outline Drawing / Enclosure



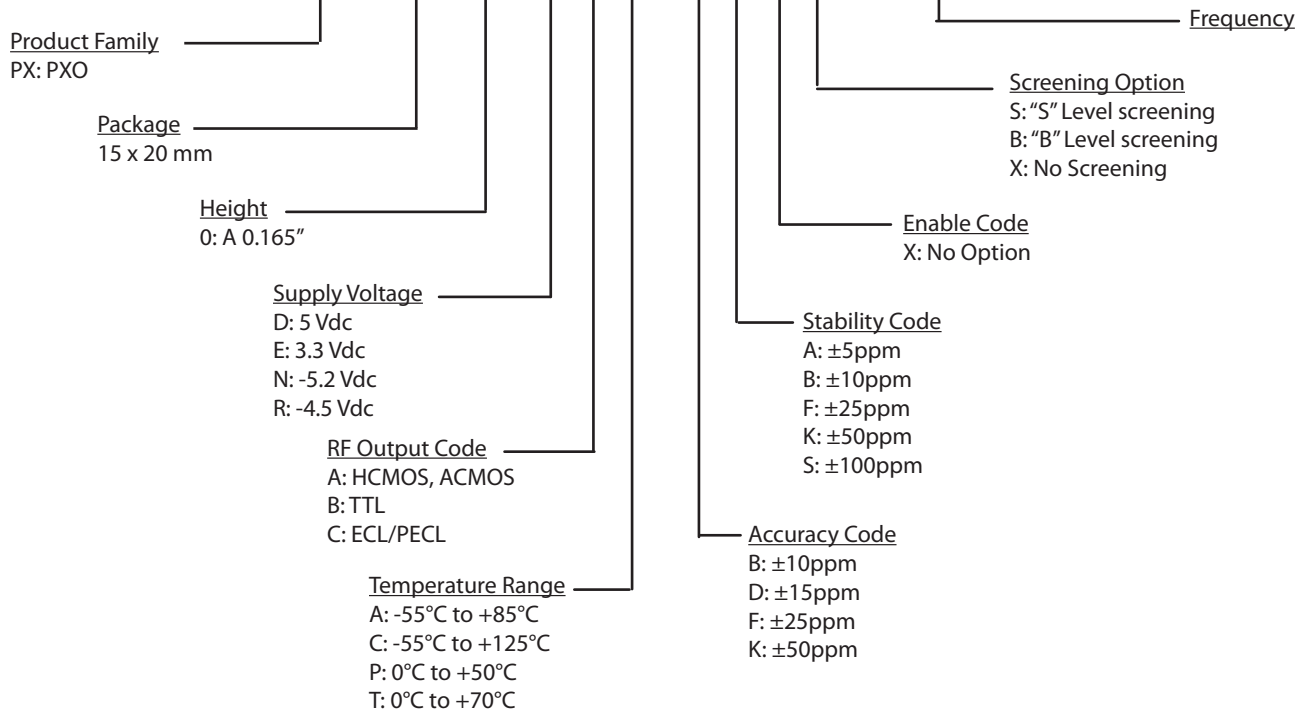
Dimensions in inches

Type A		
Code	Height "H"	Pin Length "L"
0	0.165	0.4

Pin Connections	
1	No Connect
7	Ground
8	Output
9	Complementary Output (if requires)
14	Supply

Ordering Information

PX - 340 0 - A A T - E K X S - 10M000000



Notes:

1. Contact factory for improved stabilities or additional product options. Not all options and codes are available at all frequencies.
2. Unless other stated all values are valid after warm-up time and refer to typical conditions for supply voltage, frequency control voltage, load, temperature (25°C).
3. Phase noise degrades with increasing output frequency.
4. Subject to technical modification.
5. Contact factory for availability.

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