High Performance Registered 1024x4 PROM

53/63RA441

Features/Benefits

- Edge triggered "D" registers
- Advanced Schottky processing
- 4-bit-wide in 18 pin for high board density
- Lower system package counts
- Lower system power
- Faster cycle times
- 16mA I_{OL} output drive capability

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register which holds the micro-instruction during execution, is now incorporated into the PROM chip.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION	PINS	TYPE	MIL	COM
4K	1024x4	18	J, N	53RA441	63RA441

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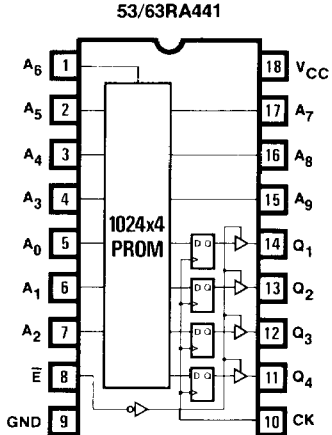
Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard.

Pin Configuration

53/63RA441



2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
t_{su}	Address set-up time	60	30		50	30		
t_h	Address hold time	0	-10		0	-10		
t_w	Clock pulse width	25	8		20	8		
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA				-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = -2mA		2.4			V
			COM I_{OH} = -3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				-40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded	MIL		120	175	mA
			All outputs open	COM		120	165	

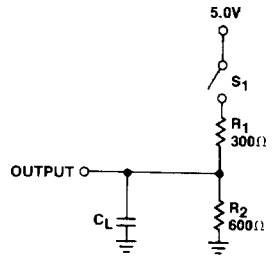
* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at 5.0V V_{CC} and 25°C T_A

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Clock to output access time		20	35		20	30	ns
t_{ER}/t_{EA}	Enable to output access and recovery time		19	35		19	30	ns

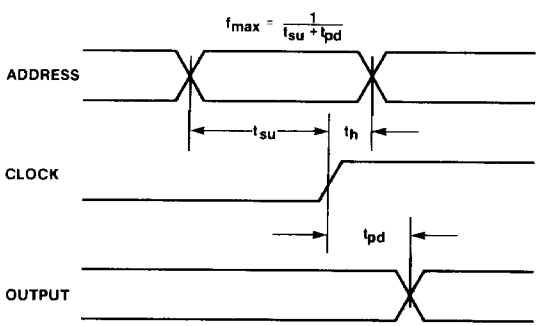
Standard Test Load

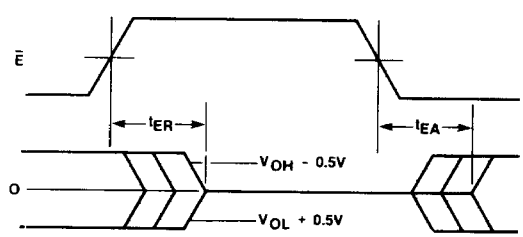


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms





ENABLE ACCESS TIME AND RECOVERY TIME

NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test. TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.