SDRAM MICRODIMM

MT4LSDT864W – 64MB
MT4LSDT1664W – 128MB

For the latest data sheet, please refer to the Micron Web site: www.micron.com/moduleds

Features

- JEDEC-standard, PC100, PC133, 144-pin, MicroDIMM
- Utilizes 125 MHz and 133 MHz SDRAM components
- 64MB (8 Meg x 64), 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 64MB module: 64ms, 4,096-cycle refresh; 128MB module: 64ms, 8,192-cycle refresh.
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

OPTIONS	MARKING
• Self Refresh Current	
Standard	None
Low Power	L
• Package	
144-pin MicroDIMM (standard)	G
144-pin MicroDIMM (lead-free)	Y
• Frequency/CAS Latency	
133 MHz/CL = 2	-13E
133 MHz/CL = 3	-133
100 MHz/CL = 2	-10E

NOTE: 1. Contact Micron for availability of lead-free products.

Figure 1: 144-Pin MicroDIMM (MO–214)

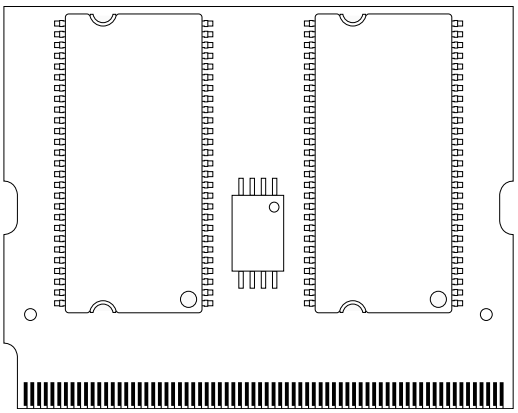


Table 1: Device Timing

MODULE MARKING	PC100 CL - ^{t}RCD - ^{t}RP	PC133 CL - ^{t}RCD - ^{t}RP
-13E	2 - 2 - 2	2 - 2 - 2
-133	2 - 2 - 2	3 - 3 - 3
-10E	2 - 2 - 2	N/A

Table 2: Address Table

	64MB	128MB
Refresh Count	4K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Row Addressing	4K (A0–A11)	8K (A0–A12)
Column Addressing	512 (A0–A8)	512 (A0–A8)
Module Ranks	1 (S0)	1 (S0)
Component Configuration	8 Meg x 16	16 Meg x 16

Table 3: Part Numbers

PART NUMBER	CONFIGURATION	VERSION
MT4LSDT864(L)WG-13E__	8 Meg x 64	133 MHz, CL = 2
MT4LSDT864(L)WY-13E__	8 Meg x 64	133 MHz, CL = 2
MT4LSDT864(L)WG-133__	8 Meg x 64	133 MHz, CL = 3
MT4LSDT864(L)WY-133__	8 Meg x 64	133 MHz, CL = 3
MT4LSDT864(L)WG-10E__	8 Meg x 64	100 MHz, CL = 2
MT4LSDT864(L)WY-10E__	8 Meg x 64	100 MHz, CL = 2
MT4LSDT1664(L)WG-13E__	16 Meg x 64	133 MHz, CL = 2
MT4LSDT1664(L)WY-13E__	16 Meg x 64	133 MHz, CL = 2
MT4LSDT1664(L)WG-133__	16 Meg x 64	133 MHz, CL = 3
MT4LSDT1664(L)WY-133__	16 Meg x 64	133 MHz, CL = 3
MT4LSDT1664(L)WG-10E__	16 Meg x 64	100 MHz, CL = 2
MT4LSDT1664(L)WY-10E__	16 Meg x 64	100 MHz, CL = 2

NOTE:

1. The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT4LSDT864WG-10EB1.

Table 4: Pin Assignment 144-Pin MicroDIMM (Front View)

PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	FRONT
1	VSS	37	DQ8	73	NC	109	A9
3	DQ0	39	DQ9	75	VSS	111	A10
5	DQ1	41	DQ10	77	NC	113	VDD
7	DQ2	43	DQ11	79	NC	115	DQM2
9	DQ3	45	VDD	81	VDD	117	DQM3
11	VDD	47	DQ12	83	DQ16	119	VSS
13	DQ4	49	DQ13	85	DQ17	121	DQ24
15	DQ5	51	DQ14	87	DQ18	123	DQ25
17	DQ6	53	DQ15	89	DQ19	125	DQ26
19	DQ7	55	VSS	91	VSS	127	DQ27
21	VSS	57	NC	93	DQ20	129	VDD
23	DQM0	59	NC	95	DQ21	131	DQ28
25	DQM1	61	CK0	97	DQ22	133	DQ29
27	VDD	63	VDD	99	DQ23	135	DQ30
29	A0	65	RAS#	101	VDD	137	DQ31
31	A1	67	WE#	103	A6	139	VSS
33	A2	69	S0#	105	A8	141	SDA
35	VSS	71	NC	107	VSS	143	VDD

Table 5: Pin Assignment 144-Pin MicroDIMM (Back View)

PIN	BACK	PIN	BACK	PIN	BACK	PIN	BACK
2	VSS	38	DQ40	74	NC	110	BA1
4	DQ32	40	DQ41	76	VSS	112	A11
6	DQ33	42	DQ42	78	NC	114	VDD
8	DQ34	44	DQ43	80	NC	116	DQM6
10	DQ35	46	VDD	82	VDD	118	DQM7
12	VDD	48	DQ44	84	DQ48	120	VSS
14	DQ36	50	DQ45	86	DQ49	122	DQ56
16	DQ37	52	DQ46	88	DQ50	124	DQ57
18	DQ38	54	DQ47	90	DQ51	126	DQ58
20	DQ39	56	VSS	92	VSS	128	DQ59
22	VSS	58	NC	94	DQ52	130	VDD
24	DQM4	60	NC	96	DQ53	132	DQ60
26	DQM5	62	CKE0	98	DQ54	134	DQ61
28	VDD	64	VDD	100	DQ55	136	DQ62
30	A3	66	CAS#	102	VDD	138	DQ63
32	A4	68	NC	104	A7	140	VSS
34	A5	70	NC/A12	106	BA0	142	SCL
36	VSS	72	NC	108	VSS	144	VDD

NOTE:
Pin 70 is a no connect (NC) for 64MB. Pin 70 is A12 for 128MB.

Figure 2: Pin Locations (144-Pin MicroDIMM)

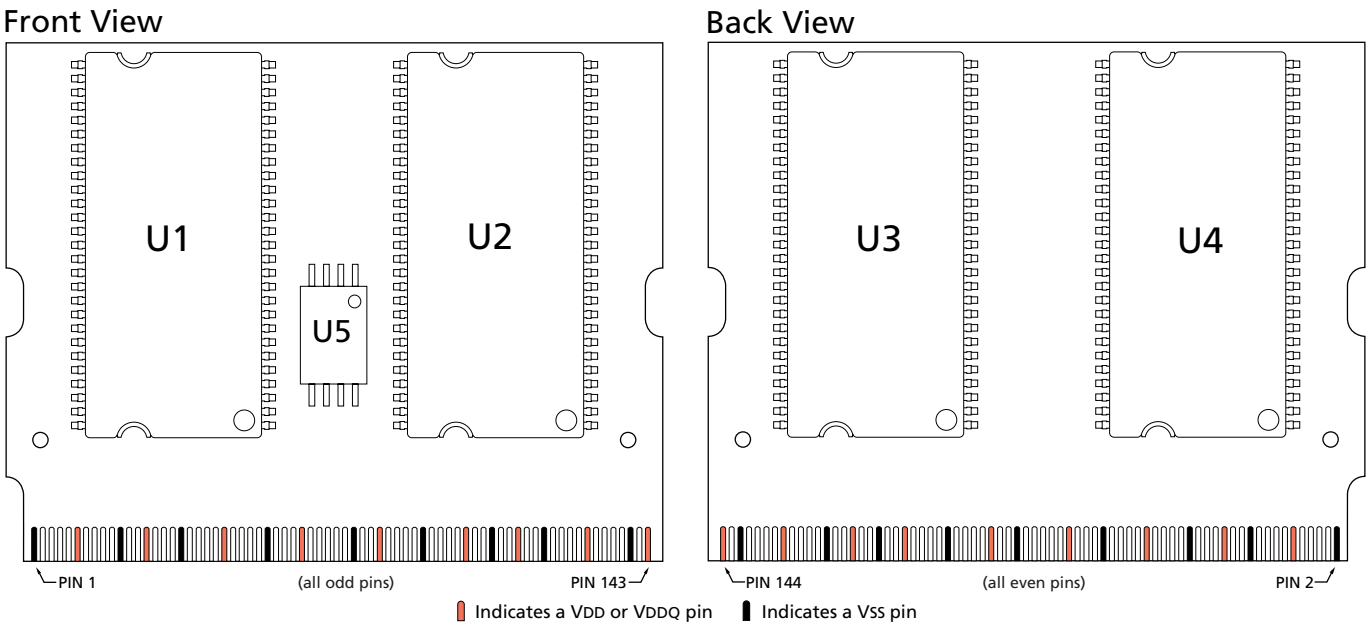
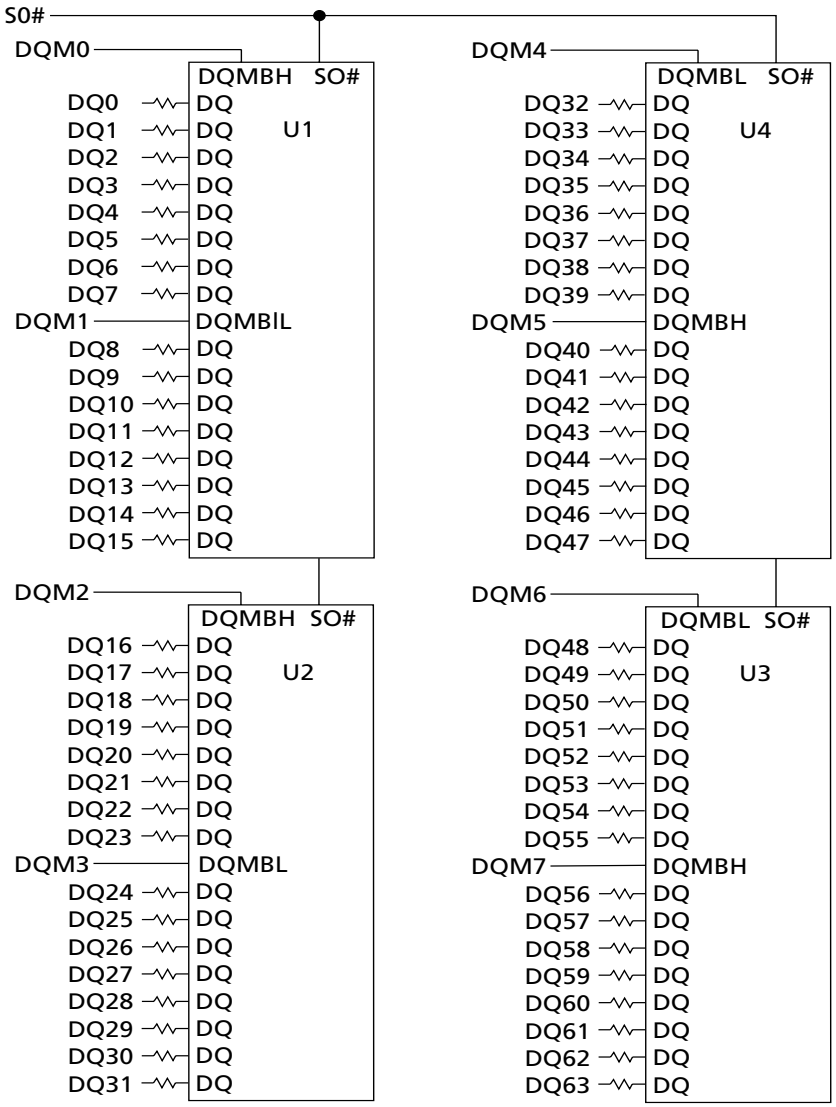


Table 6: Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
65–67	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
61	CK0	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
62	CKE0	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
69	S0#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
23–26, 115–118	DQMB0–DQMB7	Input	Input Mask: DQMB is an input mask signal for write accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
106, 110	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the Mode Register.
29–34, 70 (128MB), 103–105, 109, 111, 112	A0–A11 (64MB) A0–A12 (128MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
142	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchro nize the presence-detect data transfer to and from the module.
3–10, 13–20, 37–44, 47–54, 83–90, 93–100, 121–128, 131–138	DQ0–DQ63	Input/Output	Data I/Os: Data bus.
141	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107, 108, 119, 120, 139, 140	V_{SS}	Supply	Ground.
57 –60, 70 (64MB)–74, 77–80	NC	–	Not Connected: These pins are not connected on these modules.

Figure 3: Functional Block Diagram



NOTE:

All resistor values are 10Ω unless otherwise noted.

SDRAM = MT48LC8M16A2TG for 64MB module
SDRAM = MT48LC16M16A2TG for 128MB module

General Description

The MT4LSDT864(L)W and MT4LSDT1664(L)W are high-speed CMOS, dynamic random-access, 64MB and 128MB memory modules, organized in a x64 configuration. These modules use SDRAM devices internally configured as quad-bank DRAM devices with a synchronous interface (all signals are registered on the positive edge of the clock signal CK). Read and write accesses to SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0–A11 select the device row for 64MB ; A0–A12 for 128MB). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

SDRAM modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed device row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the device column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing the alternate device bank will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between device banks in order to hide precharge time, and the capability to randomly change device column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb and 256Mb SDRAM data sheets.

Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, Command Inhibit or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one Command Inhibit or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all device banks idle state.

Once in the idle state, two AUTO refresh cycles must be performed. After the AUTO refresh cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 4, Mode Register Definition Diagram, on page 7. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Figure 7, Burst Definition Table, on page 8. The block is uniquely selected by A1–A8 when the burst length is set to two; A2–A8 when the burst length is set to four; and by A3–A8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Figure 7, Burst Definition Table, on page 8.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Figure 7, Burst Definition Table, on page 8.

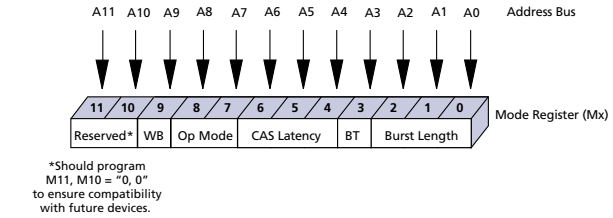
CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

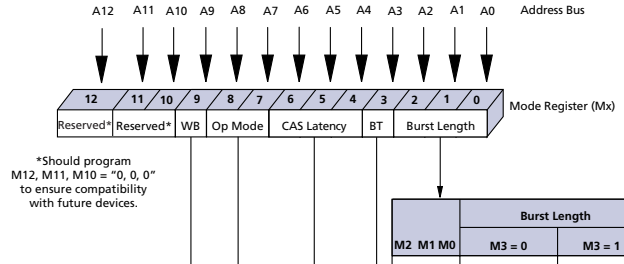
If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQ will start driving as a result of the clock edge one cycle earlier ($n + m$ - 1), and provided that the relevant access times are met, the data will be valid by clock edge $n + m$.

Figure 4: Mode Register Definition Diagram

64MB Module



128MB Module



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Table 7: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0–A8 (location 0-y)			Cn, Cn+1, Cn+2 Cn+3, Cn+4… …Cn-1, Cn…	Not supported

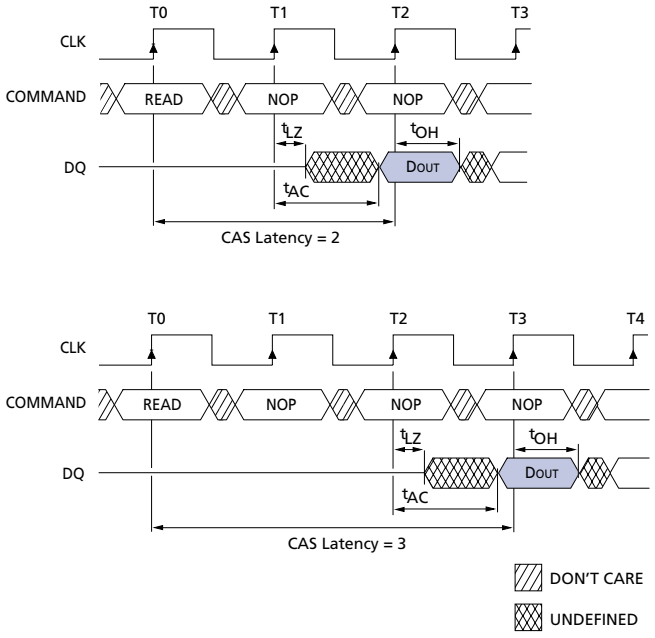
NOTE:

1. For full-page accesses: y = 512
2. For a burst length of two, A1–A8 select the block of two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A8 select the block of four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A8 select the block of eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A8 select the unique column to be accessed, and Mode Register bit M3 is ignored.

Table 8: CAS Latency Table

SPEED	ALLOWABLE OPERATING FREQUENCY (MHZ)	
	CAS LATENCY = 2	CAS LATENCY = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133
-10E	≤ 100	N/A

Figure 5: CAS Latency Diagram



For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0 and the latency is programmed to two clocks, the DQ will start driving after T1 and the data will be valid by T2, as shown in Figure 5, CAS Latency Diagram. Table 8, CAS Latency Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0–M2 applies to both read and write bursts; when M9 = 1, the programmed burst length applies to read bursts, but write accesses are single-location (nonburst) accesses.

Commands

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of commands and operations refer to the 128Mb or 256Mb SDRAM datasheets.

Table 9: Truth Table – SDRAM Commands and DQMB Operation

CKE is HIGH for all commands shown except Self Refresh

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQS	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	1
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	2
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	2
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	3
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	4, 5
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	6
Write Enable/Output Enable	–	–	–	–	L	–	Active	7
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	7

NOTE:

1. A0–A11 (64MB), A0–A12 (128MB) provide device row address. BA0, BA1 determine which device bank is made active.
2. A0–A8 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
3. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0, BA1 are "Don't Care."
4. This command is Auto Refresh if CKE is HIGH, Self Refresh if CKE is LOW.
5. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
6. A0–A11 (64MB), A0–A12 (128MB) define the op-code written to the Mode Register, and should be driven low.
7. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on V_{DD}, $V_{DD}Q$ Supply Relative to V_{SS} . . . . . -1V to +4.6V
Voltage on Inputs, NC or I/O Pins Relative to V_{SS} . . . . . -1V to +4.6V

Operating Temperature, T_A . . . . . 0°C to +70°C
Storage Temperature (plastic) . . . . . -55°C to +150°C
Power Dissipation 4W

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1, 5, 6; notes appear on page 14; V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}, $V_{DD}Q$	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-20	20	µA	
OUTPUT LEAKAGE CURRENT: DQ pins are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

Table 11: I_{DD} Specifications and Conditions – 64MB

DRAM components only;
Notes: 1, 6, 11 , 13; notes appear on page 14; V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		SYMBOL	-13E	-133	-10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN)		I_{DD1}	640	600	560	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device banks idle; CKE = LOW		I_{DD2}	8	8	8	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after ^tRCD met; No accesses in progress		I_{DD3}	200	200	160	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		I_{DD4}	660	600	560	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	^tRFC = ^tRFC (MIN)	I_{DD5}	1,320	1,240	1,080	mA	3, 12,
	^tRFC = 15.6 µs	I_{DD6}	12	12	12	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD7}	8	8	8	mA	4
	Low Power	I_{DD7}	4	4	4	mA	

Table 12: IDD Specifications and Conditions – 128MB

DRAM components only;
Notes: 1, 6, 11 , 13; notes appear on page 14; VDD, VDDQ = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		**SYMBOL**	**-13E**	**-133**	**-10E**	**UNITS**	**NOTES**
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		IDD1	540	500	500	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; All device banks idle; CKE = LOW		IDD2	8	8	8	mA	30
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All device banks active after ^{t}RCD met; No accesses in progress		IDD3	160	160	160	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All device banks active		IDD4	540	540	540	mA	3, 18, 19, 30
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	^{t}RFC = ^{t}RFC (MIN)	IDD5	1,140	1,080	1,080	mA	3, 12,
	^{t}RFC = 7.81µs	IDD6	14	14	14	mA	18, 19, 30, 31
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD7	10	10	10	mA	4
	Low Power	IDD7	6	6	6	mA	

Table 13: Capacitance

Notes: 2; notes appear on page 14

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: A0–A12, BA0, BA1, RAS#, CAS#, WE#, S#, CKE	CI1	10	15.2	pF
Input Capacitance: CK	CI2	10	14	pF
Input Capacitance: DQMB0–DQMB7	CI5	2.5	3.8	pF
Input/Output Capacitance: SCL, SA0–SA2, SDA	CI6	–	10	pF
Input/Output Capacitance: DQ0–DQ63	CIO	4	6	pF

Table 14: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 5, 6, 8, 9, 11; notes appear on page 14; Module AC timing parameters comply with PC133 Design Specs, based on component parameters

AC CHARACTERISTICS			-13E		-133		-10E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	$^tAC(3)$		5.4		5.4		6	ns	27
	CL = 2	$^tAC(2)$		5.4		6		6	ns	
Address hold time		^tAH	0.8		0.8		1		ns	
Address setup time		^tAS	1.5		1.5		2		ns	
CLK high-level width		^tCH	2.5		2.5		3		ns	
CLK low-level width		^tCL	2.5		2.5		3		ns	
Clock cycle time	CL = 3	$^tCK(3)$	7		7.5		8		ns	23
	CL = 2	$^tCK(2)$	7.5		10		10		ns	23
CKE hold time		^tCKH	0.8		0.8		1		ns	
CKE setup time		^tCKS	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		2		ns	
Data-in hold time		^tDH	0.8		0.8		1		ns	
Data-in setup time		^tDS	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	$^tHZ(3)$		5.4		5.4		6	ns	10
	CL = 2 (64MB)	$^tHZ(2)$		5.4		6		6	ns	10
	CL = 2 (128MB)	$^tHZ(2)$		5.4		6		7	ns	10
Data-out low-impedance time		^tLZ	1		1		1		ns	
Data-out hold time (load)		^tOH	3		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		^tRAS	37	120,000	44	120,000	50	120,000	ns	29
ACTIVE to ACTIVE command period		^tRC	60		66		70		ns	
ACTIVE to READ or WRITE delay		^tRCD	15		20		20		ns	
Refresh period		^tREF		64		64		64	ms	
AUTO REFRESH period		^tRFC	66		66		70		ns	
PRECHARGE command period		^tRP	15		20		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		ns	24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		^tXSR	67		75		80		ns	20

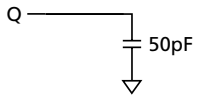
Table 15: AC Functional Characteristics

Notes: 5, 6, 7, 8, 9, 11; notes appear on page 14

PARAMETER		SYMBOL	-13E	-133	-10E	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		$^{t}CKED$	1	1	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	0	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	0	0	^{t}CK	17
DQM to data high-impedance during READs		^{t}DQZ	2	2	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	0	0	^{t}CK	17
Data-in to ACTIVE command		^{t}DAL	4	5	4	^{t}CK	15, 21
Data-in to PRECHARGE command		^{t}DPL	2	2	2	^{t}CK	16, 21
Last data-in to burst STOP command		^{t}BDL	1	1	1	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	1	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	2	2	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	2	^{t}CK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	$^{t}ROH(3)$	3	3	3	^{t}CK	17
	CL = 2	$^{t}ROH(2)$	2	2	2	^{t}CK	17

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T_A ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO Refresh commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO Refresh command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10E, and ^{t}CK = 7.5ns for -133 and -13E.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. The value of ^{t}RAS in -13E speed grade module SPDs is calculated from ^{t}RC - ^{t}RP = 45ns.
30. For -10E, CL = 2 and ^{t}CK = 10ns; for -133, CL = 3 and ^{t}CK = 7.5ns; for -13E, CL = 2 and ^{t}CK = 7.5ns.
31. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD}6 limit is actually a nominal value and does not result in a fail value.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 6, Data Validity, and Figure 7, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors

the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 8, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledgeis not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 6: Data Validity

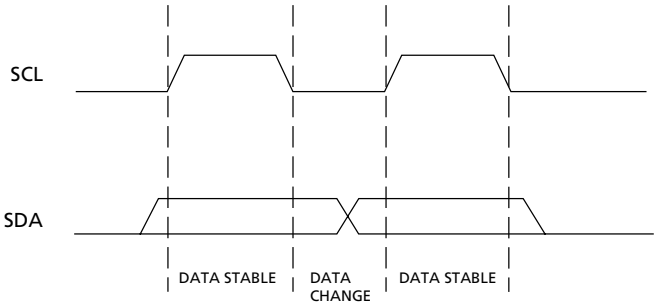


Figure 7: Definition of Start and Stop

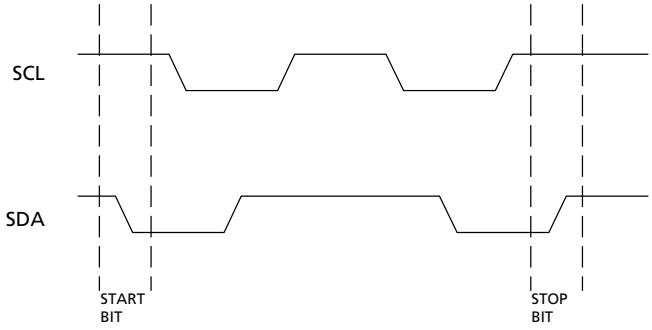


Figure 8: Acknowledge Response from Receiver

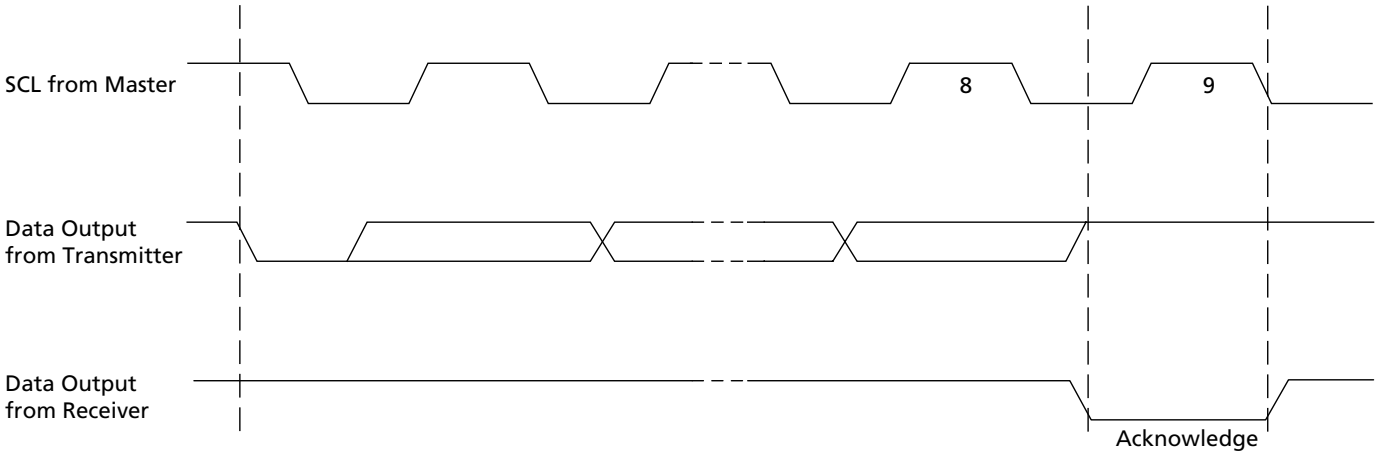


Table 16: EEPROM Device Select Code

The most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	$\overline{RW}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	$\overline{RW}$

Table 17: EEPROM Operating Modes

MODE	$\overline{RW}$ BIT	$\overline{WC}$	BYTES	INITIAL SEQUENCE
Current Address Read	1	V_{IH} or V_{IL}	1	Start, Device Select, $\overline{RW}$ = 1
Random Address Read	0	V_{IH} or V_{IL}	1	Start, Device Select, $\overline{RW}$ = 0, Address
	1	V_{IH} or V_{IL}		reSTART, Device Select, $\overline{RW}$ = 1
Sequential Read	1	V_{IH} or V_{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $\overline{RW}$ = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, $\overline{RW}$ = 0

Figure 9: SPD EEPROM Timing Diagram

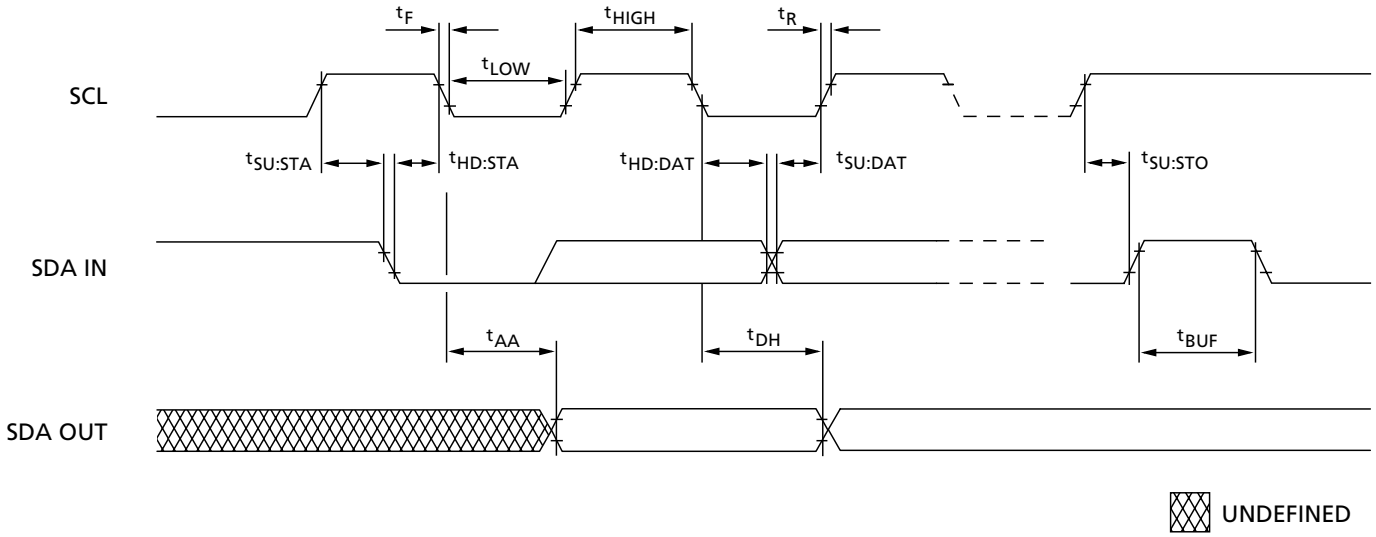


Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{DD} or V_{SS}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

NOTE:

1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 20: Serial Presence-Detect Matrix

1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT864W	MT4LSDT1664W
0	Number of Bytes Used by Micron	128	80	80
1	Total Number of SPD Memory Bytes	256	08	08
2	Memory Type	SDRAM	04	04
3	Number of Row Addresses	12 or 13	0C	0D
4	Number of Column Addresses	9	09	09
5	Number of Module Banks	1	01	01
6	Module Data Width	64	40	40
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	LVTTL	01	01
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 3)	7ns (-13E) 7.5ns (-133) 8ns (-10E)	70 75 80	70 75 80
10	SDRAM Access from CLK, ^{t}AC (CAS Latency = 3)	5.4ns (-13E/-133) 6ns (-10E)	54 60	54 60
11	Module Configuration Type	NONPARITY	00	00
12	Refresh Rate/Type	15.6µs or 7.81µs/ SELF	80	82
13	Sdram Width (Primary SDRAM)	16	10	10
14	Error-checking Sdram Data Width	NONE	00	00
15	Minimum Clock Delay from Back-to-Back Random Column Addresses, ^{t}CCD	1	01	01
16	Burst Lengths Supported	1, 2, 4, 8, PAGE	8F	8F
17	Number of Banks on SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 3	06	06
19	CS Latency	0	01	01
20	WE Latency	0	01	01
21	SDRAM Module Attributes	UNBUFFERED	00	00
22	SDRAM Device Attributes: General	0E	0E	0E
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	7.5ns (13E) 10ns (-133/-10E)	75 A0	75 A0
24	SDRAM Access from CLK, ^{t}AC (CAS Latency = 2)	5.4ns (-13E) 6ns (-133/-10E)	54 60	54 60
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1)		00	00
26	SDRAM Access from CLK, ^{t}AC (CAS Latency = 1)		00	00
27	Minimum Row Precharge Time, ^{t}RP	15ns (-13E) 20ns (-133/-10E)	0F 14	0F 14
28	Minimum Row Active to Row Active, ^{t}RRD	14ns (-13E) 15ns (-133) 20ns (-10E)	0E 0F 14	0E 0F 14
29	Minimum RAS# to CAS# Delay, ^{t}RCD	15ns (-13E) 20ns (-133/-10E)	0F 14	0F 14
30	Minimum RAS# Pulse Width, ^{t}RAS (See note 1)	45ns (-13E) 44ns (133) 50ns (-10E)	2D 2C 32	2D 2C 32
31	Module Rank Density	64MB or 128MB	10	20

Table 20: Serial Presence-Detect Matrix

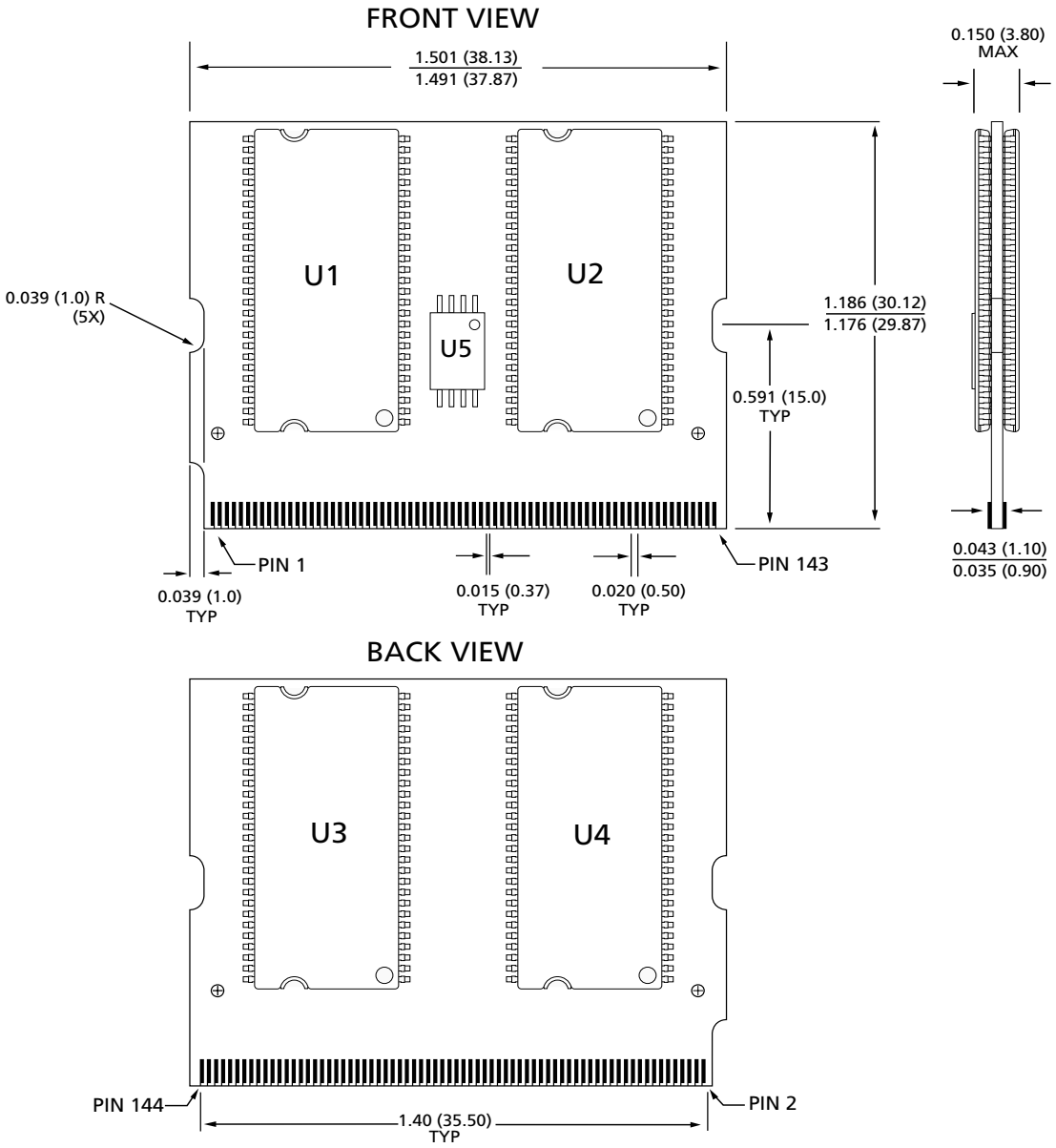
1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT864W	MT4LSDT1664W
32	Command and Address Setup Time, ^{t}AS, ^{t}CMS	1.5ns (-13E/-133) 2ns (-10E)	15 20	15 20
33	Command and Address Hold Time, ^{t}AH, ^{t}CMH	0.8ns (-13E/-133) 1ns (-10E)	08 10	08 10
34	Data Signal Input Setup Time, ^{t}DS	1.5ns (-13E/-133) 2ns (-10E)	15 20	15 20
35	Data Signal Input Hold Time, ^{t}DH	0.8ns (-13E/-133) 1ns (-10E)	08 10	08 10
36-61	Reserved		00	00
62	SPD Revision	REV. 1.2	12	12
63	Checksum for Bytes 0-62	(-13E) (-133) (-10E)	5F A5 ED	72 B8 00
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code (Cont.)		FF	FF
72	Manufacturing Location	1–12	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code		Variable Data	Variable Data
92	Identification Code (Cont.)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-125	Manufacturer-Specific Data (Rsvd)			
126	System Frequency	100 MHz (-13E/-133/-10E)	64	64
127	SDRAM Component & Clock Detail		8F	8F

NOTE:

1. The value of ^{t}RAS used for -13E modules is calculated from ^{t}RC - ^{t}RP. Actual device spec. value is 37ns.

Figure 10: 144-Pin MicroDIMM Dimensions



Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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