1.0 SCOPE

This specification covers the detail requirements for a 12-bit monolithic multiplying CMOS digital-to-analog converter for use with 8-bit bus microprocessors. Data is loaded in two bytes, 8 + 4 bits (high/low byte), to input holding registers. The complete word is then transferred into the DAC register to update the DAC.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number. The complete part numbers per Table I of this specification follow:

Device	Part Number	Package
A	PM-7548AR/883	R
B	PM-7548BR/883	R
B	PM-7548BRC/883	RC*

*Future product, contact PMI Sales for present availability.

1.2.3 Case Outline.

Letter	Case Outline (Lead finish per MIL-M-38510)
R	20-lead ceramic dual-in-line package (CERDIP)
RC	20-contact hermetic leadless chip carrier (LCC)

1.3 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{DD} to DGND ..... -0.3V, +17V
V_{REF} to DGND ..... ±25V
V_{RFB} to DGND ..... ±25V
AGND to DGND ..... -0.3V, V_{DD}
Digital Input Voltage Range to DGND ..... GND, V_{DD}
Output Voltage (pin 1) to AGND ..... -0.3V, V_{DD}
Power Dissipation (any package) to +75°C 450mW
Derate above 75°C by ..... 6mW/°C
Operating Temperature Range ..... -55°C to +125°C
DICE Junction Temperature (T_J) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

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1.5 Thermal Characteristics:

Thermal Resistance, CERDIP (R) package:

Junction-to-Case (Θ_{JC}) = 35°C/W MAX

Junction-to-Ambient (Θ_{JA}) = 120°C/W MAX

Thermal Resistance, LCC (RC) package:

Junction-to-Case (Θ_{JC}) = 35°C/W MAX

Junction-to-Ambient (Θ_{JA}) = 110°C/W MAX

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TABLE 1

V_{REF} = +10V; V_{OUT} = AGND = 0V; V_{DD} = +5V or +15V; T_A = 25°C unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7548/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Relative Accuracy	INL	-55°C ≤ T_A ≤ +125°C	--	±1/2	--	±1/2	LSB
Differential Nonlinearity	DNL	-55°C ≤ T_A ≤ +125°C	--	±1/2	--	±1	LSB
Gain Error	G_{FSE}		--	±1	--	±2	LSB
		-55°C ≤ T_A ≤ +125°C	--	±2	--	±3	LSB
DC Power Supply Rejection Ratio $\Delta Gain/\Delta V_{DD}$ (Note 1)	PSRR		--	±0.001	--	±0.001	%/%
		-55°C ≤ T_A ≤ +125°C	--	±0.002	--	±0.002	%/%
Output Leakage Current I_{OUT} (Note 2)	I_{LKG}		--	±5	--	±5	nA
		-55°C ≤ T_A ≤ +125°C	--	±100	--	±100	nA
Input Resistance	R_{REF}	-55°C ≤ T_A ≤ +125°C	7	15	7	15	kΩ
Digital Input High	V_{IH}	-55°C ≤ T_A ≤ +125°C	2.4	--	2.4	-	V
Digital Input Low	V_{IL}	-55°C ≤ T_A ≤ +125°C	--	0.8	--	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD} -55°C ≤ T_A ≤ +125°C	--	±1	--	±1	µA
Supply Current	I_{DD}	Digital Inputs = V_{IL} or V_{IH} -55°C ≤ T_A ≤ +125°C	--	3.0	--	3.0	mA
		Digital Inputs = 0V or V_{DD} -55°C ≤ T_A ≤ +125°C	--	1.0	--	1.0	mA
$\overline{WR}$ Pulse Width	t_{WR}		120	--	120	--	ns

TABLE 1

V_{REF} = +10V; V_{OUT} = AGND = 0V; V_{DD} = +5V or +15V; T_A = 25°C unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7548/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Data Valid to $\overline{WR}$ Set-up Time	t_{DS}		160	--	160	--	ns
Data Valid to $\overline{WR}$ Hold Time	t_{DH}		10	--	10	--	ns
$\overline{CSMSB}$/$\overline{CSLSB}$ to $\overline{WR}$ Set-up Time	t_{CWS}		0	--	0	--	ns
$\overline{CSMSB}$/$\overline{CSLSB}$ to $\overline{WR}$ Hold Time	t_{CWH}		0	--	0	--	ns
$\overline{LDAC}$ to $\overline{WR}$ Set-up Time	t_{LWS}		0	--	0	--	ns
$\overline{LDAC}$ to $\overline{WR}$ Hold Time	t_{LWH}		0	--	0	--	ns

NOTES:
1. ΔV_{DD} = ±5%
2. DAC loaded with 0000 0000 0000

TABLE 2

PM-7548/883

Electrical Test Requirements For Class B Devices

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3, 9

* PDA applies to Subgroup 1 only.
No other Subgroups are included in PDA.

TABLE 3

Group A Inspection

V_{REF} = +10V; V_{OUT} = AGND = 0V; V_{DD} = +5V or +15V unless otherwise specified.

			PM-7548/883				
			LIMITS A		LIMITS B		
Subgroup	Symbol	Special Conditions	Min	Max	Min	Max	Units
Subgroup 1	INL		--	±1/2	--	±1/2	LSB
T_A = +25°C	DNL		--	±1/2	--	±1	LSB
	G_{FSE}		--	±1	--	±2	LSB
	PSRR	(Note 1)	--	±0.001	--	±0.001	%/%
	I_{LKG}	(Note 2)	--	±5	--	±5	nA
	R_{REF}		7	15	7	15	kΩ
	V_{IH}		2.4	--	2.4	--	V
	V_{IL}		--	0.8	--	0.8	V
	I_{IN}	V_{IN} = 0V or V_{DD}	--	±1	--	±1	µA
	I_{DD}	V_{DD} = +5V Digital Inputs = V_{IL} or V_{IH}	--	2.0	--	2.0	mA
		V_{DD} = +5V Digital Inputs = 0V or V_{DD}	--	0.3	--	0.3	mA
		V_{DD} = +15V Digital Inputs = V_{IL} or V_{IH}	--	3.0	--	3.0	mA
		V_{DD} = +15V Digital Inputs = 0V or V_{DD}	--	1.0	--	1.0	mA
Subgroup 2	INL		--	±1/2	--	±1/2	LSB
T_A = +125°C	DNL		--	±1/2	--	±1	LSB
	G_{FSE}		--	±2	--	±3	LSB
	PSRR	(Note 1)	--	±0.002	--	±0.002	%/%
	I_{LKG}	(Note 2)	--	±100	--	±100	nA

TABLE 3

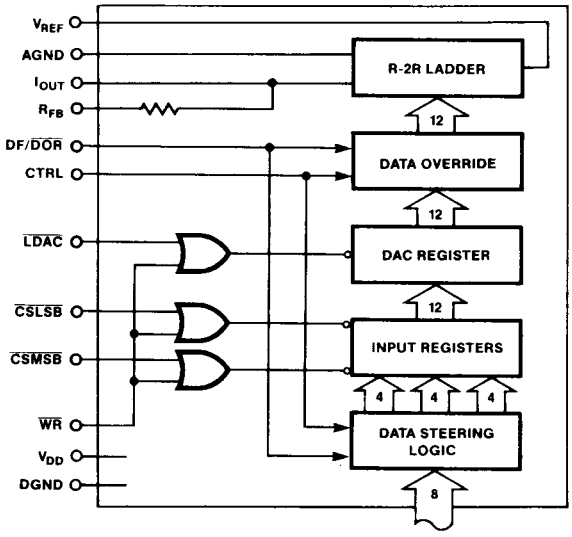
Group A Inspection

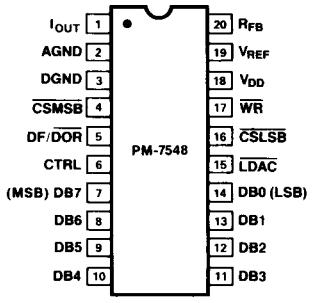
V_{REF} = +10V; V_{OUT} = AGND = 0V; V_{DD} = +5V or +15V unless otherwise specified.

Subgroup	Symbol	Special Conditions	PM-7548/883 LIMITS A Min	LIMITS A Max	LIMITS B Min	LIMITS B Max	Units
Subgroup 2	R_{REF}		7	15	7	15	kΩ
T_A = +125°C	V_{IH}		2.4	--	2.4	--	V
(Continued)	V_{IL}		--	0.8	--	0.8	V
	I_{IN}	V_{IN} = 0V or V_{DD}	--	±1	--	±1	µA
	I_{DD}	V_{DD} = +5V Digital Inputs = V_{IL} or V_{IH}	--	2.0	--	2.0	mA
		V_{DD} = +5V Digital Inputs = 0V or V_{DD}	--	0.3	--	0.3	mA
		V_{DD} = +15V Digital Inputs = V_{IL} or V_{IH}	--	3.0	--	3.0	mA
		V_{DD} = +15V Digital Inputs = 0V or V_{DD}	--	1.0	--	1.0	mA
Subgroup 3 T_A = -55°C		All Tests, Limits and Conditions are the same as for Subgroup 2.					
Subgroup 9	t_{WR}		120	--	120	--	ns
T_A = +25°C	t_{DS}		160	--	160	--	ns
	t_{DH}		10	--	10	--	ns
	t_{CWS}		0	--	0	--	ns
	t_{CWH}		0	--	0	--	ns
	t_{LWS}		0	--	0	--	ns
	t_{LWH}		0	--	0	--	ns

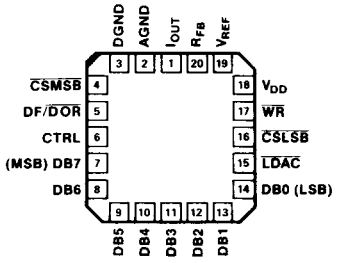
NOTES:
1. ΔV_{DD} = ±5%
2. DAC loaded with 0000 0000 0000

3.2.1 Functional Diagram and Pin Connections.





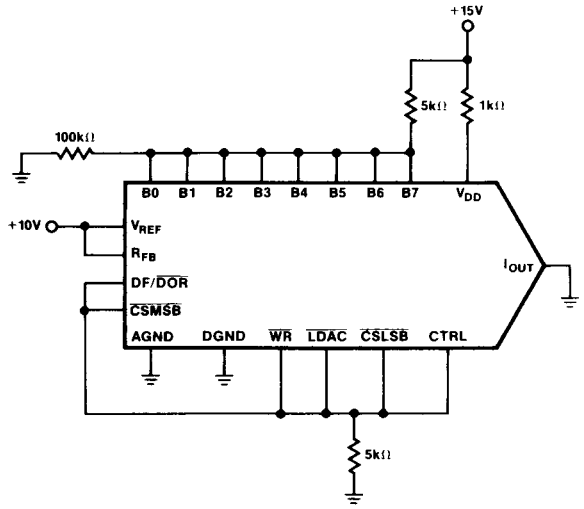
20-PIN HERMETIC DIP
(R-Suffix)



PM-7548BRC
20-PIN LCC
(RC-Suffix)

3.2.4 Microcircuit Group Assignment. This microcircuit is covered by microcircuit group 80.

4.2 Life Test/Burn-In Circuit.



Interface Input Description

$\overline{\text{CSMSB}}$ (Pin 4) - Chip Select Most Significant Byte. Active Low. Selected either with $\overline{\text{WR}}$, to load most significant byte data into the input register, or with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ to load data into both input and DAC registers.

$\overline{\text{CSLSB}}$ (Pin 16) - Chip Select Least Significant Byte. Active Low. Selected either with $\overline{\text{WR}}$ to load least significant byte data into the input register, or with $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ to load data into both input and DAC registers.

DF/$\overline{\text{DOR}}$ (Pin 5) - Data Format/Data Override. When LOW, DAC is forced to full-scale or zero-scale output as selected by CTRL. Use of Data Override does not affect data held in DAC register. When DF/$\overline{\text{DOR}}$ is HIGH, CTRL selects either right or left data input format. DF/$\overline{\text{DOR}}$ is normally held HIGH.

DF/$\overline{\text{DOR}}$	CTRL	Function
0	0	DAC forced to zero-scale (all zeros)
0	1	DAC forced to full-scale (all ones)
1	0	Left-justified data format selected
1	1	Right-justified data format selected

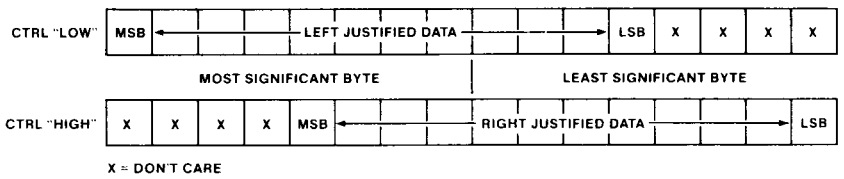
$\overline{\text{LDAC}}$ (Pin 15) - Load DAC Input. Active Low. Selected, with other interface inputs, to load DAC register from input register or external data bus.

$\overline{\text{WR}}$ (Pin 17) - Write Input. Active Low. Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

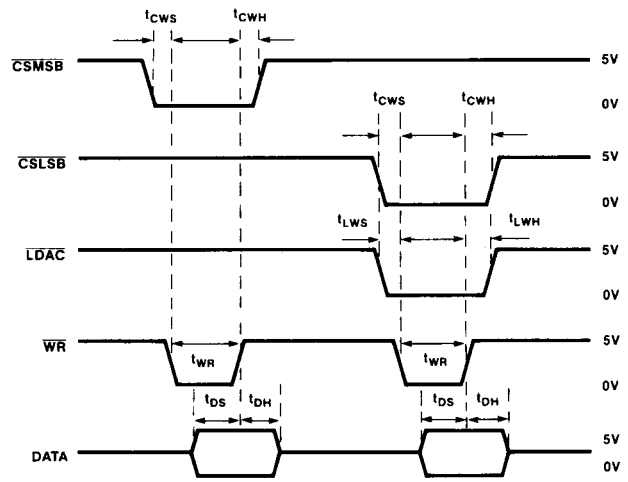
$\overline{\text{WR}}$	$\overline{\text{CSMSB}}$	$\overline{\text{CSLSB}}$	$\overline{\text{LDAC}}$	Function
0	1	0	1	Load LSByte to Input Register
0	1	0	0	Load LSByte to Input and DAC Registers
0	0	1	1	Load MSByte to Input Register
0	0	1	0	Load MSByte to Input and DAC Registers
0	1	1	0	Load Input Register to DAC Register
1	X	X	X	No Data Transfer

Input Control Information

CTRL (Pin 6) - Control Input (Refer also to DF/$\overline{\text{DOR}}$)



X = DON'T CARE



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. $\overline{\text{CSMSB}}$ (PIN 4) AND $\overline{\text{CSLSB}}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{\text{DOR}}$ = +5V.
   FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{\text{DOR}}$ = +5V.