SED1526 Series

DOT MATRIX LCD DRIVER-CONTROLLER

■ DESCRIPTION

The SED1526 Series are intelligent CMOS LCD controller-drivers with the ability to drive alphanumeric and graphic displays. The LSI communicates with a high-speed microprocessor, such as the Intel 80xx and 68xx family, through either a serial or 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (80 × 33 bits) and generates an LCD drive signal.

These devices incorporate an internal DC/DC converter to generate the negative voltage needed for the LCD contrast. The controller features software contrast adjusted by command setting.

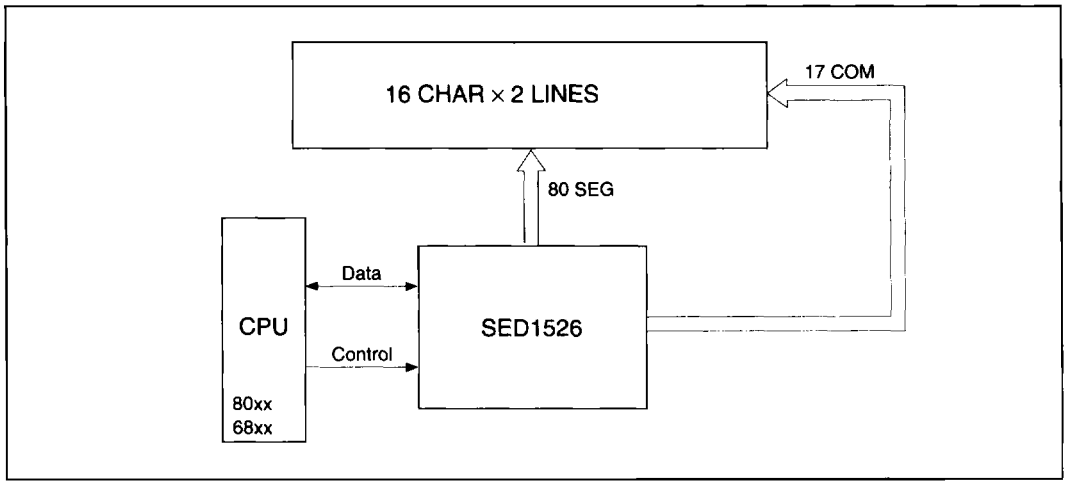
■ FEATURES

- Low-power CMOS technology
- Direct interface to both 80xx and 68xx MPU
- Support 8-bit parallel and serial interface
- On-chip display data RAM ..... 80 × 33 bits
- On-chip DC/DC converter for LCD voltage
- On-chip CR oscillator circuit
- Supports master/slave mode
- Voltage regulator, low-power voltage follower
- –.17%/°C temperature gradient
- 32-level contrast adjustment by software
- 2.4V to 6.0V supply voltage
- –4.0V to –12V LCD voltage
- Operating temperature ..... –40 to 85°C
- Low power consumption 100µA
- Package
  - QFP-5 ..... 128-pin (F0A)
  - Al pad Die D0A
  - Au bump Die D0B
  - TAB T0A

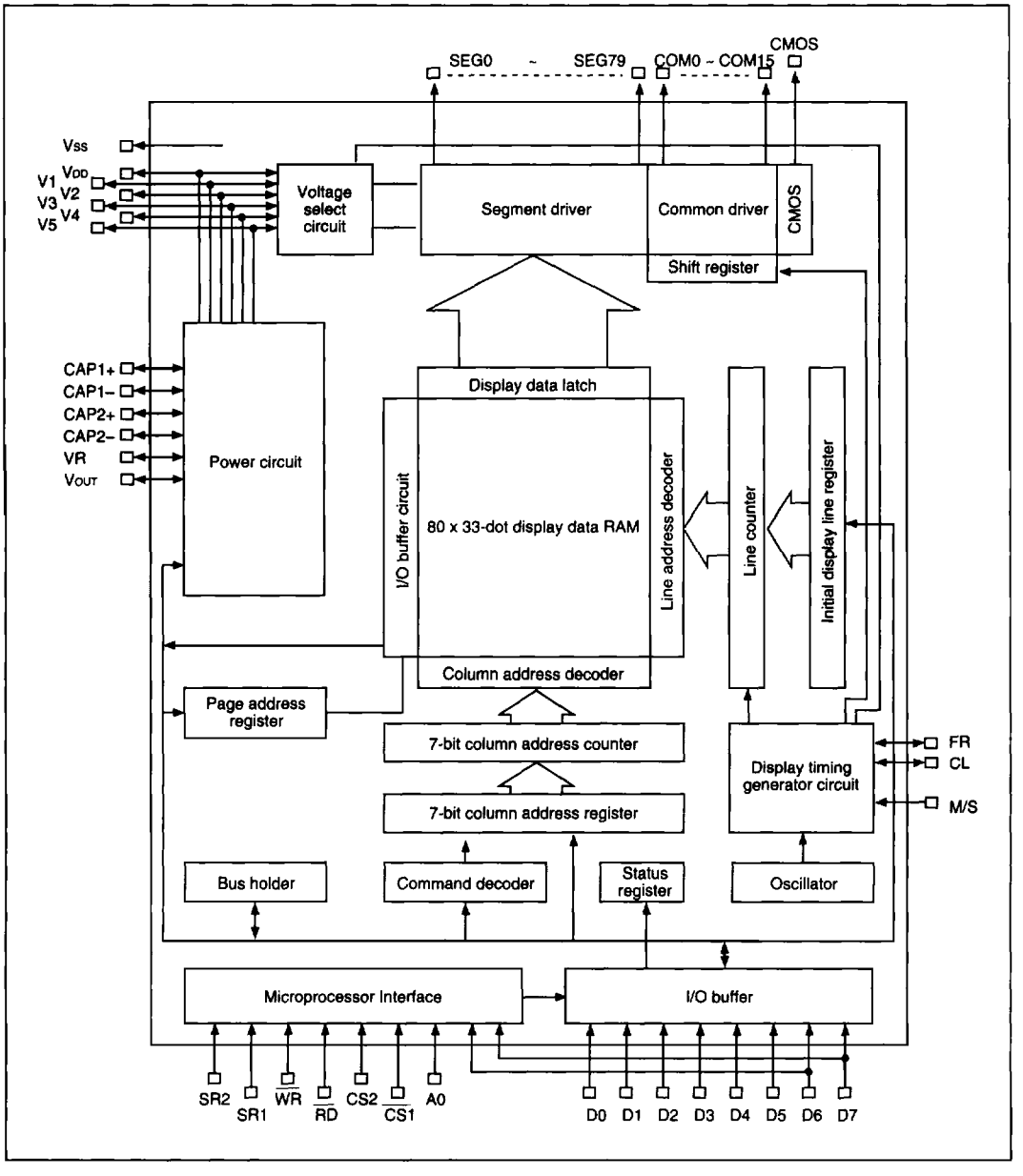
Available models

Models	Duty Cycle	LCD Bias	SEG Driver	COM Driver	Display Area
SED1526	1/8, 1/9, 1/16, 1/17	1/5	80	17	80 × 17
SED1527	1/16, 1/17, 1/32, 1/33	1/7	80	17	160 × 33
SED1528	1/32, 1/33	1/7	64	33	64 × 33

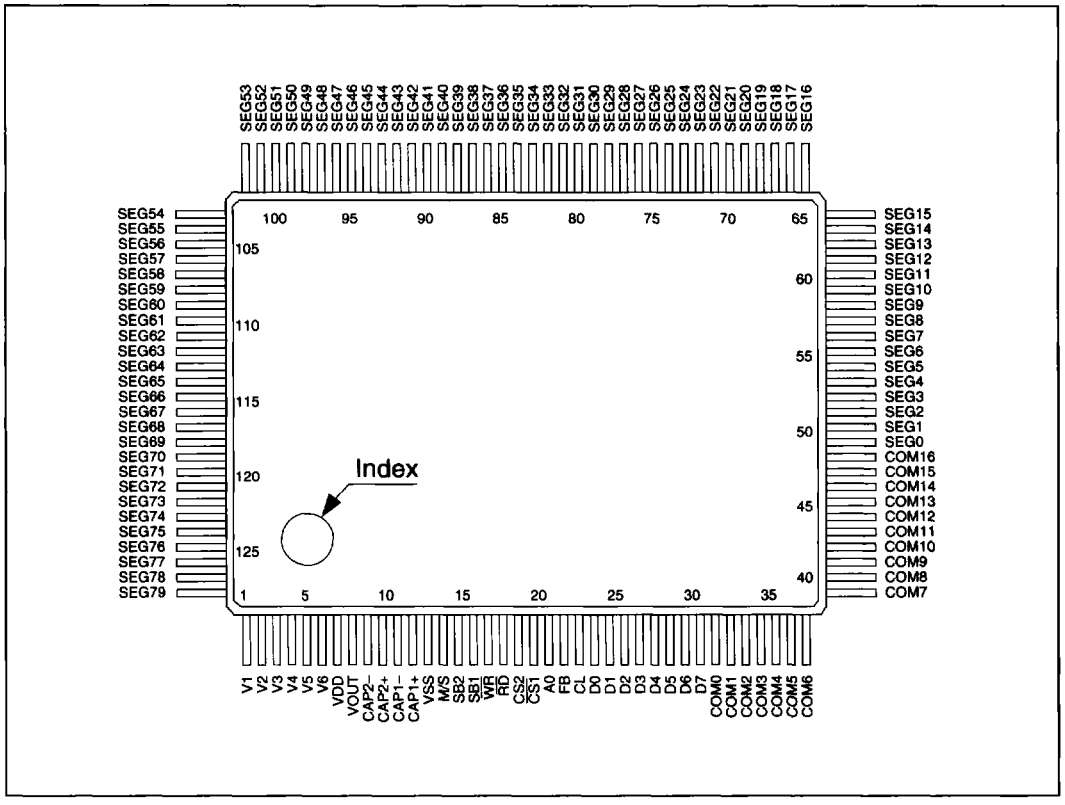
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ SED1526 AND SED1527 PIN ASSIGNMENT



■ PIN DESCRIPTION

● Power Supply

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>VDD</td><td>Supply</td><td>+5V power supply. Common to microprocessor power supply VCC pin.</td><td>1</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td><td>1</td></tr>
<tr><td>V1 ~ V5</td><td>Supply</td><td>LCD driver supply voltages. The Set Power Control command can switch the master (internal) and external power supply modes of these pins. When external mode selects, the voltage determined by the LCD cell is impedance-converted through a resistive divider or an operational amplifier depending on application. Voltages should meet the following requirement:
VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5
When master mode selects, these voltages are generated on the chip:
<table>
<tr><th></th><th>SED1526</th><th>SED1527</th><th>SED1528</th></tr>
<tr><td>V1</td><td>1/5 V5</td><td>1/7 V5</td><td>1/7 V5</td></tr>
<tr><td>V2</td><td>2/5 V5</td><td>2/7 V5</td><td>2/7 V5</td></tr>
<tr><td>V3</td><td>3/5 V5</td><td>5/7 V5</td><td>5/7 V5</td></tr>
<tr><td>V4</td><td>4/5 V5</td><td>6/7 V5</td><td>6/7 V5</td></tr>
</table>
</td><td>5</td></tr>
</table>

● LCD Driver Supplies

Pin	I/O	Function	Number of Pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
VOUT	O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between VDD and V5 using a resistive divider.	1

● **Microprocessor Interface**

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Number of Pins</th></tr>
<tr><td>D0 ~ D7
(SI)
(SCL)</td><td>I/O</td><td>Data input/outputs. The 8-bit bidirectional data buses to be connected to the standard 4/8-bit microprocessor data buses. When the serial interface is selected, D7 is serial data input (SI) and D6 is serial clock input (SCL).</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Control/display data flag is input. It is connected to the LSB of microprocessor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip select input. Data input/output is enabled when $\overline{CS1}$ is low and CS2 is high.</td><td>2</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>• Read enable input. When interfacing to an 8080-Series microprocessor and when $\overline{RD}$ is low, the SED1526 Series data bus output is enabled.
• When interfacing to a 6800-Series microprocessor and when R/W Enable E is high, R/$\overline{W}$ input is enabled.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td></td><td>• Write enable input. When interfacing to an 8080-Series microprocessor, $\overline{WR}$ is active low.
• When interfacing to a 6800-Series microprocessor, it will be in read mode when R/$\overline{W}$ is high and it will be in write mode when R/$\overline{W}$ is low.
R/$\overline{W}$ = "1" : Read
R/$\overline{W}$ = "0" : Write</td><td>1</td></tr>
<tr><td>SR1, SR2</td><td>I</td><td>Microprocessor interface select, and parallel/serial data input select.
<table>
<tr><th>SR1</th><th>SR2</th><th>Type</th></tr>
<tr><td>0</td><td>1</td><td>8080 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>1</td><td>6800 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>0</td><td>Serial input</td></tr>
<tr><td>0</td><td>0</td><td>Reset</td></tr>
</table>
* In serial mode, no data can be read from RAM and D0 to D5 are HZ. $\overline{RD}$ and $\overline{WR}$ must be high or low.</td><td>2</td></tr>
</table>

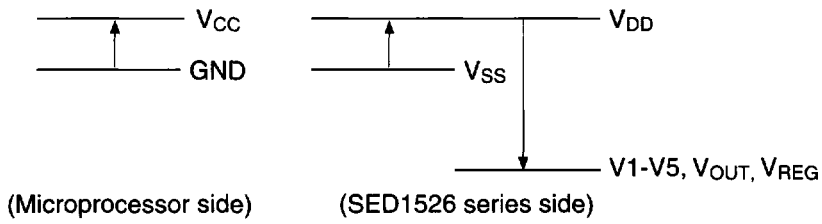
- **LCD Driver Outputs**

<table>
<tr><th>Pin</th><th>I/O</th><th>Functions</th><th>Number of Pins</th></tr>
<tr><td>M/S</td><td>I</td><td>SED1526 Series master/slave mode select input. Master mode selects when FR and CL are high, and slave mode selects when FR and CL are low. It will be master mode when M/S is high and it will be slave mode when M/S is low.
<table>
<tr><th>Model</th><th>Mode</th><th>OSC Circuit</th><th>FR</th></tr>
<tr><td rowspan="2">SED1526
SED1527
SED1528</td><td>Master</td><td>Valid</td><td>Output</td></tr>
<tr><td>Slave</td><td>Invalid</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Clock input/ouput when SED1526 Series selects master or slave mode. The Clock Stop command can disable CL output when SED1526 Series is in master mode. It will be in ouput mode when M/S is high and it will be in input mode when M/S is low.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output. When SED1526 Series selects master mode, it must connect to LCD common driver FR pin. It will be output mode when M/S is high and it will be input mode when M/S is low.</td><td>1</td></tr>
<tr><td>SEGn</td><td>O</td><td>LCD segment driver output. The display RAM and FR signal select the segment driver output source.
<table>
<tr><th>RAM Data</th><th>FR Signal</th><th>Segment Driver-n Output</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_{DD}</td></tr>
<tr><td>0</td><td>V5</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V2</td></tr>
<tr><td>0</td><td>V3</td></tr>
</table></td><td>80 (SED1526/ 1527) or 64 (SED1528)</td></tr>
<tr><td>COMn</td><td>O</td><td>LCD common driver output. The IC internal scan signal and FR signal select the common driver output source. The common scan sequence is reversed in slave mode.
<table>
<tr><th>Internal Scan Signal</th><th>FR Signal</th><th>Common Driver-n Output</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V5</td></tr>
<tr><td>0</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V1</td></tr>
<tr><td>0</td><td>V4</td></tr>
</table></td><td>80 (SED1526/ 1527) or 32 (SED1528)</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. COMS pin is equivalent to following COM output pin when DUTY+1 command is running:
<table>
<tr><th></th><th colspan="2">SED1526</th><th colspan="2">SED1527</th><th>SED1528</th></tr>
<tr><th></th><th>1/9 duty</th><th>1/17 duty</th><th>1/17 duty</th><th>1/33 duty</th><th>1/33 duty</th></tr>
<tr><td>Indicator COMS output</td><td>COM8</td><td>COM16</td><td>COM16</td><td>COM16 of slave chip</td><td>COM32</td></tr>
</table></td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Condition	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	–0.3 to +6.0	
Driver supply voltage range (1)		V5	–18.0 to +0.3	V
Driver supply voltage range (2)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IH}	–0.3 to V_{DD} +0.3	V
Output voltage range		V0	–0.3 to V_{DD} + 0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature	Flat package	T_{STG}	–65 to +150	°C
	Bear chip		–55 to +125	
Soldering temperature and time		T_{SOLDER}	260 • 10 (at leads)	°C • sec



Notes:

1. V1 to V5, V_{OUT}, and V_{REG} voltages are based on V_{DD} = 0V.
2. Voltages VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during normal operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

● DC Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, T_a = −40 to 85°C unless otherwise noted

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Pin
Power voltage (1)	Operational	V_{DD}		2.4	—	6.0	V	V_{DD} *1
Operating voltage (2)	Operational	V5		−Vss × 3	—	−3.5	V	V5 *2
	Operational	V1, V2		0.6 × V5	—	V_{DD}	V	V1, V2
	Operational	V3, V4		V5	—	0.4 × V5	V	V3, V4
CMOS	High-level input voltage	V_{IHC}		0.7 × V_{DD}	—	V_{DD}	V	*3
			V_{DD} = 2.7V	0.8 × V_{DD}	—	V_{DD}		
	Low-level input voltage	V_{ILC}		Vss	—	0.3 × V_{DD}	V	*3
			V_{DD} = 2.7V	Vss	—	0.2 × V_{DD}		
	High-level output voltage	V_{OHC}	I_{OH} = −1mA	0.8 × V_{DD}	—	V_{DD}	V	*4
			V_{DD} = 2.7V I_{OH} = −0.5mA	0.8 × V_{DD}	—	V_{DD}		
	Low-level output voltage	V_{OLC}	I_{OH} = 1mA	Vss	—	0.2 × V_{DD}	V	*4
			V_{DD} = 2.7V I_{OL} = 0.5mA	Vss	—	0.2 × V_{DD}		
SCHMITT	High-level input voltage	V_{IHS}		0.4 × V_{DD}	—	0.8 × V_{DD}	V	*5
			V_{DD} = 2.7V	0.4 × V_{DD}	—	0.8 × V_{DD}		
	Low-level input voltage	V_{ILS}		0.2 × V_{DD}	—	0.6 × V_{DD}	V	*5
			V_{DD} = 2.7V	0.2 × V_{DD}	—	0.6 × V_{DD}		
	Schmitt voltage	V_H		0.2 × V_{DD}	—	—	V	*5
			V_{DD} = 2.7V	0.2 × V_{DD}	—	—		
Input leakage current		I_{LI}		−1.0	—	1.0	µA	*6
Output leakage current		I_{LO}		−3.0	—	3.0	µA	*7
LCD driver ON resistance		R_{ON}	T_a = 25°C V5 = −0.5V	—	5.0	7.5	kΩ	SEG0–79 COS0–15 COMS
			V5 = −3.5V	—	10.0	50.0		
Static current consumption		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}	—	0.05	3.0	µA	V_{DD}
Input pin capacity		C_{IN}	T_a = 25°C, f = 1MHz	—	5.0	8.0	pF	Input pins
Built-in Power Circuit	Input voltage	V_{DD}		2.4	—	6.0	V	
	Booster output voltage	V_{OUT}	Triple voltage conversion	−16.5	—	—	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}		−16.5	—	−4.0	V	V_{OUT}
	Voltage follower operation voltage	V5 (1)	Applied to SED1526	−12.0	—	−4.0	V	
		V5 (2)	Applied to SED1527	−16.0	—	(TBD)	V	
		V5 (3)	Applied to SED1528	−16.0	—	(TBD)	V	
	Reference voltage	V_{REG}	T_a = 25°C	−2.0	−3.1	−4.0	V	

*1. Although the wide range of operating voltage is guaranteed, a spike voltage change may have an effect on the voltage assurance during access to the microprocessor.

*2. VDD and V5 operating voltage range. The operating voltage range applies if an external power supply is used.

*3. Pins D0 to D5, A0, $\overline{CS1}$, CS2, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), M/S, CL and FR.

*4. Pins D0 to D7, FR and CL.

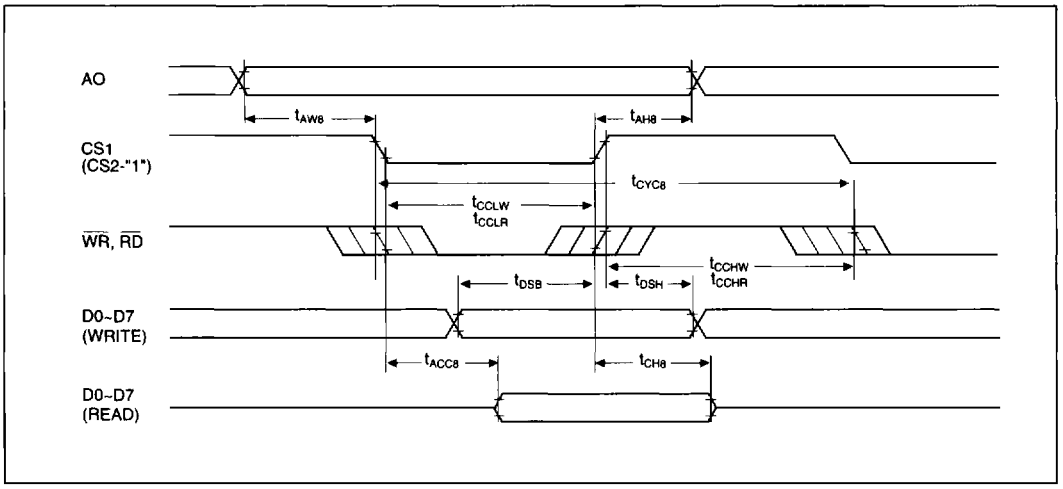
*5. Pins SI (D7), SCL (D5), SR1 and SR2.

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, SR1 and SR2.

*7. Applied if pins D0 to D7, FR and CL are high impedance.

- **Timing Characteristics**
  - **System Buses**

Read/write characteristics I (8080-Series microprocessor)



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		5	—	ns
Address setup time		t_{AW8}		5	—	ns
System cycle time		t_{CYC8}		250	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		75	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		75	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		145	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		145	—	ns
Data setup time		t_{DS5}		80	—	ns
Data hold time		t_{OH8}		10	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	80	ns
Output disable time		t_{CH8}		10	60	ns

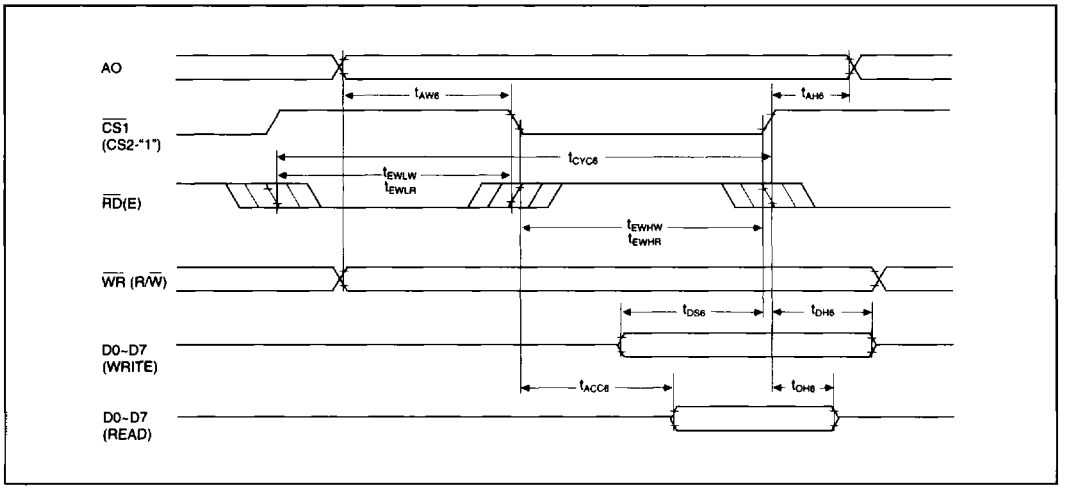
V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		500	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		185	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		185	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		285	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		285	—	ns
Data setup time		t_{DS5}		160	—	ns
Data hold time		t_{OH8}		20	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	180	ns
Output disable time		t_{CH8}		20	120	ns

Notes: 1. t_{CCLW} and t_{CCLR} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{WR}$ or $\overline{RD}$ low.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **System Buses**

Read/write characteristics II (6800-Series microprocessor)



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

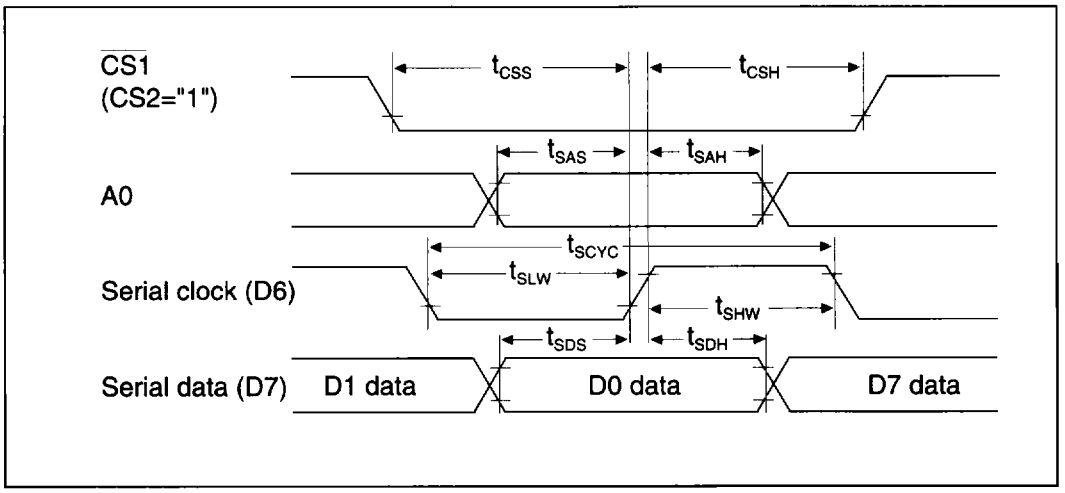
Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		A0	t_{CYC6}		250	—	ns
Address setup time		WR	t_{AW6}		20	—	ns
Address hold time		(R/W)	t_{AH6}		10	—	ns
Data setup time		D0 ~ D7	t_{DS6}		80	—	ns
Data hold time			t_{DH6}		10	—	ns
Output disable time			t_{OH6}	CL = 100pF	10	60	ns
Access time			t_{ACC6}		—	90	ns
Enable low pulse width	Read	RD (E)	t_{EWLR}		85	—	ns
	Write		t_{EWLW}		75	—	ns
Enable high pulse width	Read	RD (E)	t_{EWHR}		135	—	ns
	Write		t_{EWHW}		145	—	ns

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time		A0	t_{CYC6}		500	—	ns
Address setup time		WR	t_{AW6}		40	—	ns
Address hold time		(R/W)	t_{AH6}		20	—	ns
Data setup time		D0 ~ D7	t_{DS6}		160	—	ns
Data hold time			t_{DH6}		20	—	ns
Output disable time			t_{OH6}	CL = 100pF	20	120	ns
Access time			t_{ACC6}		—	180	ns
Enable low pulse width	Read	RD (E)	t_{EWLR}		185	—	ns
	Write		t_{EWLW}		145	—	ns
Enable high pulse width	Read	RD (E)	t_{EWHR}		285	—	ns
	Write		t_{EWHW}		325	—	ns

Notes: 1. t_{EWHR} and t_{EWHW} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{RD}$ (E) high.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **Serial Interface**



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to +85°C

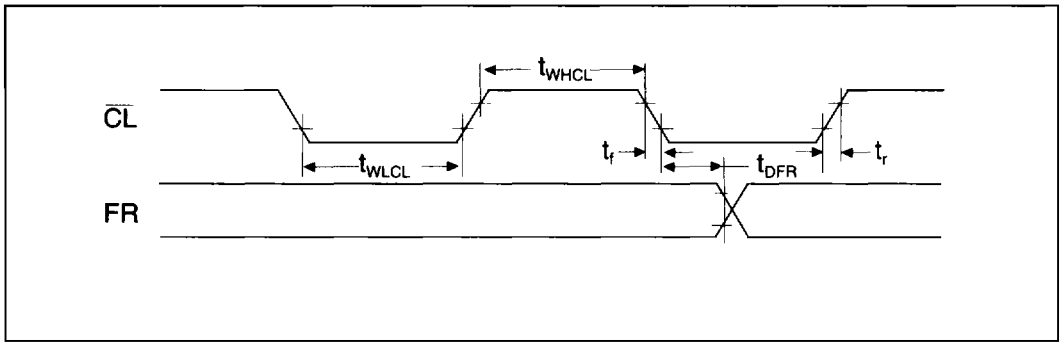
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock cycle	Serial clock	t_{SCYC}		500	—	ns
Serial clock H pulse width		t_{SHW}		150	—	ns
Serial clock L pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		120	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	Serial data	t_{SDS}		120	—	ns
Data hold time		t_{SDH}		50	—	ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2 = "1")	t_{CSS}		30	—	ns
		t_{CSH}		400	—	ns

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock cycle	Serial clock	t_{SCYC}		1000	—	ns
Serial clock H pulse width		t_{SHW}		300	—	ns
Serial clock L pulse width		t_{SLW}		300	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		400	—	ns
Data setup time	Serial data	t_{SDS}		250	—	ns
Data hold time		t_{SDH}		100	—	ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2 = "1")	t_{CSS}		60	—	ns
		t_{CSH}		800	—	ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ Display Control Timing



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Low-level pulse width	CL	t_{WLCL}	(TBD)	(TBD)	—	—	µs
High-level pulse width		t_{WHCL}	(TBD)	(TBD)	—	—	µs
Rise time		t_r	—	—	30	120	ns
Fall time		t_f	—	—	30	120	ns
FR delay time	FR	t_{DFR}	—	–1.0	0.2	1.0	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Low-level pulse width	CL	t_{WLCL}	(TBD)	(TBD)	—	—	µs
High-level pulse width		t_{WHCL}	(TBD)	(TBD)	—	—	µs
Rise time		t_r	—	—	60	240	ns
Fall time		t_f	—	—	60	240	ns
FR delay time	FR	t_{DFR}	—	–2.0	0.4	2.0	µs

○ Output Timing

V_{SS} = 0V, V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

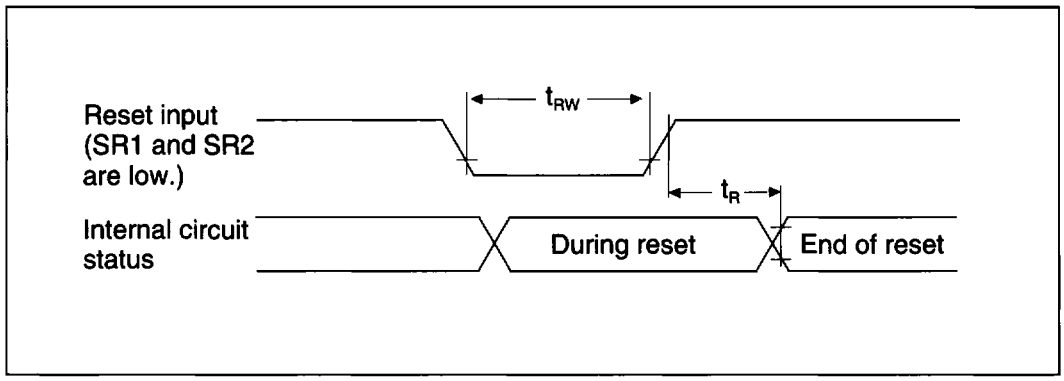
Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 100pF	—	0.2	0.4	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 100pF	—	0.4	0.8	µs

Notes: 1. The FR delay input timing must be set in slave mode; the FR delay output timing must be set in master mode.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

○ **Reset Timing**



V_{SS} = 0V, V_{DD} = 5.0V ± 10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		1.0	—	—	µs
Reset low pulse width	Reset input	t_{RW}		1.0	—	—	µs

V_{SS} = 0V, V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		3.0	—	—	µs
Reset low pulse width	Reset input	t_{RW}		30	—	—	µs

Notes:
1. t_R (reset time) represents the period from the rising edge of reset input to the end of internal circuit reset. The SED1526 Series can operate normally after t_R.
2. t_{RW} specifies the minimum pulse width of reset input. The low pulse exceeding t_{RW} is required for reset.
3. The input signal rise and fall times must be within 15 nanoseconds.
4. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

- **Commands**

The table below lists all available commands. The SED1526 Series uses a combination of A0, $\overline{RD}$ and $\overline{WR}$ (or R/$\overline{W}$) signals to identify data bus signals. Since the chip analyzes and executes each command using the internal clock only (no external clock is required), its processing speed is very high and its busy check is usually not required.

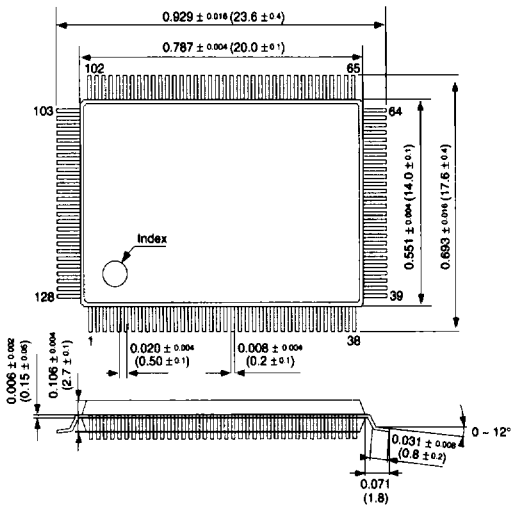
SED1526 Series Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	1	1	0	Initial display address					Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	1	Page address			Sets the display RAM page in Page Address register.
(4) Set Column Address	0	1	0	0	Column address							Sets RAM column address in Column register.
(5) Read Status	0	0	1	Status					0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	D0 = 0 Normal D0 = 1 Inverse
(9) Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Normal indication when low, but full indication when high.
(10) Duty Select	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD driver duty of 1/8 (1/16) when low, and 1/16 (1/32) when high.
(11) Duty+1	0	1	0	1	0	1	0	1	0	1	1	Selects normal LCD driver duty when low, and selects the duty added by 1 when high.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read/Modify/Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	1	0	1	1	0	Power control			Selects various power circuit functions.
(16) Set Electric Control	0	1	0	1	0	0	Electric control value					Sets V5 output voltage to Electronic Control register.
(17) Clock Stop	0	1	0	1	1	1	0	0	1	1	0/1	Stops clock output at CL when low, and stops clock when high.
(18) Power Save	—	—	—	—	—	—	—	—	—	—	—	A combination of Display OFF and Static Drive ON commands.

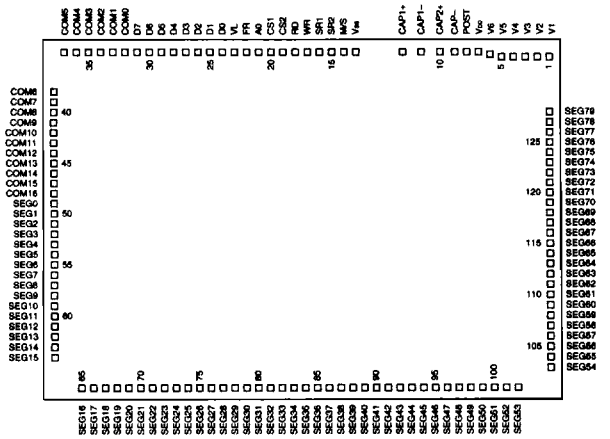
Note: Do not use any other command, or a system malfunction may result.

■ PACKAGE DIMENSIONS

Plastic QFP5-128pin-S1



Unit: inches (mm)



- Aluminum pad chip
  - Chip size ..... 5.92 × 4.86mm
  - Chip thickness .. 0.4mm
  - Pad opening ..... 81 × 85μm MIN
  - Pad pitch ..... 130μm MIN
- Gold bump chip (reference)
  - Chip size ..... 5.92 × 4.86mm
  - Chip thickness .. 0.4mm
  - Bump size ..... 70.9 × 74.7μm MIN
  - Bump height ..... 22.5 ± 5.5μm

■ PAD COORDINATES

PIN No.	PIN Name	X	Y
1	V1	2767	2106
2	V2	2637	2106
3	V3	2507	2106
4	V4	2377	2106
5	V5	2246	2106
6	VR	2116	2149
7	V_{DD}	1985	2176
8	V_{OUT}	1857	2176
9	CAP2–	1727	2176
10	CAP2+	1522	2176
11	CAP1–	1318	2176
12	CAP1+	1113	2176
13	V_{SS}	553	2166
14	M/S	356	2185
15	SR1	226	2185
16	SR2	95	2185
17	WR	–35	2185
18	RD	–165	2185
19	CS2	–295	2185
20	CS1	–425	2185
21	A0	–555	2185
22	FR	–719	2185
23	CL	–849	2185
24	D0	–979	2185
25	D1	–1109	2185
26	D2	–1239	2185
27	D3	–1369	2185
28	D4	–1500	2185
29	D5	–1630	2185
30	D6	–1760	2185
31	D7	–1890	2185
32	COM0	–2069	2185
33	COM1	–2199	2185
34	COM2	–2329	2185
35	COM3	–2459	2185
36	COM4	–2589	2185
37	COM5	–2719	2185
38	COM6	–2802	1624
39	COM7	–2802	1524
40	COM8	–2802	1393
41	COM9	–2802	1263
42	COM10	–2802	1133
43	COM11	–2802	1003

PIN No.	PIN Name	X	Y
44	COM12	–2802	873
45	COM13	–2802	743
46	COM14	–2802	612
47	COM15	–2802	482
48	COM16	–2802	352
49	SEG0	–2802	193
50	SEG1	–2802	63
51	SEG2	-2802	–67
52	SEG3	-2802	–197
53	SEG4	-2802	–327
54	SEG5	-2802	–457
55	SEG6	-2802	–588
56	SEG7	-2802	–718
57	SEG8	-2802	–848
58	SEG9	-2802	–978
59	SEG10	-2802	–1108
60	SEG11	-2802	–1238
61	SEG12	-2802	–1368
62	SEG13	-2802	–1499
63	SEG14	-2802	–1629
64	SEG15	-2802	–1759
65	SEG16	-2516	–2185
66	SEG17	-2367	–2185
67	SEG18	-2218	–2185
68	SEG19	-2088	–2185
69	SEG20	-1957	–2185
70	SEG21	-1827	–2185
71	SEG22	-1697	–2185
72	SEG23	-1567	–2185
73	SEG24	-1437	–2185
74	SEG25	-1307	–2185
75	SEG26	-1177	–2185
76	SEG27	-1046	–2185
77	SEG28	-916	–2185
78	SEG29	-786	–2185
79	SEG30	-656	–2185
80	SEG31	-526	–2185
81	SEG32	-396	–2185
82	SEG33	-266	-2185
83	SEG34	-135	-2185
84	SEG35	-5	-2185
85	SEG36	125	-2185
86	SEG37	255	-2185

PIN No.	PIN Name	X	Y
87	SEG38	385	-2185
88	SEG39	515	-2185
89	SEG40	646	-2185
90	SEG41	776	-2185
91	SEG42	906	-2185
92	SEG43	1036	-2185
93	SEG44	1166	-2185
94	SEG45	1296	-2185
95	SEG46	1426	-2185
96	SEG47	1557	-2185
97	SEG48	1687	-2185
98	SEG49	1817	-2185
99	SEG50	1947	-2185
100	SEG51	2077	-2185
101	SEG52	2226	–2185
102	SEG53	2375	–2185
103	SEG54	2802	–1932
104	SEG55	2802	–1802
105	SEG56	2802	–1672
106	SEG57	2802	–1541
107	SEG58	2802	–1411
108	SEG59	2802	–1281
109	SEG60	2802	–1151
110	SEG61	2802	–1021
111	SEG62	2802	–891
112	SEG63	2802	–760
113	SEG64	2802	–599
114	SEG65	2802	–469
115	SEG66	2802	–339
116	SEG67	2802	–209
117	SEG68	2802	–78
118	SEG69	2802	52
119	SEG70	2802	182
120	SEG71	2802	312
121	SEG72	2802	442
122	SEG73	2802	572
123	SEG74	2802	703
124	SEG75	2802	833
125	SEG76	2802	963
126	SEG77	2802	1093
127	SEG78	2802	1223
128	SEG79	2802	1353