MA31752

16-BIT FEEDTHROUGH ERROR DETECTION & CORRECTION UNIT (EDAC)

The MA31752 is a 16 bit Error Detection and Correction Unit intended for use in a high integrity system for monitoring and correcting data values retrieved from memory. The EDAC is placed in the data bus between the processor and the memory to be protected. Extra check bits added at each memory location are programmed transparently by the EDAC during a processor write cycle. The entire checkword and data combination is verified on read cycles. If any one bit in the incoming data stream is at fault the EDAC can correct the fault transparently, presenting the corrected 16-bit value to the processor. An error in two bits will be detected (but cannot be corrected). Both of these two error conditions are signalled to the system to allow the processor to take action as required.

Tristatable bus transceivers with a high drive capability are incorporated at both busses which may allow the usual bus driver devices to be removed, so reducing the overall timing overhead imposed by the EDAC. Although designed primarily for MA31750 application, this part may be used in almost any 16-bit processor system requiring high data integrity.

The device operates in a number of different modes to allow full and direct access to the memory system by the processor. This permits the processor to perform extensive testing of the main system memory and the error correction facilities. Byte-wide memory chip support is offered by using the two extra check bits.

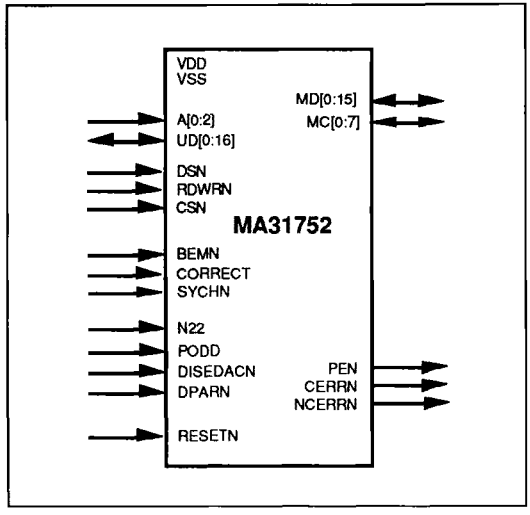

Figure 1: Block Diagram

FEATURES

- 16 Bit Operation with 6/8 Check Bits
- Radiation Hard CMOS/SOS Technology
- Flow-Through/Feed-Through Operation
- Support for x1, x4 and x8 Memories
- Error Correctable/Uncorrectable Flags
- Acts as a Data Buffer for CPU-Memory Interfacing
- On-Chip Parity Checking and Generation
- BIT Capability to Allow Testing of Error Detection and Syndrome Bit Production

1. PIN DESCRIPTIONS

Name	Input/ Output	Active	Description
Power:			
VDD	I	-	Supply (5V nominal)
VSS	I	-	Circuit 0V reference
Busses:			
UD[0:16]	I/O	High	User data bus (to processor). UD [16] is parity.
MD[0:15]	I/O	High	Memory data bus
MC[0:7]	I/O	High	Memory check bit bus (in six bit mode bits 0:1 are not used)
Error Flags:			
CERRN:	O	Low	Asserted low when a correctable (1 bit) error occurs (See Note 1)
NCERRN:	O	Low	Asserted low when an uncorrectable error occurs (See Note 1)
PEN	O	Low	Parity error output. A low level on this pin indicates an internal parity check fault.
Control signals:			
CORRECT	I	High	Selects between Correct and Detect modes. This function is also provided via bits in the EDAC control register.
SYCHN	I	Low	When low, error syndrome and memory check bits are made available on the User data bus.
N22	I	High	Selects between 22 bit or 24 bit error detection (24 bit is used with x8 memory organisation scheme). This function is also provided via bits in the EDAC control register.
PODD	I	High	Selects odd or even parity on processor bus parity pin. High gives odd parity, low gives even.
DPARN	I	Low	Disables parity check when low.
Register Control:			
CSN	I	Low	Enables selection of internal registers for read or write operation.
A[0:2]	I	High	Internal register address selection bits .
User bus strobes:			
RDWRN	I	Hi/Low	Read/write strobe
DSN	I	Low	Strobes data into internal registers on rising edge.
BEMN	I	Low	Output enable control for EDAC memory accesses.
Miscellaneous:			
DISEDACN	I	Low	In the disable state the EDAC acts as a buffer with parity, the syndrome detection is disabled and no error flags are enabled. MC[7] is the bus parity.
RESETN	I	Low	Resets the device to its default state when low.

Note 1: The error flag outputs will be inactive if the EDAC is disabled (DISEDACN is low).

Figure 2: Pin Descriptions

2. FUNCTIONAL DESCRIPTION

2.0 GENERAL

The EDAC is of flowthrough type with 16 data bits and 6/8 check bits. Two different codes are realised. The first code uses six check bits and is able to correct all single bit errors and detect all double bit errors. It can also detect any errors on any single 4-bit memory chip. The second code is an extension of the first with two extra check bits. This gives the additional capability to detect all errors on any single 8-bit memory chip. Note that when there are more than two errors, there are some bit patterns which may appear as possible correctable errors. Therefore the EDAC must be used in detect mode to provide no automatic correction. These errors will not be masked and the fault handling routine can investigate the error.

Control of the EDAC can be accomplished via discrete control lines or by software using the internal registers. The latter approach also provides access to the extensive built-in test facility within the part.

The EDAC is placed in the data bus between the processor and the memory to be protected. It forms the interface between the 22/24-bit memory bus and the 16-bit processor bus. Tristatable bus transceivers with a high drive capability are incorporated at both busses which may allow the usual bus driver devices to be removed so reducing the overall timing overhead imposed by the EDAC.

2.1 OPERATION WITHOUT USING INTERNAL REGISTERS

As mentioned above, it is possible to operate the MA31752 without using the registers inside the device. Such operation removes the requirement for MA31752 specific code and is useful where EDAC test support is not required. Figure 17 shows a typical system connection for operation in this mode.

2.2 OPERATION USING INTERNAL REGISTERS

There are six system-accessible registers which allow the function of the EDAC to be controlled from software. Each is accessed by asserting Chip Select (CSN) low after placing the appropriate address on A[0:2] as shown in Figure 3 below. Bits in the CSR allow control to be passed from the external discrete signals (following reset) to the control bits in the control and status register.

Mnem	Register	Read/ Write	A[0:2]
CSR	Control and Status Reg.	R/W	0
TR	Test Register	R/W	1,2,4
CBR	Check Bit Reg.	R/W	3
FFCBR	First Failing Check Bit Reg	R	5
CECR	Clear Error Counter Reg.	W	6
FFDR	First Failing Data Reg.	R/W	7

Figure 3: Control Register Addresses

2.3 REGISTER INITIALISATION STATE

Register	Bit No	Description	Value Following Reset
Control and Status reg	0	Check Injection / normal	0 (Normal i.e. from MC pins)
	1	Disable CORRECT input	0 (Use input signal CORRECT)
	2	Detect / Correct mode	Same as input signal CORRECT
	3	Disable N22 input	0 (Use input signal N22)
	4	N22 mode	Same as input signal N22
	5	Discrete PODD	Same as input signal PODD
	6	Discrete Dpar	Same as input signal DPARN
	7	Discrete DisE	Same as input signal DISEDACN
	8	Discrete N22	Same as input signal N22
	9	Error Status CE	0 (No error)
	10	Error Status NCE	0 (No error)
	11	Error Status PEN	0 (No error)
	12:15	Error Counter	0000 (No error)
Test Data Register	0:15		0000 (hex)
Check Bits Register	0:15		00xx (hex)
First Failing Check and Syndrome Register	0:15		0000 (hex)
First Failing Data Register	0:15		0000 (hex)

Figure 4: Initialisation State

2.4 TESTING THE EDAC

Additional internal registers are provided within the MA31752 to allow its function to be tested. A suitable test pattern can give almost 100% test coverage. The correction / detection capabilities of the EDAC, parity generation and checking, and full operation in both 6-bit and 8-bit modes can be tested. The first failing registers can also be tested and a full check done on the error counting facility. These tests are executed by constructing 22 or 24 bit test word in the TDR and CBR which may then be looped-back through the EDAC as if it had originated in the memory system. Corrected / uncorrected data can be checked, as can the stored syndrome/check bits.

The full register descriptions can be found in Section 3.

2.5 BUS CONTROL

There are five signals which control the drive status of the EDAC external busses and whether or not the syndrome bits are decoded in order to detect/correct errors: RDWRN, DSN, BEMN, CSN and DISEDACN. The relationships to each other is shown in Figure 5 below. The timing of these signals is shown in Section 5.

Bus	RDWRN	DSN	BEMN	Looptest	CSN	DISEDACN
User Data Bus	High	Low	Low	X	High	X
	High	Low	X	X	Low	X
Memory Data Bus	Low	Low	Low	X	High	X
	High	Low	X	Active *	Low	X
Check Bit Data Bus	Low	Low	Low	X	High	X
	High	Low	X	Active *	Low	X
Decode Syndrome	High	Low	Low	X	High	High
	High	Low	X	X	Low	X

* Note: Looptest is active when [0:2] is 2 or 3.

Figure 5: Bus Control

2.6 INTERNAL OPERATION

2.6.1 Check Bit Generation

The Check Bit Generation logic produces eight check bits from the incoming User Data Word UD[0:15] by masking it according to Figure 6 below: i.e. to create check bit 7, bits 13, 12, 8, 7, 6, 5, 4 and 0 of the data word are XORed together. MC[7] is the result.

These check bits are appended onto the 16 bits of user data to form a 24 bit word. Either all 24 bits are stored in memory to give error detection with memory chips 8 bits wide, or only 22 bits are stored to give error detection and correction for memory devices 1-bit wide and error detection for memory 4-bits wide.

MC	Parity	UD on write cycles															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	Even (XOR)			X	X				X	X	X	X	X				X
6	Even (XOR)		X			X	X	X	X		X		X			X	
5	Odd (XNOR)	X			X			X				X		X	X	X	X
4	Odd (XNOR)		X	X			X						X	X	X	X	X
3	Even (XOR)	X				X	X	X	X	X		X			X		
2	Even (XOR)	X	X	X	X	X				X	X			X			
1	Even (XOR)			X		X			X	X		X	X		X	X	
0	Odd (XNOR)	X		X	X	X						X		X	X	X	

Figure 6: Check Bit Generation (X indicates a bit of the UD bus used in the XOR/XNOR)

2.6.2 Syndrome Generation

The Syndrome Generation logic produces the Syndrome bits SY[0:7] from analysis of the incoming Memory Data MD[0:15] and its associated Check Bit, MC[0:7] according to Figure 7 following:

SY	Parity	MD on read cycles																MC							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	1	4	3	2	0
7	Odd (XNOR)			X	X				X	X	X	X	X				X	X							
6	Odd (XNOR)		X			X	X	X	X		X		X			X			X						
5	Even (XOR)	X			X			X				X		X	X	X	X			X					
4	Even (XOR)		X	X			X						X	X	X	X	X					X			
3	Odd (XNOR)	X				X	X	X	X	X		X			X								X		
2	Odd (XNOR)	X	X	X	X	X				X	X			X										X	
1	Odd (XNOR)			X		X			X	X		X	X		X	X					X				
0	Even (XOR)	X		X	X	X						X		X	X	X									X

Figure 7: Syndrome Generation (X indicates a bit from the MD/MC bus used in the XOR/XNOR)

If the memory uses x4 devices then the bits should be physically divided as follows: MD[0:3], MD[4:7], MD[8:11], MD[12:15], MC[0:2]+MC[6], MC[3:5]+MC[7]. For x8 organisation the bits should be divided MD[0:7], MD[8:15], MC[0:7].

2.6.2.1 6-Bit Syndrome Word

For the 6 syndrome bit code a single error in the data word read from memory causes three syndrome bits to be set low in the syndrome word. These low syndrome bits form a code which indicates which bit of the data is incorrect (the codes are shown in Figure 7.) For example, if MD[15] were incorrect, the syndrome word would have bits 2, 3 and 5 set low. The syndrome decoder in the EDAC decodes the information in the syndrome word and inverts the relevant bit of the data word if it is in correct mode. If there is an error in the check bit word, only one bit of the syndrome word is set low. This causes the error flag CERRN to be set but no correction is done as the check bit bus is not used by the system. If two errors occur, there will be either 2,4 or 5 bits set low in the syndrome word. The NCERRN error flag will be activated to indicate that errors are present but cannot be corrected. If any errors occur within one 4-bit wide memory chip, the 6-bit code can detect them. If more than two errors occur in different chips, any number of syndrome bits may be set which means that no conclusions can be drawn from the EDAC. Care must be taken if this situation arises as false information may be given by the EDAC to the system.

If a system is exposed to radiation and memory corruption occurs as a result of this, the chances are that the corruption will be confined to one memory chip. Therefore, on a system with 1-bit wide memory chips, single errors are expected and can be corrected with the 6-bit syndrome code. On a system with 4-bit wide memory chips, up to 4 errors can be expected if a chip is irradiated. These can be detected using the 6-bit syndrome code. If 8-bit wide memory chips are used, the 8-bit syndrome code should be used to detect up to 8 errors on one chip.

2.6.2.2 8-Bit Syndrome Word

For the 8 syndrome bit code, a single error in the data word read from memory can cause 3, 4 or 5 bits to be set low in the syndrome word as shown in Figure 7. The extra 2 syndrome bits mean that any number of errors can be detected within one 8-bit wide chip. However, the device must be used in detect mode as false information could cause the wrong bit to be corrected i.e. if the memory device storing the check bits was radiated and corrupted and MC[5], MC[3], MC[2] and MC[0] were erroneous, the EDAC would assume that MD[15] was a correctable error. The device should therefore be in detect mode and the flags should be ORed together to provide a general error flag.

3. REGISTER DESCRIPTION

3.1 CONTROL AND STATUS REGISTER (EDAC A[0:2] = 0)

Each register is shown with the most significant bit (UD[0]) on the left through to the least significant bit (UD[15]) on the right.

3.1.1 Read:

MSB=UD[0] LSB=UD[15]

CBI/N	DisC	C/D	DN22	N22	PODD	DPAR	DISE	N22	CE	NCE	PEN	Error Counter
EDAC mode and control					Discrete inputs				EDAC status			Error counter

3.1.2 Write:

CBI/N	DisC	C/D	DN22	N22	X	X	X	X	CE	NCE	PEN	X X X X

3.1.3 CSR Bit Functions

The bits contained in the CSR have the following meanings and actions:

Bit in CSR	Description
CBI/N	If this bit is low, the check bit source is the check bit generator (normal mode). If this bit is set the check bits are injected from the check bit register.
DisC	Setting this bit high disables the CORRECT signal input and enbles bit 2, the Correct/Detect mode bit, in the CSR. If low, the input signal overrides bit 2 of the CS register.
C/D	Setting this bit high selects EDAC correct mode. Otherwise errors are only detected.
DN22	Setting this bit high disables the N22 signal input and enables bit 4, the N22 mode bit, in the CS register. Otherwise the input signal overrides bit 4 in the CSR.
N22	Setting this bit high selects the 6 check bit code. Otherwise, 8 check bits are used.
PODD	Gives the state of the input signal pin PODD. A one indicates odd bus and register parity.
DPAR	Gives the state of the input signal DPARN. A zero indicates that the parity check is disabled i.e. PEN is deactivated.
DisE	Gives the state of the input signal pin DISEDACN. A zero indicates that the EDAC is disabled and deactivates the error flags CERRN and NCERRN.
N22	Gives the state of the input signal pin N22. A one indicates that the six bits check code is being employed, a zero indicates that all eight check bits are used.
CE	On a read cycle, this indicates that one or more correctable errors have occurred. This flag is cleared by writing a one to this bit.
NCE	On a read cycle, this indicates that one or more non-correctable errors have occurred. The flag is cleared by writing a one to this bit.
PEN	On a read cycle, this indicates that one or more parity errors have occurred. This flag is cleared by writing a one to this bit.
Error counter[3:0]	These bits count the number of correctable, non-correctable and parity errors to occur. The counter is cleared by writing to the Clear Error register (A[0:2] = 6). The maximum number of errors which can be counted is 15; if this is exceeded then the counter remains at 15 until cleared.

Figure 8: CSR Bit Functions

3.2 TEST DATA REGISTER (A[0:2] = 1)

3.2.1 Read/Write:

Test data from User Bus Data (17 bits)

Writing to this register stores the user data and the bus parity bit. Reading this data causes the register to remain unchanged.

3.3 TEST DATA LOOP BACK REGISTER (A[0:2] = 2)

3.3.1 Write:

Test data from User Bus Data (17 bits)

Writing to this register stores the user data together with the bus parity bit in the Test Data Register. At the same time the generated check bits will be stored in the Check Bit Register (CBR).

3.3.2 Read:

Corrected/uncorrected data from loopback test (16 bits)

Reading from this register causes the data stored in the Test Data Register to be looped through the EDAC with the Check Bit Register producing the check bits for the Syndrome Generator. The corrected/uncorrected data will be placed on the UD bus together with the parity from the built-in parity generator. The register contents are left unmodified.

3.4 CHECK BIT REGISTER (A[0:2] = 3)

3.4.1 Write:

Check Bit Register/Injection (8 bits)	X	X	X	X	X	X	X	X

Writing to this register stores the check bits in the CBR without parity.

3.4.2 Read:

Check Bit Register, Used Check bits (8 bits)	Unstored generated Syndrome (8 bits)

When this register is read the CBR will be looped through the EDAC together with the present data in the TDR. The code word thus generated is fed to the Syndrome Generator. The check bits used and the generated syndrome will be placed on the UD bus together with the parity from the internal parity generator.

3.5 TEST PARITY REGISTER (A[0:2] = 4)

3.5.1 Write:

Test Data from User Bus (17 bits)

Writing to this register checks internal parity bit generation. Data is stored in the Test Data Register with the internally generated parity bit.

3.5.2 Read:

Unmodified Test Data Register (16 bits)

Reading this register causes the unmodified test data to be placed on the user bus together with the inverted register parity bit forcing incorrect parity to be placed on the local data bus. This allows the bus parity error detection on the local bus master to be tested.

3.6 FIRST FAILING CHECK BITS/SYNDROME REGISTER (A[0:2] = 5)

3.6.1 Read:

First Failing Check Bits (8 bits)	First Failing Syndrome (8 bits)

This register latches the eight uncorrected memory check bits and the corresponding first-failing Syndrome when an error occurs (see FFDR). Parity is dynamically generated when this register is read, no parity bit is stored. This register is cleared when the FFDR is written to with valid parity.

3.7 CLEAR ERROR COUNTER REGISTER (A[0:2] = 6)

3.7.1 Write:

X

Writing to this location clears the EDAC error counter. Note that although particular data is not required the parity of the data supplied must be correct or the write will be aborted.

3.8 FIRST FAILING DATA REGISTER (A[0:2] = 7)

3.8.1 Write/Read:

First Failing Data (16 bits)

This register latches the 16 bits of uncorrected memory data from the memory data bus together with the generated parity bit when any of the following errors occurs:

1. EDAC correctable error.
2. EDAC uncorrectable error.
3. MD bus parity error (non EDAC mode, parity feedthrough).
4. UD bus parity error (EDAC register addresses 6 and 7 write access).

The first failing data and check and syndrome bits remain in the first failing registers until they are cleared by a write access to the FFDR. Note that parity must be correct for a FFDR write or the FFDR and the FFCb/Sy will not be cleared.

When one of the above errors occurs, the error counter within the CSR is incremented until 15 errors have been counted. Full information on the state of the system at the time of the fault may be obtained by capturing the First Failing Address, using a register external to the EDAC, as a fault occurs.

4. DC ELECTRICAL CHARACTERISTICS AND RATINGS

Absolute maximum ratings are shown in Figure 9. Stresses above those listed in the table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Operating Characteristics (Figure 10) section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD}+0.3	V
T_A	Operating temperature	-55	+125	°C
T_S	Storage temperature	-65	+150	°C

Figure 9: Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit	Notes
VOH	Output high voltage	Vdd-0.5	-	V	IOH = -5mA
VOL	Output low voltage	-	Vss+0.5	V	IOL= 5mA
VIH	Input high voltage	2.0	-	V	
VIL	Input low voltage	-	0.8	V	
IIL, IIH	Input current high/low	-	10	µA	
IOZ	Output tristate leakage	-	50	µA	VO = 0 - VDD
ISS	Standby current	-	10	mA	
IDD	Operating current	-	50	mA	

Note: Conditions VDD = 4.5 to 5.5V, Ta = -55 to +125°C
Mil-Std-883, method 5005, subgroups 1, 2, 3

Figure 10: Operating Electrical Characteristics

5. AC CHARACTERISTICS

Parameter	Description	Min	Max
T1	Address valid to CSN falling	-	-
T2	CSN falling to DSN falling	-	-
T3	DSN falling to user data bus valid (read)	-	30
T4	DSN falling to User data bus driven (read)	15	-
T5	DSN rising to User data bus tristate (read)	-	20
T6	DSN rising to User data bus invalid (read)	15	-
T7	DSN rising to CSN rising	-	-
T8	DSN rising to RDWRN invalid	-	-
T9	DSN rising to address invalid	-	-
T10	User data setup to DSN rising (write)	-	-
T11	User data hold after DSN rising (write)	-	-
T12	BEMN low to User data bus driven (processor read)	-	-
T13	MD[0:23] to UD[0:16] propagation (correct/no correct)	-	35
T14	BEMN rising to UD[0:16] tristate	-	-
T15	BEMN falling to Memory Data bus driven (processor write)	-	-
T16	UD[0:16] to MD[0:15] propagation delay	-	30
T17	BEMN rising to MD[0:15] tristate	-	-
T18	BEMN falling to Memory Checkbit bus driven (processor write)	-	-
T19	UD[0:16] to MC[0:7] propagation delay	-	30
T20	BEMN rising to MC[0:7] tristate	-	-

Mil-Std-883, method 5005, subgroups 9, 10, 11

Figure 11: Preliminary Timing Parameters (all timings are in ns unless otherwise stated)

The timings supplied are preliminary simulated data. No characterisation data is available at present.

Subgroup	Definition
1	Static characteristics specified in Figure 10 at +25°C
2	Static characteristics specified in Figure 10 at +125°C
3	Static characteristics specified in Figure 10 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 11 at +25°C
10	Switching characteristics specified in Figure 11 at +125°C
11	Switching characteristics specified in Figure 11 at -55°C

Figure 12: Definition of Subgroups

6. TIMING DIAGRAMS

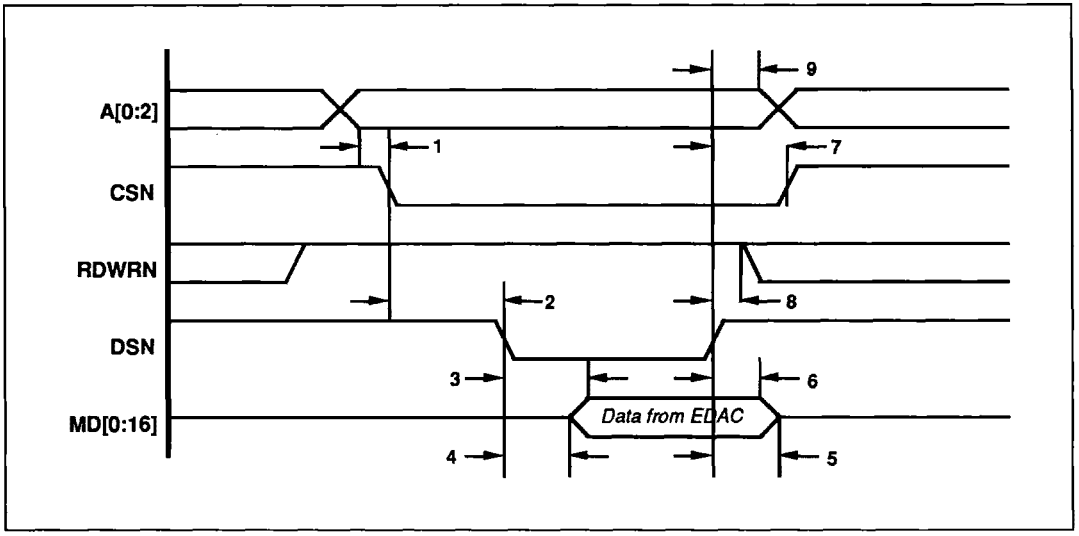

Figure 13: Register Read Cycle Timing

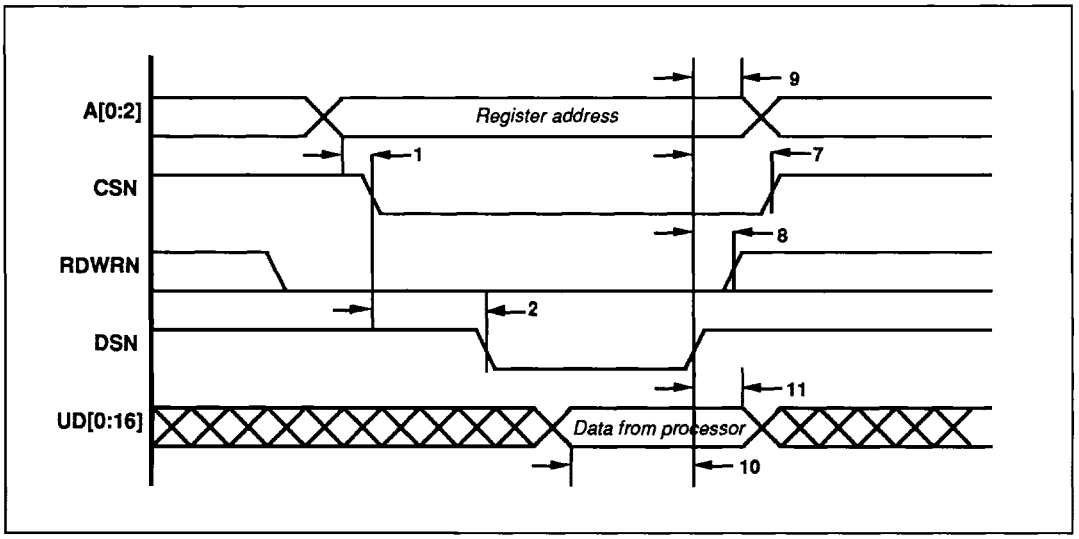

Figure 14: Register Write Cycle Timing

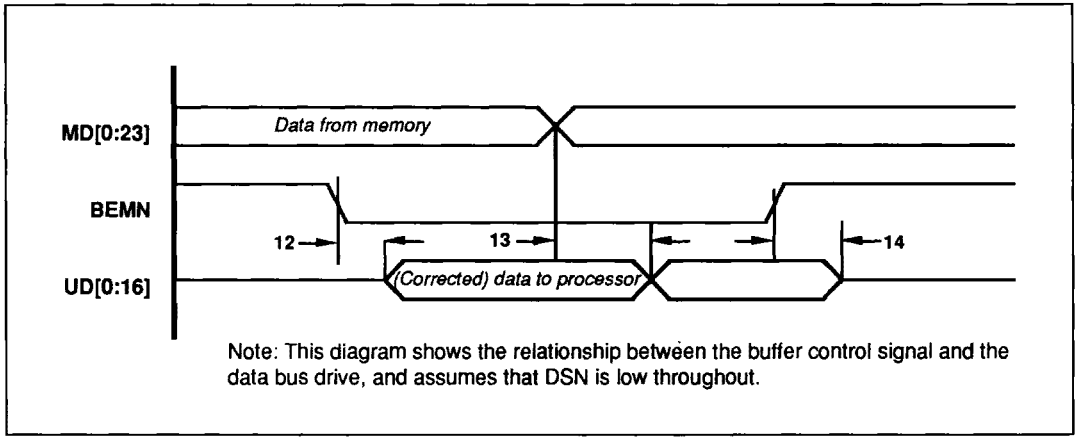

Figure 15: Buffer Enable Timing, Processor Reading from Memory

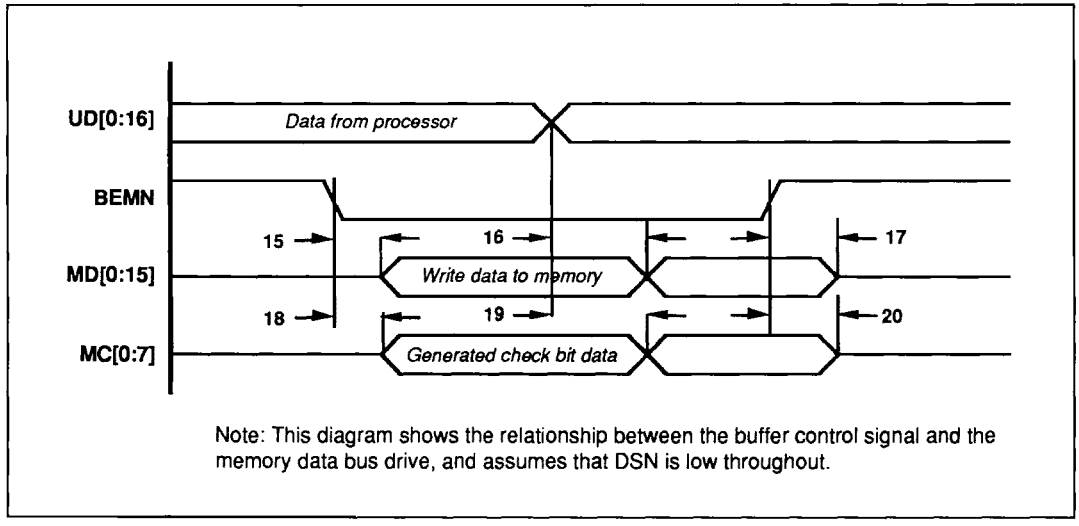

Figure 16: Buffer Enable Timing, Processor Writing to Memory

7. RADIATION TOLERANCE

7.1 TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (Survivability)	$>10^{11}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 17: Radiation Hardness Parameters

8. APPLICATIONS INFORMATION

The diagram below shows a typical system configuration for an MA31752 used in conjunction with the MA31750 processor. In this example the two fault indicators NCERRN and CERRN are returned to the processor interrupt inputs. The user is free to reassign these lines to different interrupt/ fault inputs or to ignore the error indication in the case of CERRN.

In this system the two buffer enable signal BEMN has been tied low. In a multiprocessor system this signal may be used to isolate the EDAC busses from the system and remove the need for extra tristatable buffers.

9. PACKAGING

The device is supplied in a 68-pin PGA for development with a 68-pin flatpack option for flight parts. No pinout is available at present.

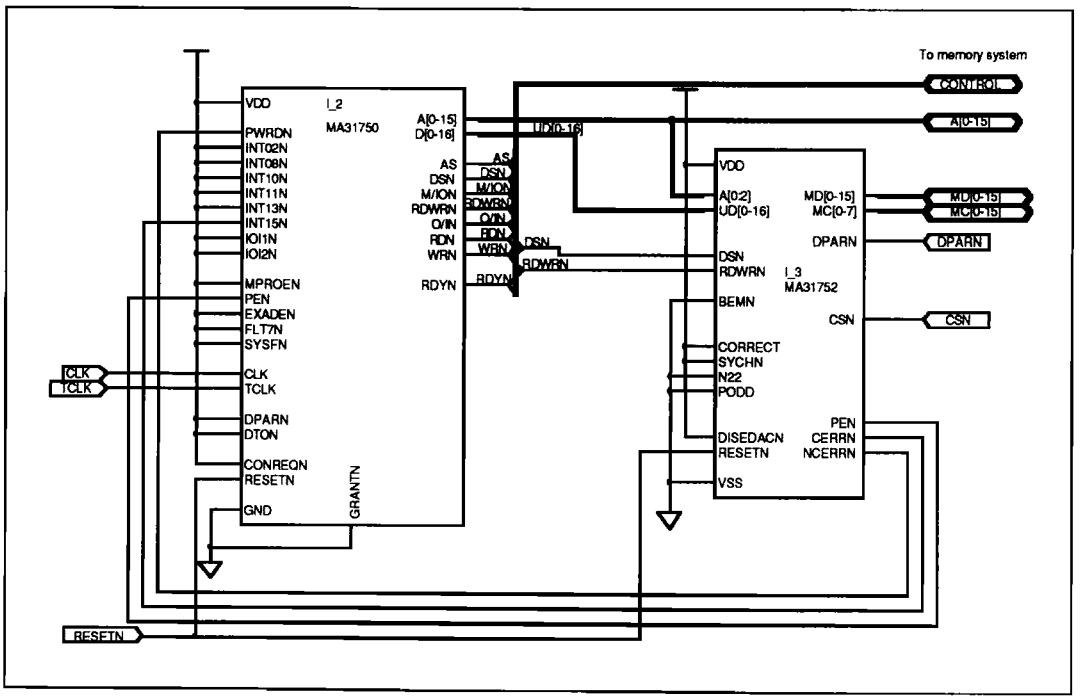

Figure 18: MA31750 to MA31752 Interfacing