EM78P210N

8-Bit Microcontroller with OTP ROM

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

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APPENDIX

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
0.9	Preliminary version	2007/03/20
1.0	Initial released version	2007/10/19
1.1	Renamed the Product as EM78P210N from EM78P211N, EM78P212N	2008/01/24
1.2	* 1. Retrieved ICE220N, Updated with ICE210N. * 2. For ICE210N and EM78P210N, added Green mode and Idle mode.	2008/04/22
1.3	Added LVR specifications	2013/04/22
1.4	1. Modified the package type in Section 2 *Features* 2. Added User Application Note 3. Modified Appendix A “Ordering and Manufacturing Information”	2016/04/18

*ICE210N vs ICE220N Comparison Table

Item	ICE220N	ICE210N
P72, P73 Function (when used as output pins)	Open drain pins	General Output pins
P81 Function (when used as output pins)	General Output pins	Open drain pins
Port 6 High Drive Function	×	o
Port 5 High Sink Function	×	o
Port 6 High Sink Function	×	o
Type Selection in Bank3-R7 Register	×	o
Operating Mode	Sleep, Normal	Sleep, Idle, Green, Normal

Note: *"o" = function is available if enabled* *"x" = function is not available*

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. The internal TCC will stop running when in sleep mode.

2. The noise rejection function is turned off in the LXT2 and sleep mode

1 General Description

The EM78P210N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has as an on-chip 2K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Two Code option bits are also available to meet user's requirements.

With its enhanced OTP-ROM features, the device provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development code.

2 Features

- CPU configuration
  - 2K×13 bits on-chip OTP-ROM
  - 80×8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Three programmable Level Voltage Reset (LVR) : 4.0V, 3.0V, 2.5V
  - Less than 1.5 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - Four bidirectional I/O ports: P5, P6, P7 and P8
  - Wake-up port : P6
  - 22 I/O pins
  - Eight programmable pull-down I/O pins
  - Eight programmable pull-high I/O pins
  - Eight programmable open-drain I/O pins
  - Eight Programmable high drive current I/O pins
  - 16 Programmable high sink current I/O pins
  - External interrupt : P77, P71
- Operating voltage range:
  - OTP version:
    Operating voltage: 2.1V~5.5V (commercial)
    Operating voltage: 2.3V~5.5V (industrial)
- Operating temperature range:
  Operating temperature: 0°C~70°C (commercial)
  Operating temperature: -40°C~85°C (industrial)
- Operating frequency range
  - Crystal mode:
    DC~16MHz/2 clks @ 4.5V; DC~125ns inst. cycle @ 4.5V
    DC~8 MHz/2 clks @ 3V; DC~250ns inst. Cycle @ 3V
  - ERC mode:
    DC~16 MHz/2 clks @ 4.5V; DC~125ns inst. cycle @ 4.5V
    DC~8 MHz/2 clks @ 3V; DC~250ns inst Cycle @ 3V
  - IRC mode:
    Oscillation mode: 16 MHz, 4 MHz, 1 MHz, 455kHz
    Process deviation: Typ. ± 3%, Max. ± 5%
    Temperature deviation: ± 5% (-40°C~85°C)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	±5%	±5%	±4%	±14%
16 MHz	±5%	±5%	±4%	±14%
1 MHz	±5%	±5%	±4%	±14%
455kHz	±5%	±5%	±4%	±14%

All the four main frequencies can be trimmed by programming with four calibrated bits in the ICE210N Simulator. OTP is auto trimmed by ELAN Writer (DWTR).

- Fast set-up time requires only 800μs (VDD:5V, Crystal: 4MHz, C1/C2: 30pF) in HXT2 mode and 10μs in IRC mode (VDD:5V IRC:4MHz)
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - One comparator (can act as an OP) (offset voltage is smaller than 10mV)
- Five available interrupts
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake up from sleep mode)
  - Two External interrupts
  - Comparator high/low interrupt
- Special Features
  - Programmable free running Watchdog Timer
  - Two clocks per instruction cycle
  - Power-on voltage detector available (1.8 V± 0.1V)
  - High EFT immunity (better performance at 4MHz or below)
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Package Type:
  - 20-pin DIP 300mil : EM78P210ND20
  - 20-pin SOP 300mil : EM78P210NSO20
  - 20-pin SSOP 209mil : EM78P210NSS20
  - 24-pin skinny DIP 300mil : EM78P210NK24
  - 24 pin SOP 300mil : EM78P210NSO24
  - 24 pin SSOP 209mil : EM78P210NSS24A

Note: *These are Green products which do not contain hazardous .substances.*

3 Pin Assignment

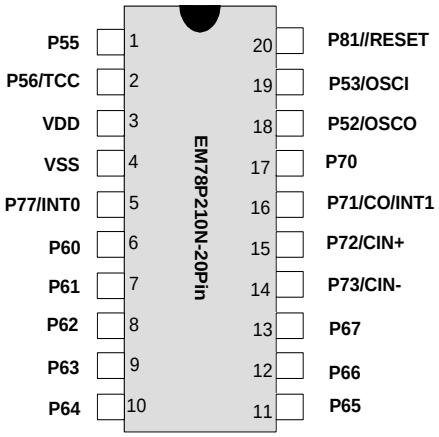


Figure 3-1 EM78P210ND20/SO20/SS20

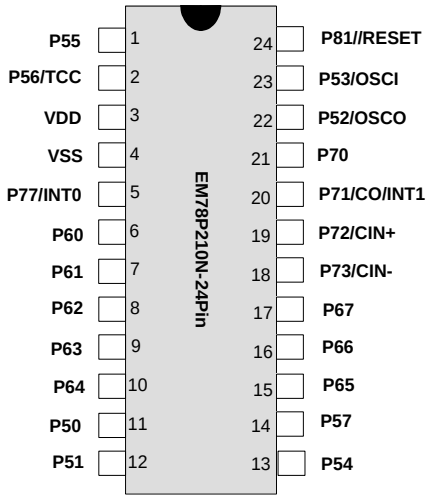


Figure 3-2 EM78P210NK24/SO24/SS24A

4 Pin Description

4.1 EM78P210ND20/SO20/SS20

Symbol	Pin No.	Type	Function
P52~P53 P55~P56	18~19 1~2	I/O	4-bit General purpose input/output pins. Pull-high (P52~P53) / Open-drain function. High sink function. Default value at power-on reset.
P60~P67	6 ~ 13	I/O	8-bit General purpose input/output pins. Pull-high (P64~P67) / Pull-down function. High drive / High sink function. Wake-up from sleep mode when the pin status changes. Default value at power-on reset.
P70~P73 P77	14 ~ 17 5	I/O	5-bit General purpose input/output pins. Default value at power-on reset.
P81	20	I/O	1-bit General purpose input or output open-drain pin. Default value at power-on reset.
CIN- CIN+ CO	14 15 16	I I O	"-" : input pin of Vin- of the comparator "+" : input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (Bank 1-RA) <3:4>
OSCI	19	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	18	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
/RESET	20	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
INT0~INT1	5, 16	I	External interrupt pin
VDD	3	-	Power supply
VSS	8	-	Ground

4.2 EM78P210NK24/SO24/SS24A

Symbol	Pin No.	Type	Function
P50~P57	11~14 22~23 1~2	I/O	8-bit General purpose input/output pins. Pull-high (P50~P53) / Open-drain function. High sink Function. Default value at power-on reset.
P60~P67	6 ~ 10 15 ~17	I/O	8-bit General purpose input/output pins. Pull-high (P64~P67) / Pull-down function. High drive / High sink function. Wake up from sleep mode when the pin status changes. Default value at power-on reset.
P70~P73 P77	18 ~ 21 5	I/O	5-bit General purpose input/output pins. Default value at power-on reset.
P81	24	I/O	1-bit General purpose input or output open-drain pin. Default value at power-on reset.
CIN- CIN+ CO	18 19 20	I I O	"-" : input pin of Vin- of the comparator "+" : input pin of Vin+ of the comparator Pin CO is the comparator output. Defined by CMPCON (Bank 1-RA) <3:4>
OSCI	23	I	Crystal type: Crystal input terminal RC type: RC oscillator input pin
OSCO	22	O	Crystal type: Output terminal for crystal oscillator. RC type: Clock output with a duration of one instruction cycle time. External clock signal input.
/RESET	24	I	If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode.
INT0~INT1	5, 20	I	External interrupt pin
VDD	3	-	Power supply
VSS	4	-	Ground

5 Block Diagram

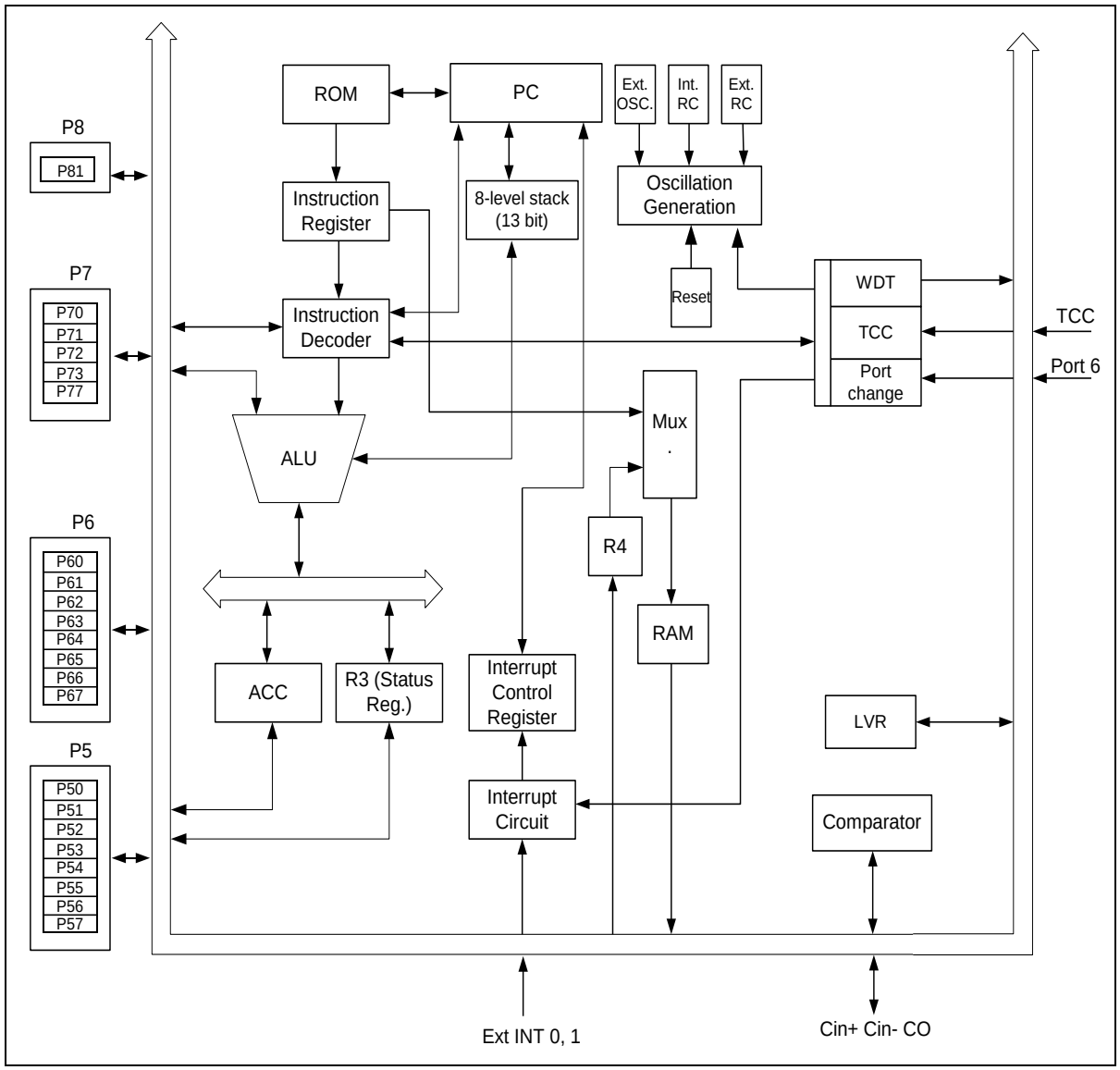


Figure 5 EM78P210N Functional Block Diagram

6 Functional Description

6.1 Register Configuration

Addr	Bank 0 Registers	Bank 1 Registers	Bank 2 Registers	Bank 3 Registers
00	**R0** (Indirect Addressing Register)			
01	**R1** (Memory switch register)			
02	**R2** (Program Counter)			
03	**R3** (Status Register)			
04	**R4** (Select Indirect Address)			
05	**R5** (Port 5)	**R5** (I/O Port Control Register)	**R5** (High Drive Control Register for Port 6)	**R5** (Time Clock / Counter)
06	**R6** (Port 6)	**R6** (I/O Port Control Register)	**R6** (High Sink Control Register for Port 5)	**R6** (IRC control Register) *
07	**R7** (Port 7)	**R7** (I/O Port Control Register)	**R7** (High Sink Control Register for Port 6)	**R7** (Noise and LVR Control Register) *
08	**R8** (Port 8)	**R8** (I/O Port Control Register)	**R8** (Operating mode Control Register)	Reserve
09	Reserve	Reserve	Reserve	Reserve
0A	Reserve	**RA** (Comparator Control Register)	Reserve	Reserve
0B	Reserve	**RB** (Pull-down Control Register)	Reserve	Reserve
0C	Reserve	**RC** (Open-drain Control Register)	Reserve	Reserve
0D	Reserve	**RD** (Pull-high Control Register)	Reserve	Reserve
0E	**RE** (Wake-up Control Register)	**RE** (WDT Control Register)	Reserve	Reserve
0F	**RF** (Interrupt Status Register)	**RF** (Interrupt Mask Register)	Reserve	Reserve
10 : 1F	General Registers (16×8 bits)			
20 : 3F	General Registers (32×8 bits)	General Registers (32×8 bits)		

Note: *1. All registers are 8 bits.*

2. When using ICE, some registers code options are set. Refer to Section 6.2 for detailed register description.

*3. Registers with asterisk * can only be used in ICE210N simulator.*

6.2 Registers Description

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT Signal Edge

0 = interrupt occurs at a rising edge on the INT0 and INT1 pin

1 = interrupt occurs at a falling edge on the INT0 and INT1 pin

Bit 6 (INT): Interrupt Enable Flag

0 = masked by DISI or hardware interrupt

1 = enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC Signal Source

0 = internal instruction cycle clock. If P56 is used as I/O pin, TS must be 0.

1 = transition on the TCC pin

Bit 4 (TE): TCC Signal Edge

0 = increment if the transition from low to high takes place on the TCC pin

1 = increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0 = prescaler disable bit. TCC rate is 1:1

1 = prescaler enable bit. TCC rate is set as Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: *Tcc time-out period [1/Fosc x prescaler x (256 -Tcc cnt) x 1]*
Fosc: Oscillator (Crystal, ERC, IRC) frequency

6.2.3 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.2.4 R1 (Memory Switch Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	"0"	"0"	BS1	BS0

Bits 7~2: Not used, fixed to "0" all the time.

Bits 1~0: is used to select Banks 0 ~ 1 for R20~R3F and select Banks 0~3 for control register.

See the table under Section 6.1 *Registers Configuration* for the data memory configuration.

6.2.5 R2 (Program Counter) and Stack

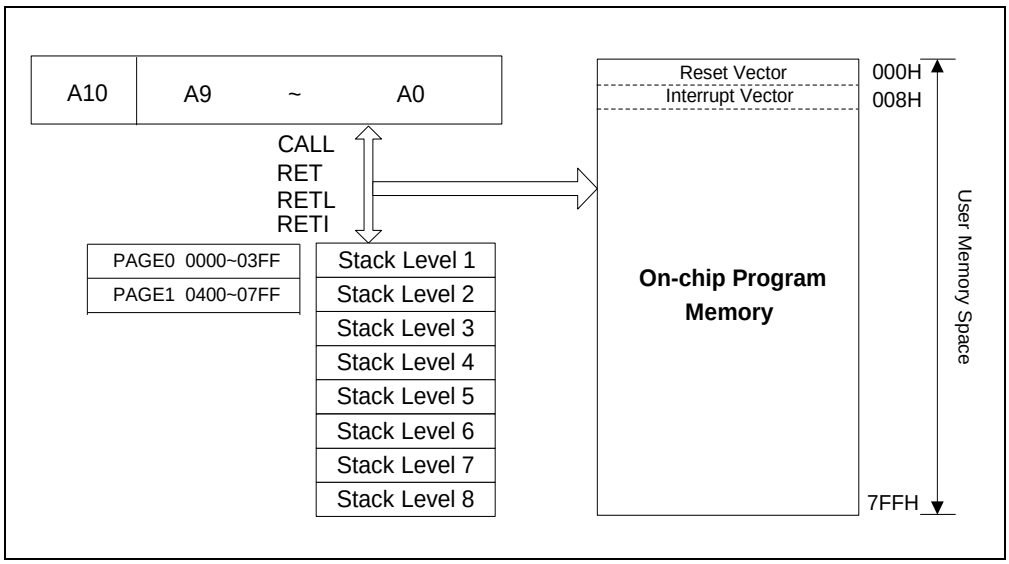


Figure 6-1 Program Counter Organization

R2 and hardware stacks are 11-bit wide. The structure is depicted in the table under Section *6.1Register Configuration*.

Generates 2K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

The contents of R2 are all set to "0"s when a reset condition occurs.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a Page (1K).

"CALL" instruction loads the lower 10 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page (1K).

"LJMP" instruction allows direct loading of the lower 11 program counter bits. Therefore, "LJMP" allows the PC to jump to any location within 2K (2^{11}).

"LCALL" instruction loads the lower 11 bits of the PC, and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 2K (2^{11}).

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of the stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will be incremented progressively.

"MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC will remain unchanged.

Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and above bits of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2) except “LCALL” and “LJMP” instructions. The “LCALL” and “LJMP” instructions need two instruction cycles.

6.2.6 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	T	P	Z	DC	C

Bits 7~5: not used, fixed to 0 all the time.

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power-on and reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 and Bit 3 (T and P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.2.7 R4 (Select Indirect Address)

Bits 7~6: not used, fixed to 0 all the time.

Bit 5 ~ 0: used to select registers (Address**:** 00 ~ 3F) in indirect addressing mode.

6.2.8 Bank 0-R5 (Port 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

Bits 7 ~ 0 (P57 ~ P50): I/O data bits

6.2.9 Bank 0-R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Bits 7 ~ 0 (P67 ~ P60): I/O data bits

6.2.10 Bank 0-R7 (Port 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P77	0	0	0	P73	P72	P71	P70

Bits 7, 3 ~ 0 (P77, P73 ~ P70): I/O data bits

Bits 6~4: not used, fixed to 0 all the time.

6.2.11 Bank 0-R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	NREN	0	0	0	P81	0

Bits 7~6, 4~2, 0: not used, fixed to 0 all the time.

Bit 5 (NREN): Noise rejection enable

0 = disable noise rejection (Default)

1 = enable noise rejection. However in crystal oscillator mode (LXT2), the noise rejection circuit is always disabled.

Bit 1 (P81): I/O data bit.

[Note]: P81 is input or open-drain for output pin.

6.2.12 Bank 0-R9~RD (Reserve)

Bits 7~0: not used, fixed to "0" all the time.

6.2.13 Bank 0-RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EX1IF	0	0	ICWE	0	CMPWE	0	CMPIF

Bit 7 (EX1IF): External interrupt flag. Set by INT1 pin, reset by software.

0 = no interrupt occurs

1 = with interrupt request

Bits 6~5, 3, 1: not used, fixed to "0" all the time

Bit 4 (ICWE): Port 6 input change to wake-up status enable bit

0 = Disable Port 6 input change to wake-up status

1 = Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to enter interrupt vector or to wake-up EM78P210N from sleep, the ICWE bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

0 = Disable Comparator wake-up

1 = Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up from sleep, the CMPWE bit must be set to "Enable".

Bit 0 (CMPIF): Comparator Interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

0 = no interrupt occurs

1 = with interrupt request

NOTE

- *Bank 0-RE <7, 0> can be cleared by instruction but cannot be set.*
- *Bank 1-RE <0> is an interrupt mask register.*
- *Interrupt results from "logic AND" of Bank 0-RE <7, 0> and Bank 1-RE <0>, with instruction "ENI".*

6.2.14 Bank 0-RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	EX0IF	ICIF	TCIF

Bits 7~3: not used, fixed to "0" all the time

Bit 2 (EX0IF): External interrupt flag. Set by INT0 pin. Reset by software.

0 = no interrupt occurs

1 = with interrupt request

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

0 = no interrupt occurs

1 = with interrupt request

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

0 = no interrupt occurs

1 = with interrupt request

NOTE

- *Bank 0-RF <2, 1, 0> can be cleared by instruction but cannot be set.*
- *Bank 1-RF <2, 1, 0> is an interrupt mask register.*
- *Interrupt results from "Logic AND" of Bank 0-RF <2, 1, 0> and Bank 1-RF <2, 1, 0> with instruction "ENI".*

6.2.15 Bank 1-R5 ~R7 (I/O Port Control Register)

0 = defines the relative I/O pin as output

1 = puts the relative I/O pin into high impedance

Bank 1-R5, R6 and R7 registers are all readable and writable.

6.2.16 Bank 1-R8 (I/O Port Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	C81	0

Bits 7~2, 0: not used, fixed to 0 all the time

Bit 1 (C81): **0** = defines the relative I/O pin as output

1 = puts the relative I/O pin into high impedance

[Note]: P81 is input or open-drain output pin.

6.2.17 Bank 1-R9 (Reserve)

Bits 7~0: not used, fixed to 0 all the time

6.2.18 Bank 1-RA (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIS1	EIS0	CMPOUT	CMPCOS1	CMPCOS0	0	0	0

Bit 7 (EIS1): Control bit used to define the function of the P71 (/INT1) pin

0 = P71, normal I/O pin

1 = /INT1, external interrupt pin. In this case, the I/O control bit of P71 (Bit 1 of Bank 1-R7) must be set to "1".

Bit 6 (EIS0): Control bit used to define the function of the P77 (/INT0) pin

0 = P77, normal I/O pin

1 = /INT0, external interrupt pin. In this case, the I/O control bit of P77 (Bit 7 of Bank 1-R7) must be set to "1"

NOTE

- *When EIS is "0," the path of /INT is masked. When EIS is "1," the status of /INT pin can also be read by way of reading Port 7 (Bank 0-R7). Refer to Figure 6-4 (I/O Port and I/O Control Register Circuit for P77 (/INT0) and P71 (/INT1) under Section 6.4 (I/O Ports).*
- *EIS0 and EIS1 are both readable and writable.*
- *The highest priority of P71/INT1/CO is INT1. When EIS1=0, the working type of P71/INT1/CO is determined by CMPCOS1 and CMPCOS0.*

Bit 5 (CMPOUT): The result of the comparator output

Bit 4 ~ Bit 3 (CMPCOS1 ~ CMPCOS0): Comparator Select bits

CMPCOS1	CMPCOS0	Function Description
0	0	Comparator is not used. P72, P73, and P71 are normal I/O pins.
0	1	P72 and P73 are Comparator input pins and P71 is normal I/O pin.
1	0	P72 and P73 are Comparator input pins and P71 is Comparator output pin (CO)
1	1	Used as OP and P71 is OP output pin (CO)

Bits 2~0: not used, fixed to 0 all the time

6.2.19 Bank 1-RB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bank 1-RB register is both readable and writable

Bit 7 (/PD7): Control bit is used to enable the pull-down of the P67 pin

0 = Enable internal pull-down

1 = Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable P66 pull-down pin

Bit 5 (/PD5): Control bit used to enable P65 pull-down pin

Bit 4 (/PD4): Control bit used to enable P64 pull-down pin

Bit 3 (/PD3): Control bit used to enable P63 pull-down pin

Bit 2 (/PD2): Control bit used to enable P62 pull-down pin

Bit 1 (/PD1): Control bit used to enable P61 pull-down pin

Bit 0 (/PD0): Control bit used to enable P60 pull-down pin

6.2.20 Bank 1-RC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/OD7	/OD6	/OD3	/OD2	/OD5	/OD4	/OD1	/OD0

Bank 1-RC register is both readable and writable.

Bit 7 (OD7): Control bit is used to enable the open-drain of the P57 pin.

0 = Enable open-drain output

1 = Disable open-drain output

Bit 6 (OD6): Control bit used to enable open-drain output of the P56 pin.

Bit 5 (OD5): Control bit used to enable open-drain output of the P55 pin.

Bit 4 (OD4): Control bit used to enable open-drain output of the P54 pin.

Bit 3 (OD3): Control bit used to enable open-drain output of the P53 pin.

Bit 2 (OD2): Control bit used to enable open-drain output of the P52 pin.

Bit 1 (OD1): Control bit used to enable open-drain output of the P51 pin.

Bit 0 (OD0): Control bit used to enable open-drain output of the P50 pin.

6.2.21 Bank 1-RD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bank 1-RD register is both readable and writable.

Bit 7 (/PH7): Control bit used to enable the pull-high function of the P67 pin.

0 = Enable internal pull-high

1 = Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable pull-high function of the P66 pin.

Bit 5 (/PH5): Control bit used to enable pull-high function of the P65 pin.

Bit 4 (/PH4): Control bit used to enable pull-high function of the P64 pin.

Bit 3 (/PH3): Control bit used to enable pull-high function of the P53 pin.

Bit 2 (/PH2): Control bit used to enable pull-high function of the P52 pin.

Bit 1 (/PH1): Control bit used to enable pull-high function of the P51 pin.

Bit 0 (/PH0): Control bit used to enable pull-high function of the P50 pin.

6.2.22 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	0	PSWE	PSW2	PSW1	PSW0	0	CMPIE

NOTE

- *Bank 1-RE <0> register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the Bank 1-RF <0 > to "1".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 7 (WDTE): Control bit is used to enable Watchdog Timer

0 = Disable WDT

1 = Enable WDT

WDTE is both readable and writable.

Bits 6, 1: not used, fixed to 0 all the time

Bit 5 (PSWE): Prescaler enable bit for WDT

0 = prescaler disable bit. WDT rate is 1:1

1 = prescaler enable bit. WDT rate is set as Bit 4~Bit 2

Bit 4 ~ Bit 2 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 0 (CMPIE): CMPIF interrupt enable bit

0 = Disable CMPIF interrupt

1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter next instruction, the CMPIE bit must be set to “Enable”. But actually the comparator output must be read to latch the status first. Then the output of the comparator is compared to this latch to produce the information of output status change.

6.2.23 Bank 1-RF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	EXIE	ICIE	TCIE

NOTE

- *RF register is both readable and writable.*
- *Individual interrupt is enabled by setting its associated control bit in the RF to "1".*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bits 7~3: not used, fixed to "0" all the time

Bit 2 (EXIE): EX0IF and EX1IF interrupts enable bit

0 = Disable EX0IF and EX1IF interrupts

1 = Enable EX0IF and EX1IF interrupts

Bit 1 (ICIE): ICIF interrupt enable bit

0 = Disable ICIF interrupt

1 = Enable ICIF interrupt

If Port 6 Input Status Change Interrupt is used to enter an interrupt vector or to enter next instruction, the ICIE bit must be set to "Enable".

Bit 0 (TCIE): TCIF interrupt enable bit

0 = Disable TCIF interrupt

1 = Enable TCIF interrupt

6.2.24 Bank 2-R5 (HDCR: High Drive Control Register for Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60

Bit 7 (HD67): Output High Drive Current Select for P67

Bit 6 (HD66): Output High Drive Current Select for P66

Bit 5 (HD65): Output High Drive Current Select for P65

Bit 4 (HD64): Output High Drive Current Select for P64

Bit 3 (HD63): Output High Drive Current Select for P63

Bit 2 (HD62): Output High Drive Current Select for P62

Bit 1 (HD61): Output High Drive Current Select for P61

Bit 0 (HD60): Output High Drive Current Select for P60

HDxx	VDD = 5V, Drive Current
0	9 mA (in 0.9VDD)
1	27 mA (in 0.7VDD)

6.2.25 Bank 2-R6 (HSCR1: High Sink Control Register for Port 5)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS50

Bit 7 (HS57): Output High Sink Current Select for P57

Bit 6 (HS56): Output High Sink Current Select for P56

Bit 5 (H55): Output High Sink Current Select for P55

Bit 4 (H54): Output High Sink Current Select for P54

Bit 3 (H53): Output High Sink Current Select for P53

Bit 2 (H52): Output High Sink Current Select for P52

Bit 1 (H51): Output High Sink Current Select for P51

Bit 0 (H50): Output High Sink Current Select for P50

HDxx	VDD = 5V, Sink Current
0	18 mA (in 0.1VDD)
1	75 mA (in 0.3VDD)

6.2.26 Bank 2-R7 (HSCR2: High Sink Control Register for Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60

Bit 7 (HS67): Output High Sink Current Select for P67

Bit 6 (HS66): Output High Sink Current Select for P66

Bit 5 (H65): Output High Sink Current Select for P65

Bit 4 (H64): Output High Sink Current Select for P64

Bit 3 (H63): Output High Sink Current Select for P63

Bit 2 (H62): Output High Sink Current Select for P62

Bit 1 (H61): Output High Sink Current Select for P61

Bit 0 (H60): Output High Sink Current Select for P60

HDxx	VDD = 5V, Sink Current
0	18 mA (in 0.1VDD)
1	75 mA (in 0.3VDD)

6.2.27 Bank 2-R8 (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TIMERSC	CPUS	IDLE	0	0	0	0

Bit 7: not used, fixed to "0" all the time.

Bit 6 (TIMERSC): TCC clock sources.

0 = Fs: sub frequency for WDT internal RC time base 16kHz ± 30% (fs)

1 = Fm: main-oscillator clock (fosc)

Bit 5 (CPUS): CPU Oscillator Source Select

0 : sub-oscillator (fs)

1 : main oscillator (fosc)

When CPUS=0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

From SLEP instruction, this bit will determine as to which mode to choose.

0 : IDLE = '0' + SLEP instruction → sleep mode

1 : IDLE = '1' + SLEP instruction → idle mode

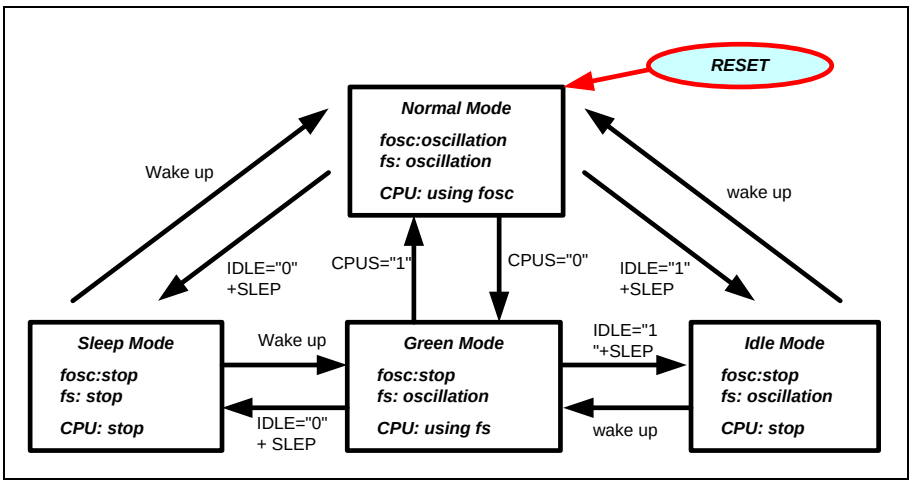


Figure 6-2 CPU Operation Mode Diagram

Bits 3~0: not used, fixed to "0" all the time.

6.2.28 Bank 2-R9~RF (Reserve)

Bits 7~0: not used, fixed to "0" all the time

6.2.29 Bank 3-R5 (Timer Clock/Counter)

- Incremented by an external signal edge through the TCC pin, or by the instruction cycle clock.
- External signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increment the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

6.2.30 Bank 3-R6 (IRC Control)-only for ICE

Bit	7	6	5	4	3	2	1	0
EM78P210N	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
ICE210N	C3	C2	C1	C0	RCM1	RCM0	'0'	'0'

Bits 7 ~ 2:

[With Simulator (C3~C0, RCM1~RCM0)]: IRC calibration bits in IRC oscillator mode. In IRC oscillator mode of the ICE210N simulator, these are the IRC mode selection bits and IRC calibration bits.

[With EM78P210N]: Unimplemented, read as '0'.

Bits 7 ~ 4 (C3 ~ C0): Calibrator of internal RC mode

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) × F
0	0	0	1	(1-31.5%) × F
0	0	1	0	(1-27%) × F
0	0	1	1	(1-22.5%) × F
0	1	0	0	(1-18%) × F
0	1	0	1	(1-13.5%) × F
0	1	1	0	(1-9%) × F
0	1	1	1	(1-4.5%) × F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) × F
1	1	0	1	(1+9%) × F
1	1	0	0	(1+135%) × F
1	0	1	1	(1+18%) × F
1	0	1	0	(1+22.5%) × F
1	0	0	1	(1+27%) × F
1	0	0	0	(1+31.5%) × F

1. Frequency values shown are theoretical and taken at an instance of a high frequency mode. Hence, frequency values are shown for reference only. Definite values depend on the actual process.
2. Similar way of calculation is also applicable to low frequency mode.

Bits 3 ~ 2 (RCM1 ~ RCM0): IRC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (default)
1	0	16
0	1	1
0	0	455kHz

Bits 1 ~ 0: are not used, fixed to "0" all the time.

6.2.31 Bank 3-R7 (Noise and LVR Control) - only for ICE

Bit	7	6	5	4	3	2	1	0
EM78P210N	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
ICE210N	"0"	"0"	TYPE1	TYPE0	NRHL	NRE	LVR1	LVR0

[With EM78P210N]: Unimplemented, read as '0'.

[With Simulator]:

Bits 7 ~ 6: not used, fixed to "0" all the time.

Bits 5 ~ 4 (TYPE1, TYPE0): Type selection for EM78P210N

TYPE1, TYPE0	MCU Type
00	EM78P210N-20Pin
01	
10	EM78P210N-24Pin
11	Not used

Bit 3 (NRHL): Noise rejection high/low pulse defined bit. The INT pin is a falling edge trigger

0 = Pulses equal to 8/fc [s] are regarded as signal.

1 = Pulses equal to 32/fc [s] are regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and in sleep mode.

Bit 2 (NRE): Noise rejection enable

0 = disable noise rejection

1 = enable noise rejection (default). However in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bits 1 ~ 0 (LVR1 ~ LVR0): Low Voltage Reset enable bits. If Vdd has a crossover at Vdd reset level as Vdd changes, the system will be reset.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.5V	2.7V
01	3.0V	3.2V
00	4.0V	4.2V

6.2.32 Bank 3-R8~RF (Reserve)

Bits 7~0: are not used, fixed to "0" all the time.

6.2.33 R10 ~ R1F

All of these are 8-bit general-purpose registers.

6.2.34 Banks 0~3 - R20 ~ R3F

All of these are 8-bit general-purpose registers.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT. The PST2~PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2~PSW0 bits of the Bank 1-RE register are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler are cleared by the "WDTC" and "SLEP" instructions. Figure 6-2 depicts the block diagram of TCC/WDT.

TCC (Bank 3-R5) is an 8-bit timer/counter. The TCC clock source can be internal clock (Fosc) or external signal input (edge selectable from the TCC pin). If the TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than 1CLK. 1 CLK is always Fosc/2. Refer to Figure 6-2.

NOTE

The internal TCC will stop running when in sleep mode.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode through software programming. Refer to WDTE bit of Bank 1-RE register (Section 6.2.10 Bank 1-RE (WDT Control Register). With no prescaler, the WDT time-out duration is approximately 18ms.[1]

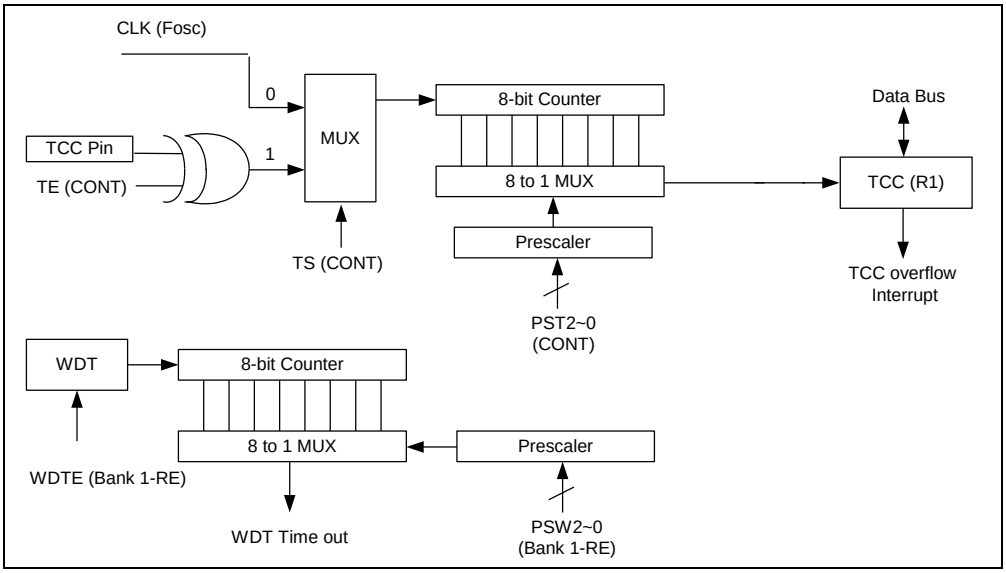
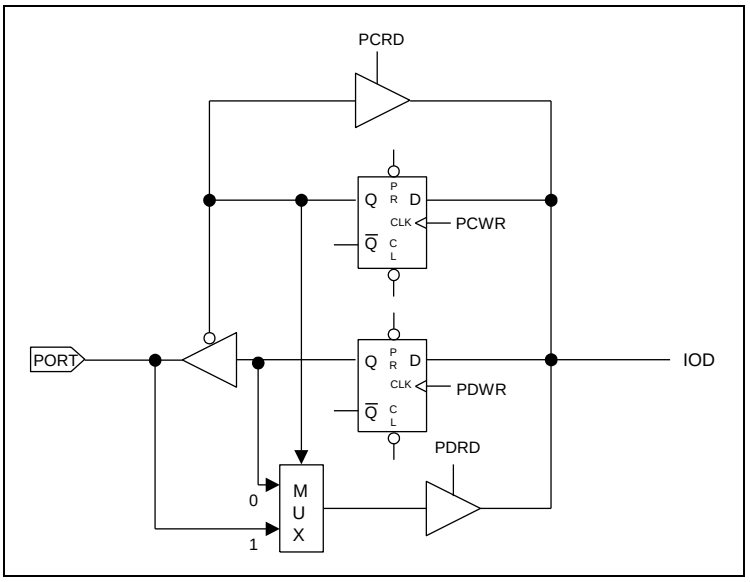


Figure 6-3 TCC and WDT Block Diagram

[1] *VDD=5V, WDT Time-out period = 15.2ms ± 30%.*
VDD=3V, WDT Time-out period = 18ms ± 30%.

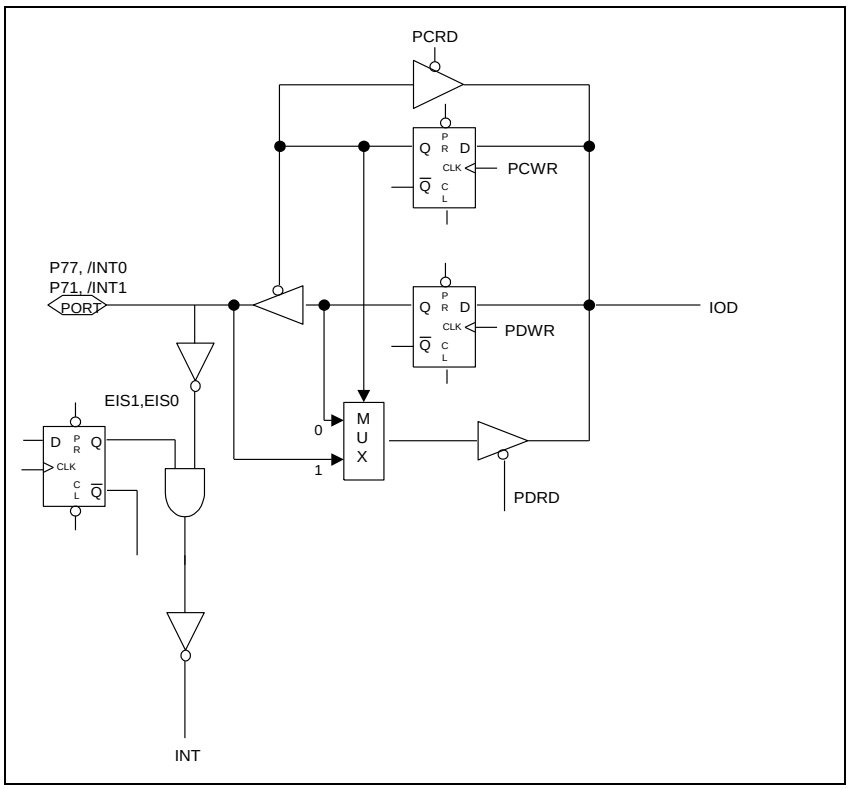
6.4 I/O Ports

The I/O registers (Port 5, Port 6, Port 7, and Port 8) are bidirectional tri-state I/O ports. The Pull-high, Pull-down, and Open-drain functions can be set internally by Bank 1-RB, Bank 1-RC, and Bank 1-RD respectively. The High drive and High Sink functions can be set internally by Bank 2-R5, Bank 2-R6, and Bank 2-R7 respectively. Port 6 features an input status change interrupt (or wake-up) function. Most I/O pin can be defined as "input" or "output" pin by the I/O control registers. The I/O registers and I/O control registers are both readable and writable. However, the initial states of these I/O ports (Port 5, Port 6, Port 7 and Port 8) are unknown input (high impedance). Then, if the I/O pin is pulled to a level at external circuit, the pin must induce a voltage. Hence, user must take into consideration whether the induced voltage causes a wrong action in the system. The I/O interface circuits for Port 5, Port 6, Port 7, and Port 8 are illustrated in Figures 6-4, 6-5, and 6-6 respectively. Port 6 with Input Change Interrupt/Wake-up is shown in Figure 6-7.



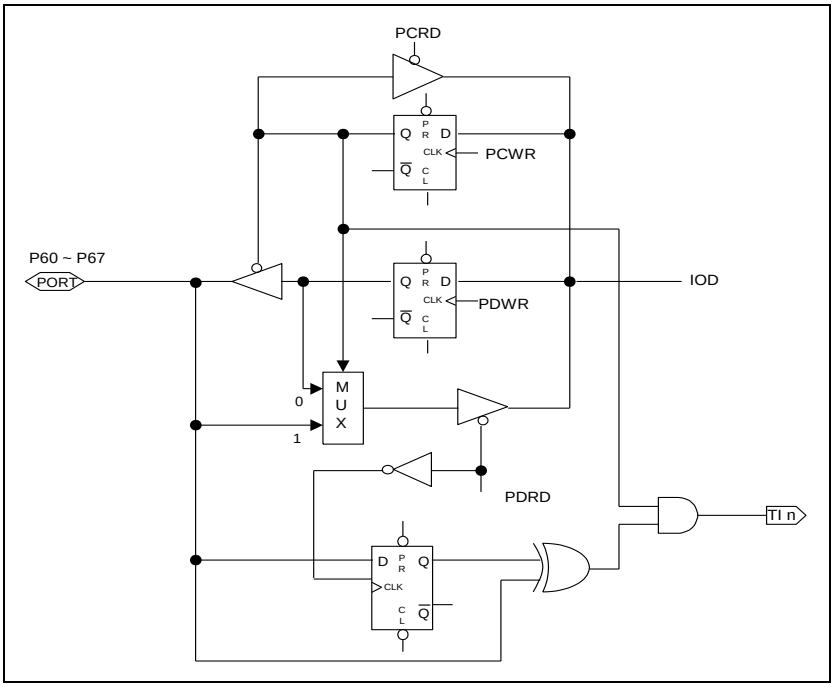
Note: *Pull-high and Open-drain are not shown in the figure.*

Figure 6-4 I/O Port and I/O Control Register Circuit for Port 5, Port 7 and Port 8



Note: CO, Pull-high and Open-drain are not shown in the figure.

Figure 6-5 I/O Port and I/O Control Register Circuit for P77 (/INT0) and P71 (/INT1)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-6 I/O Port and I/O Control Register Circuit for Port 6

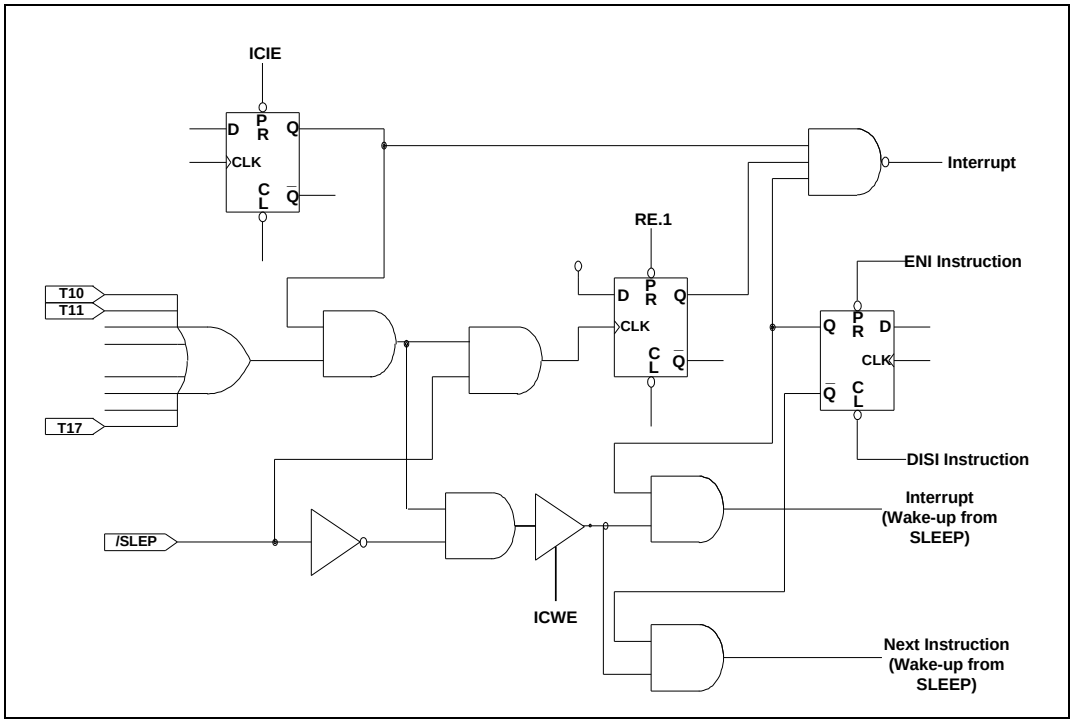


Figure 6-7 Port 6 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(1) Wake-up	**(2) Wake-up and Interrupt**
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set Bank 0-RE ICWE =1)	4. Enable wake-up bit (Set Bank 0-RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set BANK1-RF ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction
(3) Interrupt	
(a) Before Port 6 pin change	
1. Read I/O Port 6 (MOV R6,R6)	
2. Execute "ENI" or "DISI"	
3. Enable interrupt (Set BANK1-RF ICIE =1)	
(b) After Port 6 pin changed (interrupt)	
1. IF "ENI" → Interrupt vector (008H)	
2. IF "DISI" → Next instruction	

6.5 Reset and Wake-up

6.5.1 Reset and Wake-up Operation

A reset is initiated by one of the following events**:**

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

A device is kept in a reset condition for the duration of approximately 18ms[2] after the reset is detected. When in LXT 2 mode, the reset time is 500ms. Once a reset occurs, the following functions are performed (the initial address is 000h):

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, the Memory switch register (R1) is set to 0.
- The CONT register bits are set to all "0" except for Bit 6 (INT flag).
- Bank 0-RF register bits are set to all "0".
- Bank 1-RB register bits are set to all "1".
- Bank 1-RC register bits are set to all "1".
- Bank 1-RD register bits are set to all "1".
- Bank 1-RE register bits are set to all "0".
- Bank 1-RF register bits are set to all "0".

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator and TCC are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 6 input status changes (if ICWE is enabled)

Case 4 Comparator output status changes (if CMPWE is enabled)

[2] *VDD=5V, Setup time period = 16.5ms ± 30%.*
VDD=3V, Setup time period = 18ms ± 30%.

The first two cases (1 and 2) will cause the EM78P210N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3 and 4 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up. All sleep mode wake-up time is dependent on the oscillator mode, no matter what the oscillator type or mode is (except when it's in LXT2 mode). In LXT2 mode, wake-up time is 2~3 sec.

Although each of Cases 1 to 4 can be enabled, but not simultaneously, only one at a time can be enabled before entering sleep mode. That is**:**

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P210N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.6) for further details.

Case [b] If Port 6 Input Status Change is used to wake -up EM78P210N and ICWE bit of Bank 0-RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P210N can be awakened only with Case 3. Wake-up time is dependent on the oscillator mode. In RC mode (VDD: 5V, IRC: 4 MHz), wake-up time is 10 μs (for stable oscillators). In HXT2 mode (VDD: 5V, Crystal: 4 MHz, C1/C2: 30pF), wake-up time is 800 μs (for stable oscillators), and in LXT2 mode, wake-up time is 2~3 sec.

Case [c] If the Comparator output status change is used to wake-up the EM78P210N and the CMPWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P210N can be awakened only with Case 4.

Wake-up time is dependent on the oscillator mode. In RC mode (VDD: 5V, IRC: 4 MHz), wake-up time is 10 μs (for stable oscillators). In HXT2 mode (VDD: 5V, Crystal: 4 MHz, C1/C2: 30pF), wake-up time is 800 μs (for stable oscillators), and in LXT2 mode, wake-up time is 2~3 sec.

If Port 6 Input Status Change Interrupt is used to wake up the EM78P210N (as in Case b above), the following instructions must be executed before SLEP:

```
MOV           A, @000110xxb     ; Select WDT prescaler and disable WDT
BANK          1
MOV           RE, A
WDTC                            ; Clear WDT and prescaler
BANK          0
MOV           R6, R6            ; Read Port 6
ENI (or DISI)                   ; Enable (or disable) global interrupt
MOV           A, @xxx1xxxxb     ; Enable Port 6 input change wake-up bit
MOV           RE
MOV           A, @00000x1xb     ; Enable Port 6 input change interrupt
BANK          1
MOV           RF, A
SLEP                            ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P210N (as in Case [c] above), the following instructions must be executed before SLEP:

```
MOV           A, @xxx01xxxb   ; Select Comparator and P71 functions as
                              ; general I/O pin
BANK          1
MOV           RA, A
MOV           A, @000110xxb   ; Select WDT prescaler and Disable WDT
MOV           RE, A
WDTC                          ; Clear WDT and prescaler
ENI (or DISI)                 ; Enable (or disable) global interrupt
MOV           A, @00000100b   ; Enable comparator output status change
                              ; wake-up bit
BANK          0
MOV           RE, A
BANK          1
MOV           A, @0x00000001b ; Enable Comparator output status change
                              ; interrupt
MOV           RE, A
SLEP                          ; Sleep
```

6.5.1.1 Wake-up and Interrupt Modes Operation Summary

All categories under Reset, Wake-up and Interrupt modes are summarized below.

Wake-up Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
External interrupt	x	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Port 6 pin change	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable ICWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
TCC overflow interrupt	x	Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
Comparator interrupt	If enable CMPWE bit Wake-up + interrupt (if interrupt enable) + next instruction	If enable CMPWE bit Wake-up + interrupt (if interrupt enable) + next instruction	Interrupt (if interrupt enable) or next instruction	Interrupt (if interrupt enable) or next instruction
WDT Time out	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode
Low Voltage Reset	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode	Reset to Normal mode

After wake up:

1. If interrupt enable → interrupt+ next instruction
2. If interrupt disable → next instruction

The controller can be awakened from sleep and Idle mode. The wake-up signals are listed as follows:

Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
INT0 INT1	N/A	DISI + Bank 1-RF (EXIE) Bit 2 = 1	DISI + Bank 1-RF (EXIE) Bit 2 = 1	DISI + Bank 1-RF (EXIE) Bit 2 = 1
		Wake-up+ Next Instruction + Set Bank 0-RF (EX0IF)=1	Next Instruction+ Set Bank 0-RF (EX0IF) = 1 or Set Bank 0-RE (EX1IF)=1	Next Instruction+ Set Bank 0-RF (EX0IF) = 1 or Set Bank 0-RE (EX1IF)=1
		ENI + Bank 1-RF (EXIE) Bit 2 = 1	ENI + Bank 1-RF (EXIE) Bit 2 = 1	ENI + Bank 1-RF (EXIE) Bit 2 = 1
		Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (EX0IF) = 1
Port 6 Input Status Change	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1 = 0	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1=0	Bank 1-RF (ICIE) Bit 1 = 0	Bank 1-RF (ICIE) Bit 1 = 0
	Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Port 6 input status change interrupt is invalid	Port 6 input status change interrupt is invalid
	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1=1	Bank 0-RE (ICWE) Bit 4=0, Bank 1-RF (ICIE) Bit 1 = 1	N/A	N/A
	Set Bank 0-RF (ICIF) = 1, Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	Set Bank 0-RF (ICIF) = 1, Oscillator and TCC are stopped. Port 6 input status changed wake-up is invalid.	N/A	N/A
	Bank 0-RE (ICWE) Bit 4=1, Bank 1-RF (ICIE) Bit 1=0	Bank 0-RE (ICWE) Bit 4=1, Bank 1-RF (ICIE) Bit 1=0	N/A	N/A
	Wake-up+ Next Instruction Oscillator and TCC are stopped.	Wake-up+ Next Instruction Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (ICWE) Bit 4=1, DISI + Bank 1-RF (ICIE) Bit 1 = 1	Bank 0-RE (ICWE) Bit 4=1, DISI + Bank 1-RF (ICIE) Bit 1 = 1	DISI + Bank 1-RF (ICIE) Bit 1 = 1	DISI + Bank 1-RF (ICIE) Bit 1 = 1
	Wake-up+ Next Instruction+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Wake-up+ Next Instruction+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Next Instruction+ Set Bank 0-RF (ICIF) = 1	Next Instruction+ Set Bank 0-RF (ICIF) = 1
	Bank 0-RE (ICWE) Bit 4=1, ENI + Bank 1-RF (ICIE) Bit 1 = 1	Bank 0-RE (ICWE) Bit 4=1, ENI + Bank 1-RF (ICIE) Bit 1 = 1	ENI + Bank 1-RF (ICIE) Bit 1 = 1	ENI + Bank 1-RF (ICIE) Bit 1 = 1
	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1 Oscillator and TCC are stopped.	Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (ICIF) = 1
TCC Overflow	N/A	DISI + Bank 1-RF (TCIE) Bit 0 = 1	DISI + Bank 1-RF (TCIE) Bit 0 = 1	DISI + Bank 1-RF (TCIE) Bit 0 = 1
		Wake-up+ Next Instruction + Set Bank 0-RF (TCIF)=1	Next Instruction+ Set Bank 0-RF (TCIF) = 1	Next Instruction+ Set Bank 0-RF (TCIF) = 1
		ENI + Bank 1-RF (TCIE) Bit 0 = 1	ENI + Bank 1-RF (TCIE) Bit 0=1	ENI + Bank 1-RF (TCIE) Bit 0=1
		Wake-up+ Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1	Interrupt Vector (0x08)+ Set Bank 0-RF (TCIF) = 1

Signal	Sleep Mode	Idle Mode	Green Mode	Normal Mode
Comparator (Comparator Output Status Change)	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 0	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 0	Bank 1-RE (CMPIE) Bit 0 = 0	Bank 1-RE (CMPIE) Bit 0 = 0
	Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Comparator output status change interrupt is invalid.	Comparator output status change interrupt is invalid.
	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 1	Bank 0-RE (CMPWE) Bit 2 = 0 Bank 1-RE (CMPIE) Bit 0 = 1	N/A	N/A
	Set Bank 0-RE (CMPIF) = 1, Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	Set Bank 0-RE (CMPIF)=1, Comparator output status changed wake-up is invalid. Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (CMPWE) Bit 2 = 1, Bank 1-RE (CMPIE) Bit 0 = 0	Bank 0-RE (CMPWE) Bit 2 = 1, Bank 1-RE (CMPIE) Bit 0 = 0	N/A	N/A
	Wake-up+ Next Instruction, Oscillator and TCC are stopped.	Wake-up+ Next Instruction, Oscillator and TCC are stopped.	N/A	N/A
	Bank 0-RE (CMPWE) Bit 2 = 1, DISI + Bank 1-RE (CMPIE) Bit 0 =1	Bank 0-RE (CMPWE) Bit 2 = 1, DISI + Bank 1-RE (CMPIE) Bit 0 =1	DISI + Bank 1-RE (CMPIE) Bit 0 = 1	DISI + Bank 1-RE (CMPIE) Bit 0 = 1
	Wake-up+ Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 =1, Oscillator and TCC are stopped.	Wake-up+ Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 =1, Oscillator and TCC are stopped.	Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1	Next Instruction+ Set Bank 0-RE (CMPIF) Bit 0 = 1
	Bank 0-RE (CMPWE) Bit 2 = 1, ENI + Bank 1-RE (CMPIE) Bit 0 = 1	Bank 0-RE (CMPWE) Bit 2 = 1, ENI + Bank 1-RE (CMPIE) Bit 0 = 1	ENI + Bank 1-RE (CMPIE) Bit 0 = 1	ENI + Bank 1-RE (CMPIE) Bit 0 = 1
	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0- RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Wake-up+ Interrupt Vector (0x08)+ Set Bank 0- RE (CMPIF) Bit 0 = 1, Oscillator and TCC are stopped.	Interrupt Vector (0x08)+ Bank 0-RE (CMPIF) Bit 0 = 1	Interrupt Vector (0x08)+ Bank 0-RE (CMPIF) Bit 0 = 1
WDT Time-out Bank 1-RE (WDTE) Bit 7=1	Wake-up+ Reset (Address 0x00)	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)
Low Voltage Reset	Wake-up+ Reset (Address 0x00)	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)	Reset (Address 0x00)

6.5.1.2 Register Initial Values after Reset

The following table summarizes the registers initialized values.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (MSR)	Bit Name	-	-	-	-	-	-	BS1	BS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute the next instruction							
0x03	R3 (SR)	Bit Name	-	-	-	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 0-R5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 0-R6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 0-R7	Bit Name	P77	-	-	-	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	Bank 0-R8	Bit Name	-	-	NREN	-	-	-	P81	-
		Power-on	0	0	0	0	0	0	U	U
		/RESET & WDT	0	0	0	0	0	0	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9~ 0XD	Bank 0-R9~RD (Reserve)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 0-RE (WUCR)	Bit Name	EX1IF	-	-	ICWE	-	CMPWE	-	CMPIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xF	Bank 0-RF (ISR)	Bit Name	-	-	-	-	-	EX0IF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 1-R5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 1-R6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	Bank 1-R7	Bit Name	C77	-	-	-	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x8	Bank 1-R8 (IOPCR)	Bit Name	-	-	-	-	-	-	C81	-
		Power-on	0	0	0	0	0	0	1	1
		/RESET & WDT	0	0	0	0	0	0	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	Bank 1-R9 (Reserve)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xA	Bank 1-RA (CMPCON)	Bit Name	EIS1	EIS0	CMP OUT	CMP COS1	CMP COS0	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xB	Bank 1-RB (PDCR)	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xC	Bank 1-RC (ODCR)	Bit Name	/OD7	/OD6	/OD5	/OD4	/OD3	/OD2	/OD1	/OD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xD	Bank 1-RD (PHCR)	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xE	Bank 1-RE (WDTCR)	Bit Name	WDTE	-	PSWE	PSW2	PSW1	PSW0	-	CMPIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF	Bank 1-RF (IMR)	Bit Name	-	-	-	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 2-R5 (HDCR)	Bit Name	HD67	HD66	HD65	HD64	HD63	HD62	HD61	HD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 2-R6 (HSCR1)	Bit Name	HS57	HS56	HS55	HS54	HS53	HS52	HS51	HS50
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	Bank 2-R7 (HSCR2)	Bit Name	HS67	HS66	HS65	HS64	HS63	HS62	HS61	HS60
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	Bank 2-R8 (OMCR)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	U	1	1	1	U	U	U	U
		/RESET & WDT	P	1	1	1	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9 ~ 0xF	Bank 2-R9 (RF)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	Bank 3-R5 (TCC)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	Bank 3-R6 (IRC) (only for ICE)	Bit Name	C3	C2	C1	C0	RCM1	RCM0	-	-
		Power-on	1	1	1	1	1	1	U	U
		/RESET & WDT	1	1	1	1	1	1	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x07	Bank 3-R7 (only for ICE)	Bit Name	-	-	-	-	NRHL	NRE	LVR1	LVR0-
		Power-on	U	U	U	U	1	1	1	1
		/RESET & WDT	P	P	P	P	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x10 ~ 0x1F	R10 ~ R1F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x20 ~ 0x3F	Bank 0~1 R20 ~ R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: ***"x"*** *= not used* ***"P"*** *= previous value before reset*
"u" *= unknown or don't care* ***"t"*** *= check "Reset Type" Table in Section 6.5.2*

6.5.1.3 Controller Reset Block Diagram

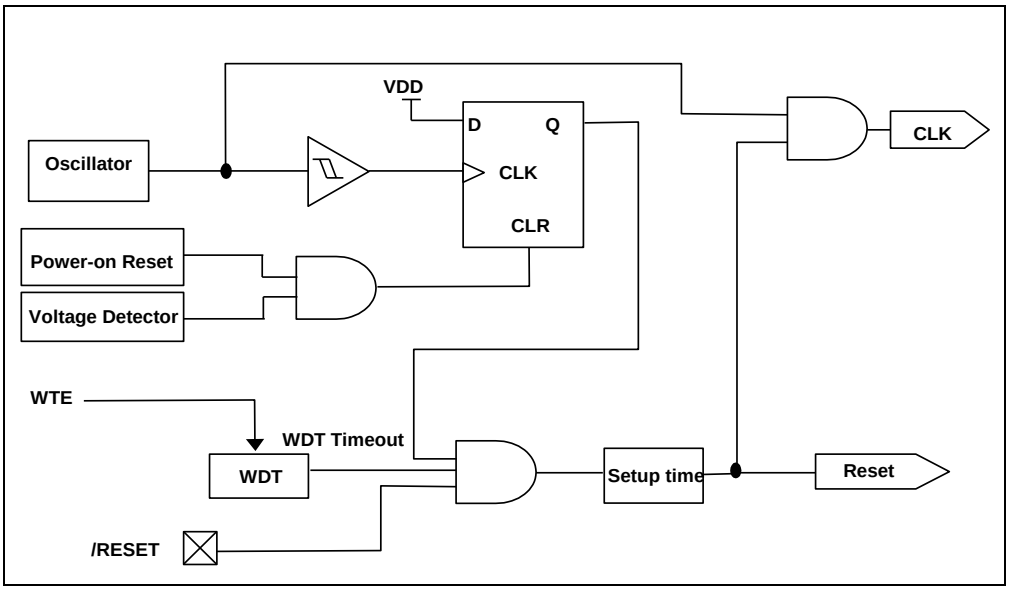


Figure 6-8 Controller Reset Block Diagram

6.5.2 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
LVR during Operating mode,	*P	*P
LVR wake-up during SLEEP mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* *P: Previous status before reset*

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

* *P: Previous value before reset*

6.6 Interrupt

The EM78P210N has four interrupts as listed below**:**

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External Interrupt INT0, INT1
4. When the Comparator output status changes

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Port 6 Input Status Change Interrupt will wake up the EM78P210N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When wake-up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the Interrupt Vector 008H.

The external interrupt has a built-in digital noise rejection circuit (if the input pulse is less than 8 system clock times, it is eliminated as noise. Edge selection is possible with /INT. Refer to Word 1 Bits 8~7 (Section 6.13.2, *Code Option Register (Word 1)*) for digital noise rejection definition.

During a power source unstable situation, like during external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. While Vdd is still unsettled, the supply voltage may be below the working voltage. When the system supply voltage Vdd is below the working voltage, the IC kernel must automatically keep all register status.

Bank 0-RE and Bank 0-RF are the interrupt status register that records the interrupt requests in the relative flags/bits. Bank 1-RE and Bank 1-RF are Interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in Bank 0-RE and Bank 0-RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

When interrupt mask bits are “Enabled”, the flag in the Interrupt Status Register (RF) is set regardless of the ENI execution. Note that the result of Bank 0-RE/RF will be the Logic AND of Bank 0-RE/RF and Bank 1-RE/RF (refer to Figure 6-8). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

When any interrupt occurs, the contents of ACC, R1 (Bits 5, 4, 1, 0), R3 (Bits 2 ~0), R4 registers are pushed to the corresponding stack (Figure 6-9). After the RETI instruction is executed, the contents of the corresponding stack are popped to ACC, R1 (Bits 5, 4, 1, 0), R3 (Bits 2 ~0), R4 registers.

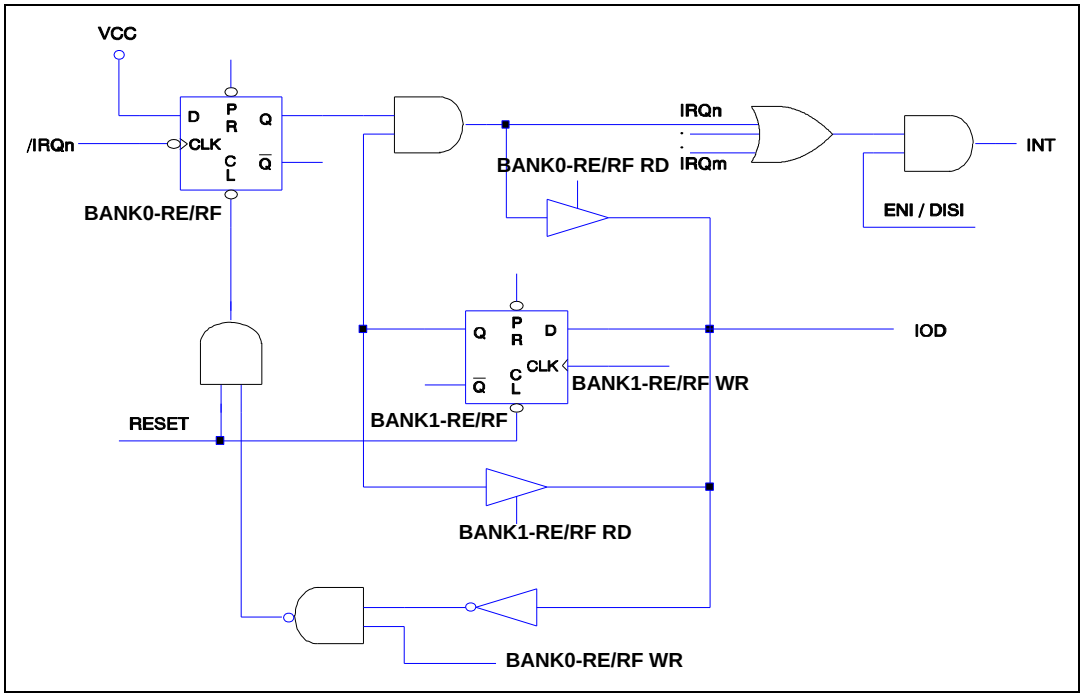


Figure 6-9 Interrupt Input Circuit

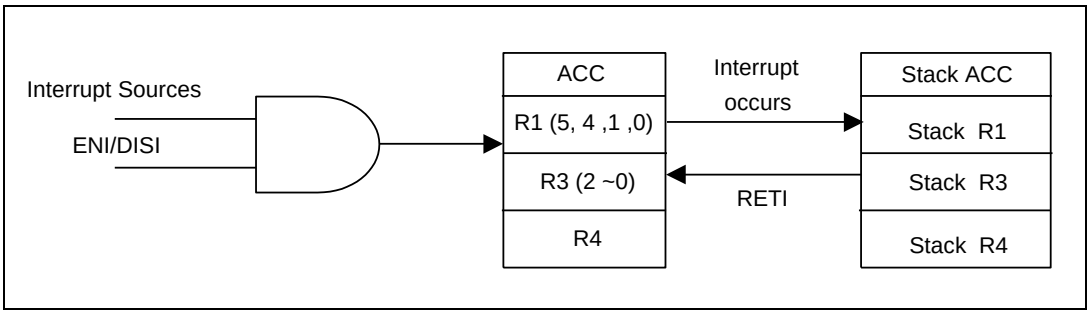


Figure 6-10 Interrupt Backup Diagram

6.7 Comparator

The EM78P210N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up the EM78P210N from sleep mode. The comparator circuit diagram is depicted in the figure below.

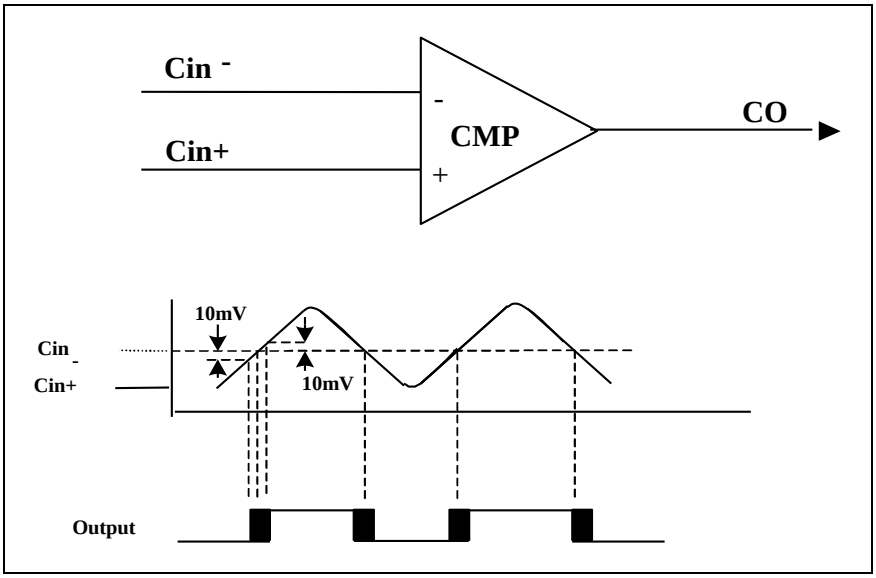


Figure 6-11 Comparator Circuit Diagram and Operating Mode

6.7.1 External Reference Signal

The analog signal presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.7.2 Comparator Outputs

- The compared result is stored in the CMPOUT of Bank 1-RA.
- Bits 3 ~ 4 <CMPCOS1, CMPCOS0> of the Bank 1-RA register. See Section 6.2.18, *Bank 1-RA (CMPCON: Comparator Control Register)* for Comparator select bits function description.

NOTE

- *The highest priority of P71/INT1/CO is INT1. When EIS1=0, the working type of P71/INT1/CO is determined by CMPCOS1 and CMPCOS2.*
- *The CO and P71 of the P71/CO pins cannot be used at the same time.*
- *The P71/CO pin priority is as follows:*

P71/INT1/CO Pin Priority		
High	Medium	Low
/INT1	CO	P71

The following figure shows the Comparator Output Block Diagram.

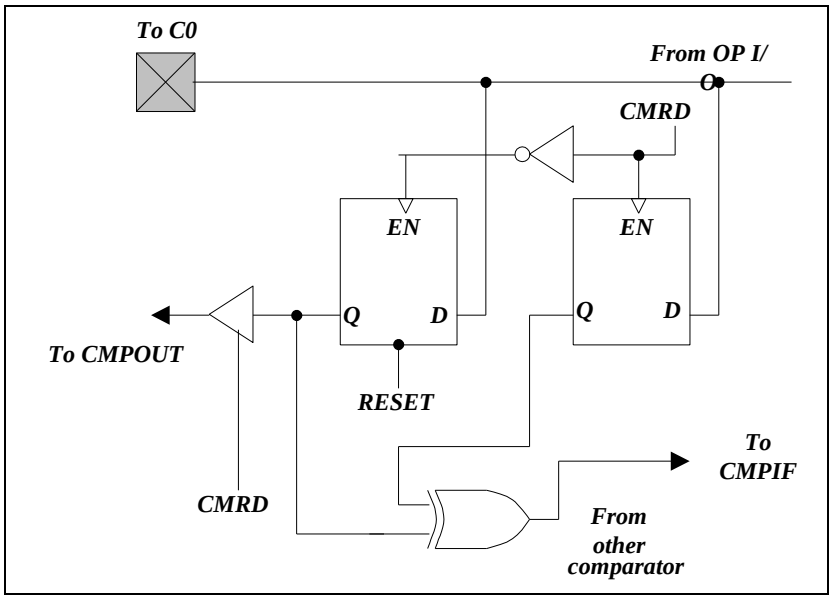


Figure 6-12 Comparator Output Configuration

6.7.3 Using a Comparator as an Operation Amplifier

6.7.3.1 Bank 0-RE (WUCR: Wake-up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EX1IF	0	0	ICWE	0	CMPWE	0	CMPIF

Bit 2 (CMPWE): Comparator wake-up enable bit

0 = Disable Comparator wake-up

1 = Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up the EM78P210N from sleep, the CMPWE bit must be set to “Enable”.

Bit 0 (CMPIF): Comparator Interrupt flag. Set when a change occurs in the Comparator output. Reset by software

6.7.3.2 Bank 1-RA (CMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EIS1	EIS0	CMPOUT	CMPCOS1	CMPCOS0	0	0	0

Bit 5 (CMPOUT): The result of the Comparator output

Bit 4 ~ Bit 3 (CMPCOS1 ~ CMPCOS0): Comparator Select bits

CMPCOS1	CMPCOS0	Function Description
0	0	Comparator is not used. P72, P73, and P71 are normal I/O pins
0	1	P72 and P73 are Comparator input pins and P71 is normal I/O pin
1	0	P72 and P73 are Comparator input pins and P71 is Comparator output pin (CO)
1	1	Used as OP and P71 is OP output pin (CO)

6.7.3.3 Bank 1-RE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	0	PSWE	PSW2	PSW1	PSW0	0	CMPIE

Bit 0 (CMPIE): CMPIF interrupt enable bit

0 = Disable CMPIF interrupt

1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter an interrupt vector or to enter the next instruction, the CMPIE bit must be set to “Enable”. But actually the comparator output must be read to latch the status at first. Then the comparator output is compared to this latch to produce the information of output status change.

6.7.4 Comparator Interrupt

- CMPIE must be enabled for the “ENI” instruction to take effect
- Interrupt is triggered whenever a change occurs on the comparator output pin
- The actual change on the pin can be determined by reading the Bit CMPOUT
- CMPIF the comparator interrupt flag, can only be cleared by software

6.7.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into sleep mode.

6.8 Oscillator

6.8.1 Oscillator Modes

The EM78P210N can be operated in six different oscillator modes, such as High Crystal oscillator mode (HXT 1, 2), Low Crystal oscillator mode (LXT 1, 2), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator (IRC). Select one of such modes by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P52/OSCO act as P52	0	0	0
ERC[1] (External RC oscillator mode); P52/OSCO act as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P52/OSCO act as P52	0	1	0
IRC[2] (Internal RC oscillator mode); P52/OSCO act as OSCO	0	1	1
LXT1[3] (Frequency range of XT mode is 1MHz~100kHz)	1	0	0
HXT1[3] (Frequency range of XT mode is 16MHz~6MHz)	1	0	1
LXT2[3] (Frequency range of XT mode is 32kHz)	1	1	0
HXT2[3] (Frequency range of XT mode is 6MHz~1MHz) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P53 is normal I/O pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT1, LXT2, HXT1 and HXT2 modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

The maximum operating frequency limit of the crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.1	4
	3.0	8
	4.5	16

6.8.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P210N can be driven by an external clock signal through the OSCO pin as illustrated below.

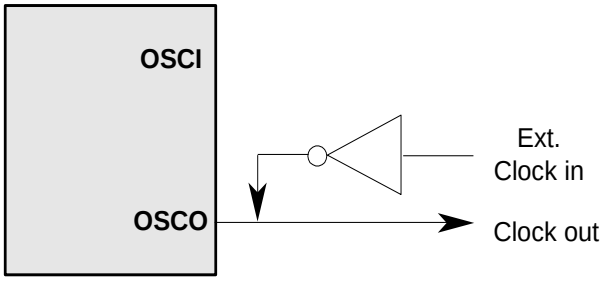


Figure 6-13 External Clock Input Circuit

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-17 below depicts such a circuit. The same applies to the HXT 1, 2 modes and the LXT 1, 2 modes.

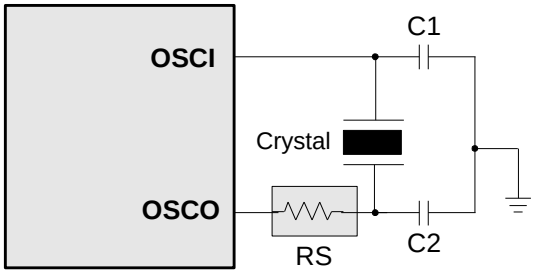


Figure 6-14 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode. Figure 6-13-1 is PCB layout suggestion. When the system works in Crystal mode (16 MHz), a 10 KΩ is connected between OSCI and OSCO.

Capacitor selection guide for crystal oscillator or ceramic resonators**:**

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT (100K~1 MHz)	100kHz	67pF	67pF
		200kHz	30pF	30pF
		455kHz	30pF	30pF
		1 MHz	30pF	30pF
	HXT (1~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	30pF	30pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	20pF	20pF
	LXT1 (100K~1 MHz)	100kHz	67pF	67pF
		200kHz	30pF	30pF
		455kHz	30pF	30pF
		1 MHz	30pF	30pF
	HXT2 (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	30pF	30pF
		6.0 MHz	30pF	30pF
	HXT1 (6~16 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF
		16.0 MHz	15pF	15pF

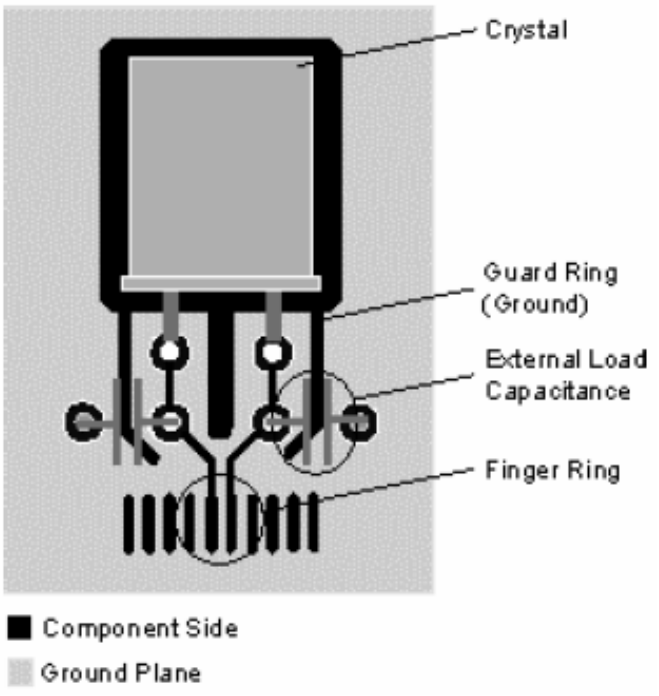


Figure 6-15 Parallel Mode Crystal/Resonator Circuit Diagram

6.8.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Figure 6-16) could offer a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

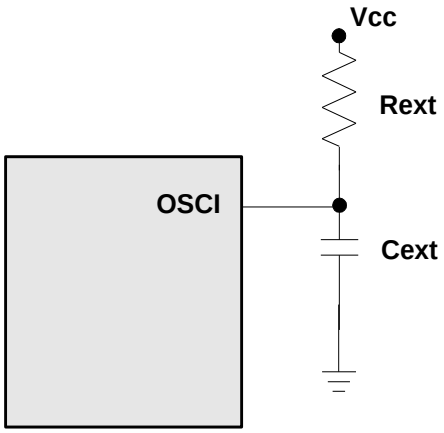


Figure 6-16 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and the value of Rext should not be greater than 1MΩ. If the frequency cannot be kept within this range, the frequency can be easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot discharge the capacitance current correctly.

Based on the above reasons, it must be kept in mind that all the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB is layout, have certain effect on the system frequency.

The RC Oscillator frequencies**:**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: *[1]: Measured based on DIP packages.*

[2]: The values are for design reference only.

[3]: The frequency drift is ± 30%

6.8.4 Internal RC Oscillator Mode

The EM78P210N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (1 MHz, 16 MHz, and 455kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P210N internal RC drift with the variations on voltage, temperature, and process.

Internal RC Drift Rate (Ta=25°C, VDD=5.0V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.1V~5.5V)	Process	Total
4 MHz	± 5%	± 5%	± 4%	±14%
16 MHz	± 5%	± 5%	± 4%	±14%
1 MHz	± 5%	± 5%	± 4%	±14%
455kHz	± 5%	± 5%	± 4%	±14%

Theoretical values are for reference only. Actual values may vary depending on actual process.

6.9 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes to a steady state. EM78P210N has a built-in Power-on Voltage Detector (POVD) with detection level range of 1.7V to 1.9V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.9.1 External Power-on Reset Circuit

The circuit shown in the figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Since the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. This way, the voltage at Pin /Reset is held below 0.2V. The diode (D) functions as a short circuit at power-down. The "C" capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

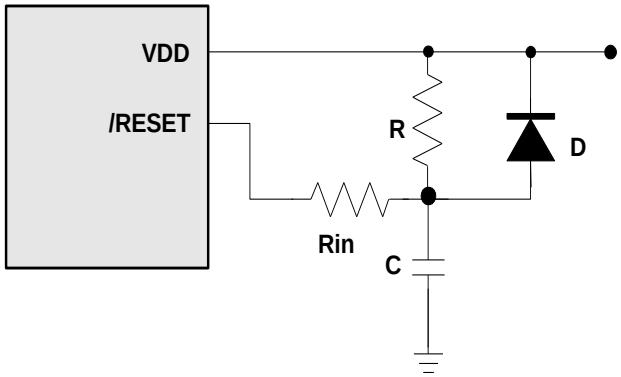


Figure 6-17 External Power on Reset Circuit

6.9.2 Residual Voltage Protection

When the battery is replaced, device power Vdd is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-16 and Figure 6-17 show how to create a protection circuit against residual voltage.

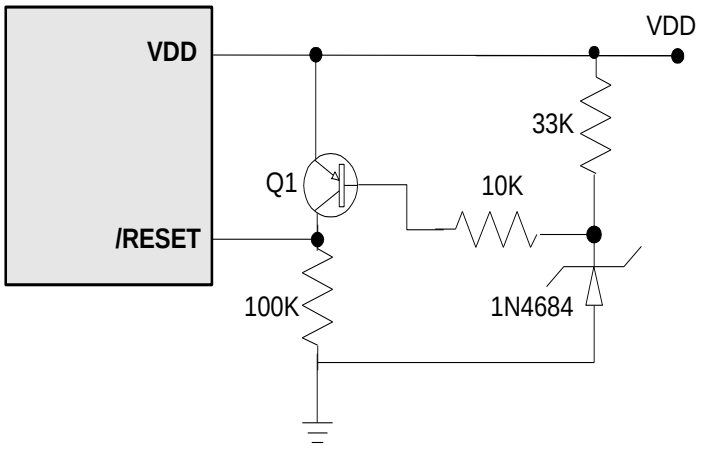


Figure 6-18 Residual Voltage Protection Circuit 1

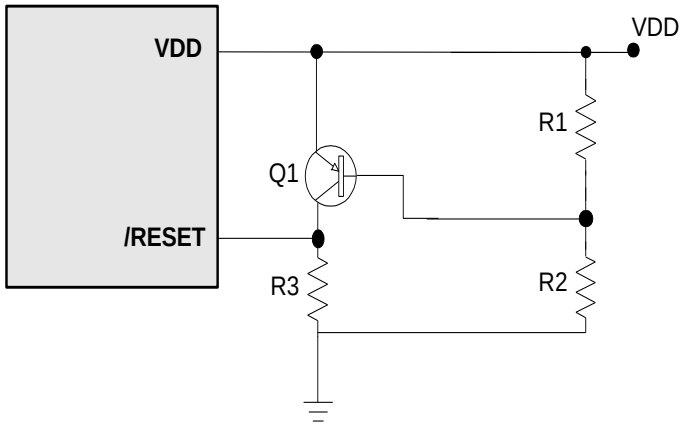


Figure 6-19 Residual Voltage Protection Circuit 2

6.10 Low Voltage Reset

The low voltage reset (LVR) is designed for unstable power situation, such as external power noise interference or in EMS test condition.

When LVR is enabled, system supply voltage (Vdd) drops below Vdd reset level (V_{RESET}) and remains 10us, the system reset will occur and the system will keep on reset status. The system will remain at reset status until Vdd voltage rises above Vdd release level. Refer to Figure 6-20.

LVR property is set at Code Option Word 0, Bits 10 and 9. Detailed operation mode is as follows:

Word 0												
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TYPE1	TYPE0	LVR1	LVR0	CLKS	ENWDTB	OSC2	OSC1	OSC0	-	Protect		

Bits 10~9 (LVR1 ~ LVR0): Low Voltage Reset Enable bits. If Vdd has a crossover at Vdd reset level as Vdd changes, the system will be reset.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.5V	2.7V
01	3.0V	3.2V
00	4.0V	4.2V

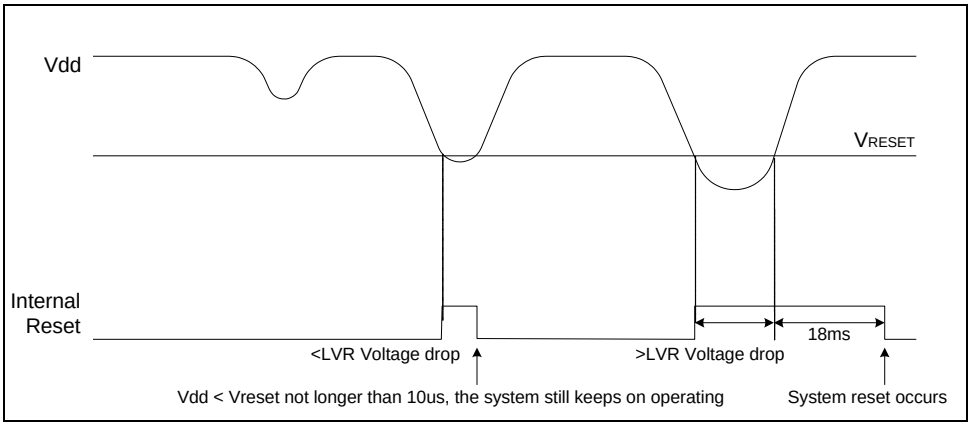


Figure 6-20 LVR Waveform Situation

6.11 Code Option

EM78P210N has two Code Option Words and one Customer ID word that are not a part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.11.1 Code Option Register (Word 0)

Word 0													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	TYPE1	TYPE0	LVR1	LVR0	CLKS	ENWDTB	OSC2	OSC1	OSC0	–	Protect		
1	High	High	High	High	4clocks	Disable	High	High	High	–	Disable		
0	Low	Low	Low	Low	2clocks	Enable	Low	Low	Low	–	Enable		

Bits 12 ~ 11 (TYPE1, TYPE0): Type selection for EM78P210N

TYPE1, TYPE0	MCU Type
00	Not used
01	EM78P210N-20Pin
10	EM78P210N-24Pin
11	Not used

NOTE
TYPE1, TYPE0, LVR1 and LVR0 are at Bank 3-R7, when using ICE.

Bits 10 ~ 9 (LVR1 ~ LVR0): Low Voltage Reset control bits

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (default)	
10	2.5V	2.7V
01	3.0V	3.2V
00	4.0V	4.2V

Bit 8 (CLKS): Instruction time period option bit

0 = two oscillator time periods

1 = four oscillator time periods **(Default)**

Refer to Section 6.12 for Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0 = Enable

1 = Disable (default)

Bits 6, 5 and 4 (OSC2, OSC1 and OSC0): Oscillator Mode Selection bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P52/OSCO act as P52	0	0	0
ERC[1] (External RC oscillator mode); P52/OSCO act as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P52/OSCO act as P52	0	1	0
IRC[2] (Internal RC oscillator mode); P52/OSCO act as OSCO	0	1	1
LXT1[3] (Frequency range of XT mode is 1MHz~100kHz)	1	0	0
HXT1[3] (Frequency range of XT mode is 16MHz~6MHz)	1	0	1
LXT2[3] (Frequency range of XT mode is 32kHz)	1	1	0
HXT2[3] (Frequency range of XT mode is 6MHz~1MHz) (default)	1	1	1

[1] *In ERC mode, OSCI is used as oscillator pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.*

[2] *In IRC mode, P53 is normal I/O pin. OSCO/P52 is defined by code option Word 0 Bit 6 ~ Bit 4.*

[3] *In LXT1, LXT2, HXT1 and HXT2 modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.*

Bit 3: Not used (Reserved). This bit is set to 0 all the time

Bits 2 ~ 0 (Protect**):** Protect Bits. Each protect status is as follows:

Protect Bits	Protect
0	Enable
1	Disable **(Default)**

6.11.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	–	RESETENB	RCOUT	NRHL	NRE	–	C3	C2	C1	C0	RCM1	RCM0
1	–	–	P81	System_clk	32/fc	Enable	–	High	High	High	High	High	High
0	–	–	/RESET	Open_drain	8/fc	Disable	–	Low	Low	Low	Low	Low	Low

Bit 12: Not used (reserved), fixed to “1” all the time.

Bit 11: Not used (reserved), fixed to “0” all the time.

Bit 10 (RESETENB): P81/RESET pin select bit

0 = P81 set to /RESET pin

1 = P81 is general purpose input pin or open drain for output port **(Default)**

Bit 9 (RCOUT): System clock output enable bit in IRC or ERC mode

0 = OSCO pin is open drain

1 = OSCO output instruction clock **(Default)**

Bit 8 (NRHL): Noise rejection high/low pulse define bit. INT pin has a falling edge trigger.

0 = Pulses equal to 8/fc is regarded as signal

1 = Pulses equal to 32/fc is regarded as signal **(Default)**

NOTE
NRHL and NRE are at Bank 3-R7, when using ICE.

Bit 7 (NRE): Noise rejection enable

0 = disable noise rejection

1 = enable noise rejection (default). However in Low Crystal oscillator (LXT2) mode, the noise rejection circuit is always disabled.

NOTE
The noise rejection function is turned off in LXT2 and sleep mode.

Bit 6: Not used (Reserved). This bit is set to "1" all the time.

NOTE
C3, C2, C1, C0, RCM1 and RCM0 are at Bank 3-R6, when using ICE.

Bits 5~2 (C3~C0): Internal RC mode Calibration bits. These bits must always be set to "1" only (auto calibration)

Bit 1 and Bit 0 (RCM1 and RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 **(Default)**
1	0	16
0	1	1
0	0	455kHz

6.11.3 Customer ID Register (Word 2)

Word 2													
Bit	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Mnemonic	–	NRM	–	–	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
1	–	MOD1	–	–	High	High	High	High	High	High	High	High	High
0	–	MOD2	–	–	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12: Not used (reserved), fixed to "0" all the time

Bit 11 (NRM):

0 = Noise reject Mode 2. For multi-time circuit use, such as key scan and LED output.

1 = Noise reject Mode 1. For General input or output use. **(Default)**

Bits 10~9: Not used (reserved), fixed to "1" all the time

Bits 8 ~ 0: Customer's ID code

6.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator time periods). Note the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, these instructions only need one instruction cycles

In addition, the instruction set has the following features**:**

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

b *= Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[1]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[2]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → SP, (lower 10 bits of k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(lower 10 bits of k) → PC	None

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1110 1001 kkkk	1E9k	BANK k	k → R1 (1:0)	None
1 1110 1010 kkkk k kkkk kkkk kkkk	1EAk	LCALL k	Next instruction: k kkkk kkkk kkkk; PC+1 → [SP], k → PC	None
1 1110 1011 kkkk k kkkk kkkk kkkk	1EBk	LJMP k	Next instruction: k kkkk kkkk kkkk; k → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: *[1] This instruction is not recommended for RF operation*

[2] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	850	F±30%	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.75	–	V
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.25	–	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–1.0	0	1.0	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	3.75	–	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	1.5	–	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	–	1.9	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	1.2	–	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	–	3.75	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	–	1.25	–	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.75	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.25	–	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = 0.9VDD	–	-9	–	mA
IOH2	Output High Voltage (Ports 6)	VOH = 0.7VDD	–	-27	–	mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = 0.1VDD	–	16.8	–	mA
IOL2	Output Low Voltage (Ports 5, 6)	VOL = 0.3VDD	–	67.2	–	mA
LVR1	Low voltage reset level	Ta = 25℃	2.21	2.5	2.79	V
		Ta = -40 ~ 85℃	1.94	2.5	3.05	V
LVR2		Ta = 25℃	2.6	3.0	3.42	V
		Ta = -40 ~ 85℃	2.23	3.0	3.75	V
LVR3		Ta = 25℃	3.56	4.0	4.43	V
		Ta = -40 ~ 85℃	3.16	4.0	4.81	V
IPH	Pull-high current (Ports 50~53, 64~67)	Pull-high active, input pin at VSS	50	–	90	μA
IPL	Pull-low current (Ports 60~67)	Pull-low active, input pin at Vdd	20	–	60	μA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled, LVR disabled	–	2	–	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled, LVR disabled	–	10	–	μA
ISB3	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled LVR enabled	–	4.0	–	μA
ICC1	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled, LVR disabled	–	15	20	μA
ICC2	Operating supply current at two clocks (VDD=3V)	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled, LVR disabled	–	15	25	μA
ICC3	Operating supply current at two clocks (VDD=5V)	/RESET= 'High', Fosc = 4 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled, LVR disabled	–	1.5	1.7	mA
ICC4	Operating supply current at two clocks (VDD=5V)	/RESET= 'High', Fosc = 10 MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled, LVR disabled	–	2.8	3.0	mA

Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25℃	5V	3.84 MHz	4 MHz	4.16 MHz
16 MHz	25℃	5V	15.36 MHz	16 MHz	16.64 MHz
1 MHz	25℃	5V	0.96 MHz	1 MHz	1.04 MHz
455kHz	25℃	5V	436.8kHz	455kHz	473.2kHz

Internal RC Electrical Characteristics (Ta=-40 ~85°C, VDD=2.1~5.5 V, VSS=0V)

Internal RC	Drift Rate				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40℃~85℃	2.1V~5.5V	3.44 MHz	4 MHz	4.56 MHz
16 MHz	-40℃~85℃	2.1V~5.5V	13.76 MHz	16 MHz	18.24 MHz
1 MHz	-40℃~85℃	2.1V~5.5V	0.86 MHz	1 MHz	1.14 MHz
455kHz	-40℃~85℃	2.1V~5.5V	391.3kHz	455kHz	518.7kHz

8.1 Comparator (OP) Characteristics

Vdd = 5.0V, Vss=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOS	Input offset voltage	RL = 5.1K (Note[1])	–	–	10	mV
Vcm	Input common-mode voltages range	(Note [2])	GND	–	VDD-1	V
IOS	Input offset current	–	–	–	50	nA
IBS	Input bias current	–	–	25	250	nA
ICO	Comparator Supply current	–	–	300	–	μA
TRS	Response time	VREF=1.4V,VRL = 5V, RL = 5.1k, CL=15p, (Note [3])	0.5	1.3	3.5	μs
TLRS	Large signal response time	VRL = 5V, RL = 5.1k	–	300	–	ns
IOL	Output sink current	Vi(-) =1V, Vi(+) =0V, Vo = GND+0.5V	–	12	–	mA
VSAT	Saturation voltage	Vi(-) =1V, Vi(+) =0V, IOL ≤ 4mA	–	0.2	0.4	V
VS	Operating range	–	2.5	–	5.5	V

Note: *[1]. The output voltage is in the unit gain circuitry and over the full input common-mode range.*
[2]. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is VDD-1.
[3]. The response time specified is a 100mV input step with 5mV overdrive.

9 AC Electrical Characteristics

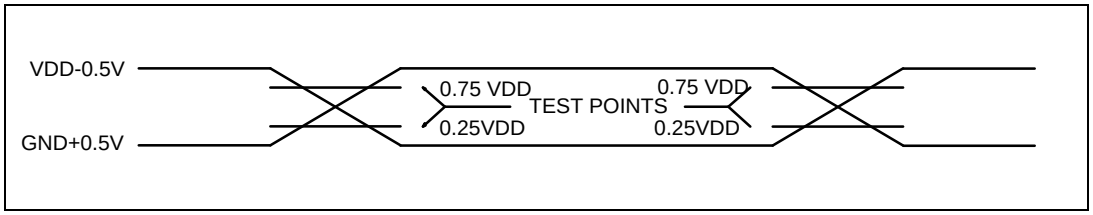
Ta=25°C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20) × N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25℃	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25℃	2000	–	–	ns
Twdt	Watchdog timer duration	Ta = 25℃	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25℃	1	3	5	ns

Note: * N = selected prescaler ratio

10 Timing Diagrams

AC Test Input/Output Waveform



Note: *AC Testing: Input is driven at VDD-0.5V for Logic "**1**", and GND+0.5V for Logic "**0**"*
*Timing measurements are made at 0.75V for Logic "**1**", and 0.25VDD for Logic "**0**"*

Figure 10-1a AC Test Input/Output Waveform Timing Diagram

Reset Timing (CLK = "0")

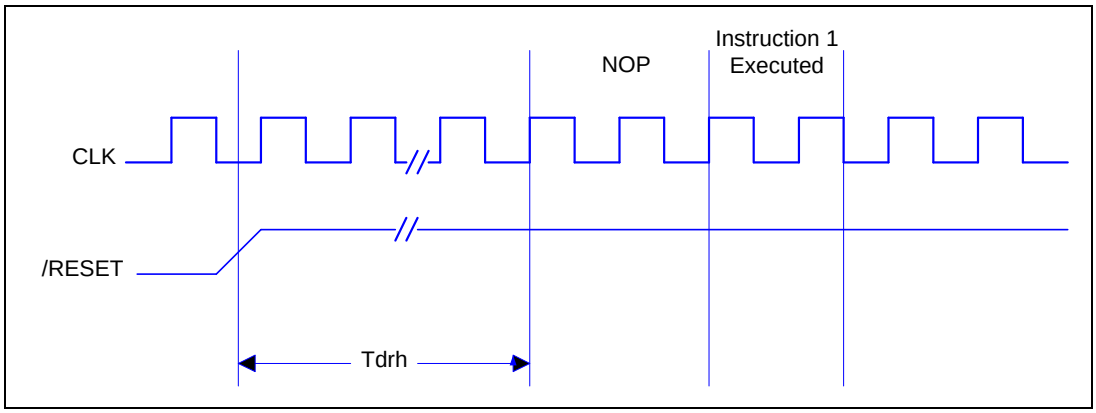


Figure 10-1b Reset Timing Diagram

TCC Input Timing (CLKS = "0")

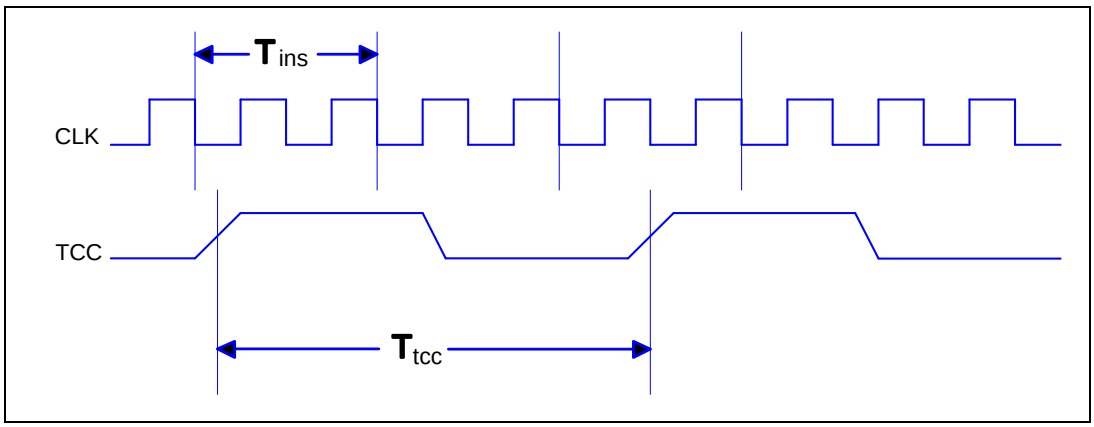
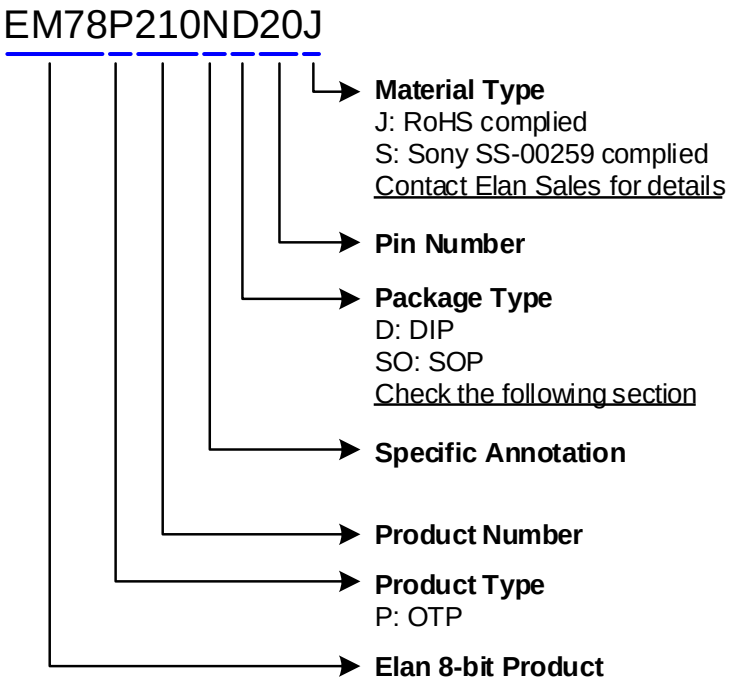


Figure 10-1c TCC Input Timing Diagram

APPENDIX

A Ordering and Manufacturing Information

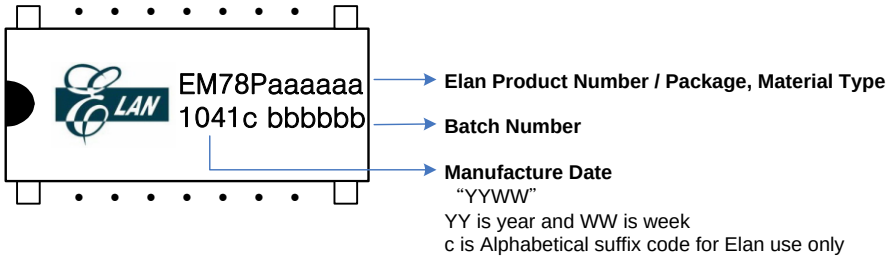


For example:

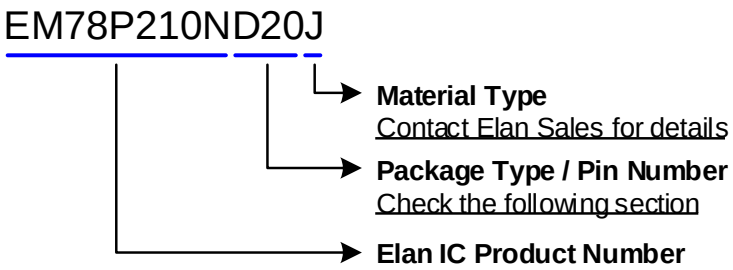
EM78P210NSO20S

is EM78P210N with OTP program memory product,
in 20-pin SOP 300mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

OTP MCU	Package Type	Pin Count	Package Size
EM78P210ND20	DIP	20 pins	300 mil
EM78P210NSO20	SOP	20 pins	300 mil
EM78P210NSS20	SSOP	20 pins	209 mil
EM78P210NK24	Skinny DIP	24 pins	300 mil
EM78P210NSO24	SOP	24 pins	300 mil
EM78P210NSS24A	SSOP	24 pins	209 mil

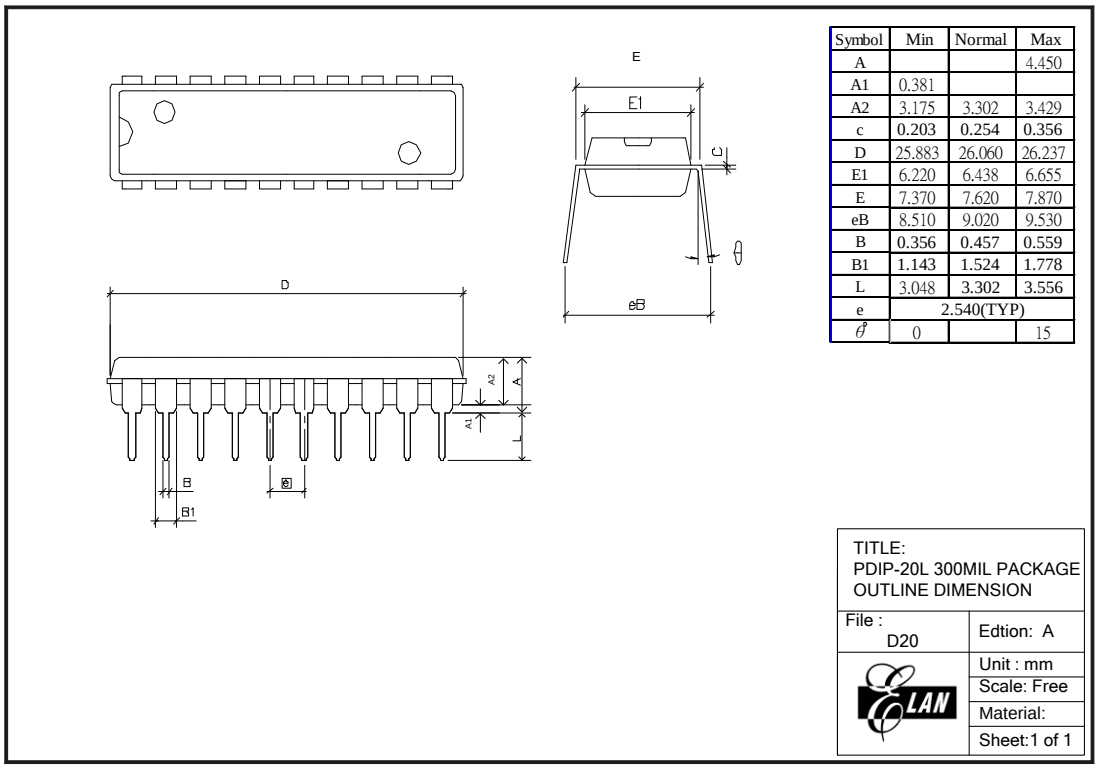
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb contents less is than 100 ppm and complies with Sony specifications.

Part No.	EM78P210NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Packaging Configurations

C.1 EM78P210ND20

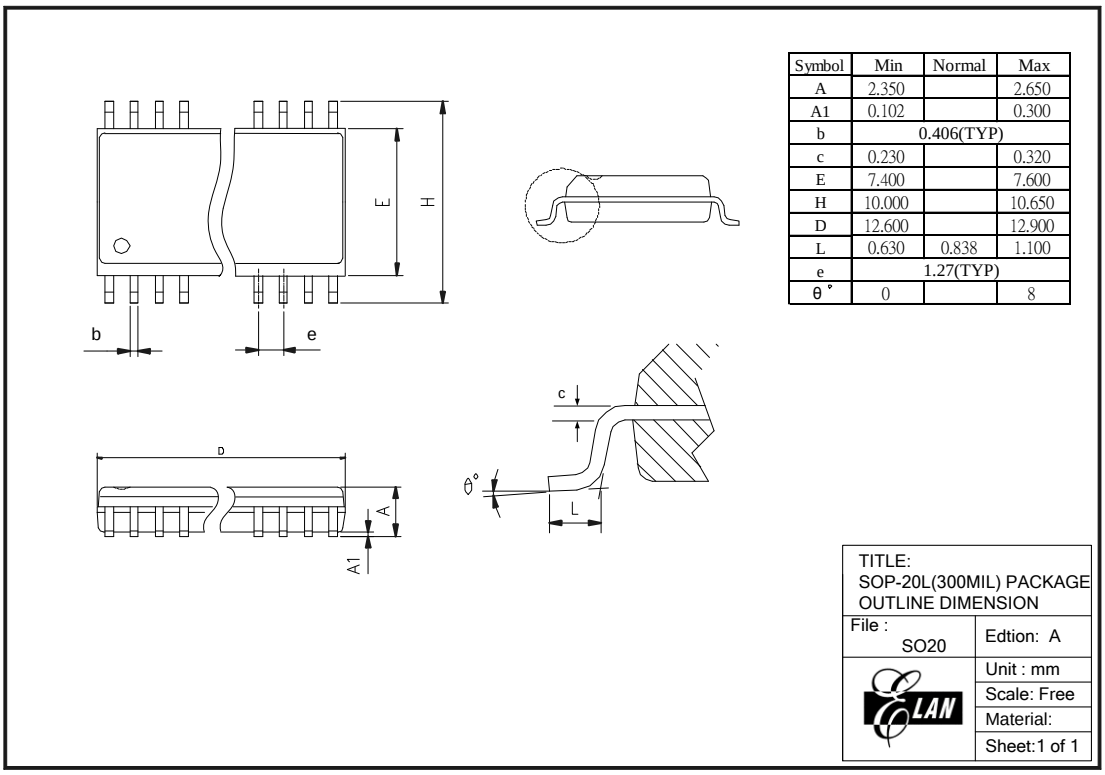


Symbol	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

TITLE: PDIP-20L 300MIL PACKAGE OUTLINE DIMENSION	
File : D20	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1 EM78P210N 20-pin PDIP Package Type

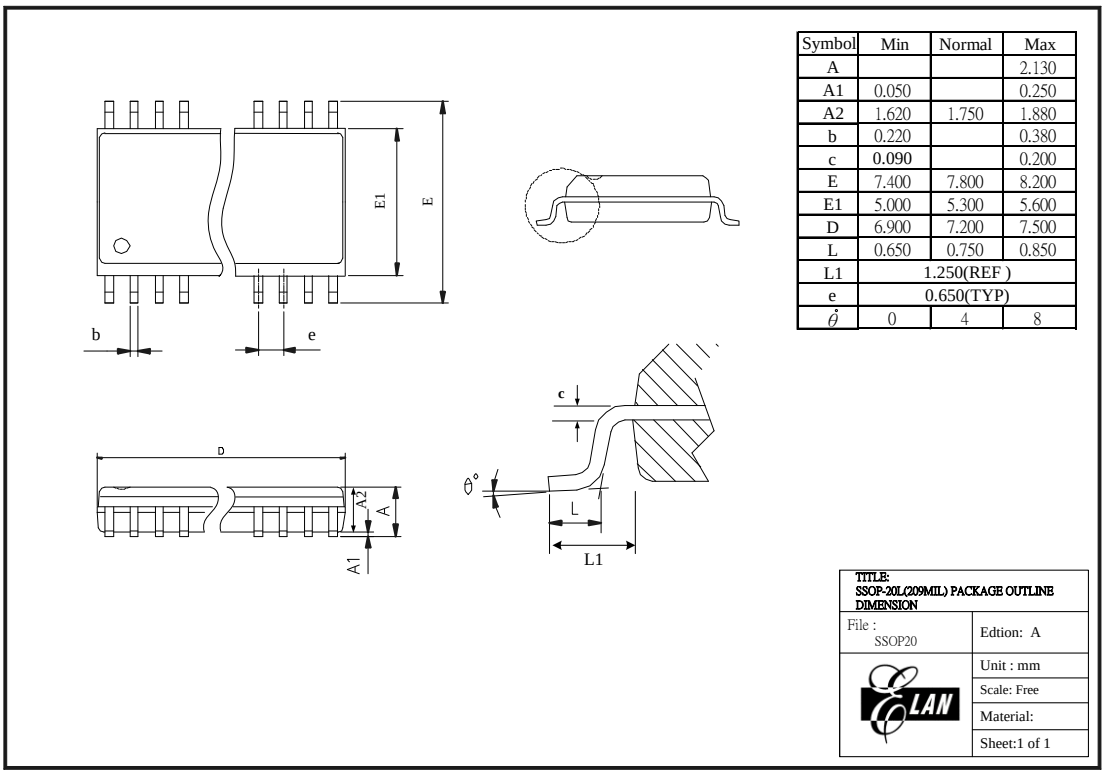
C.2 EM78P210NSO20



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

Figure C-2 EM78P210N 20-pin SOP Package Type

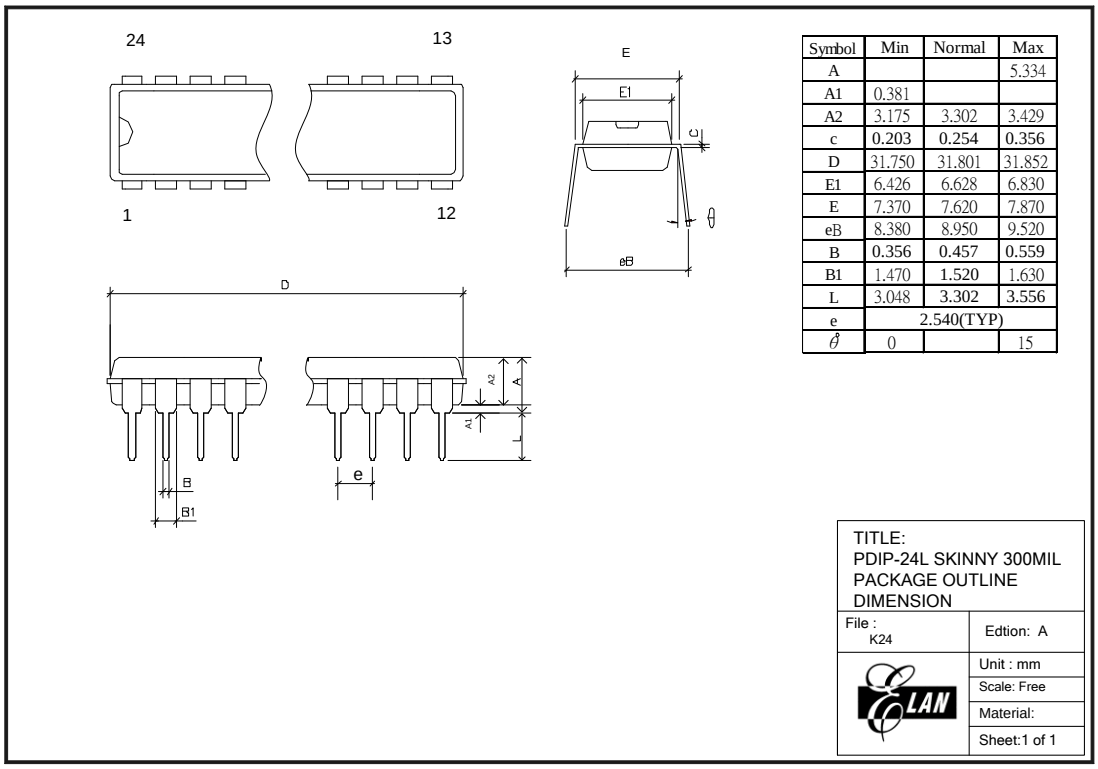
C.3 EM78P210NSS20



Symbol	Min	Normal	Max
A			2.130
A1	0.050		0.250
A2	1.620	1.750	1.880
b	0.220		0.380
c	0.090		0.200
E	7.400	7.800	8.200
E1	5.000	5.300	5.600
D	6.900	7.200	7.500
L	0.650	0.750	0.850
L1	1.250(REF)		
e	0.650(TYP)		
θ	0	4	8

Figure C-3 EM78P210N 20-pin SSOP Package Type

C.4 EM78P210NK24



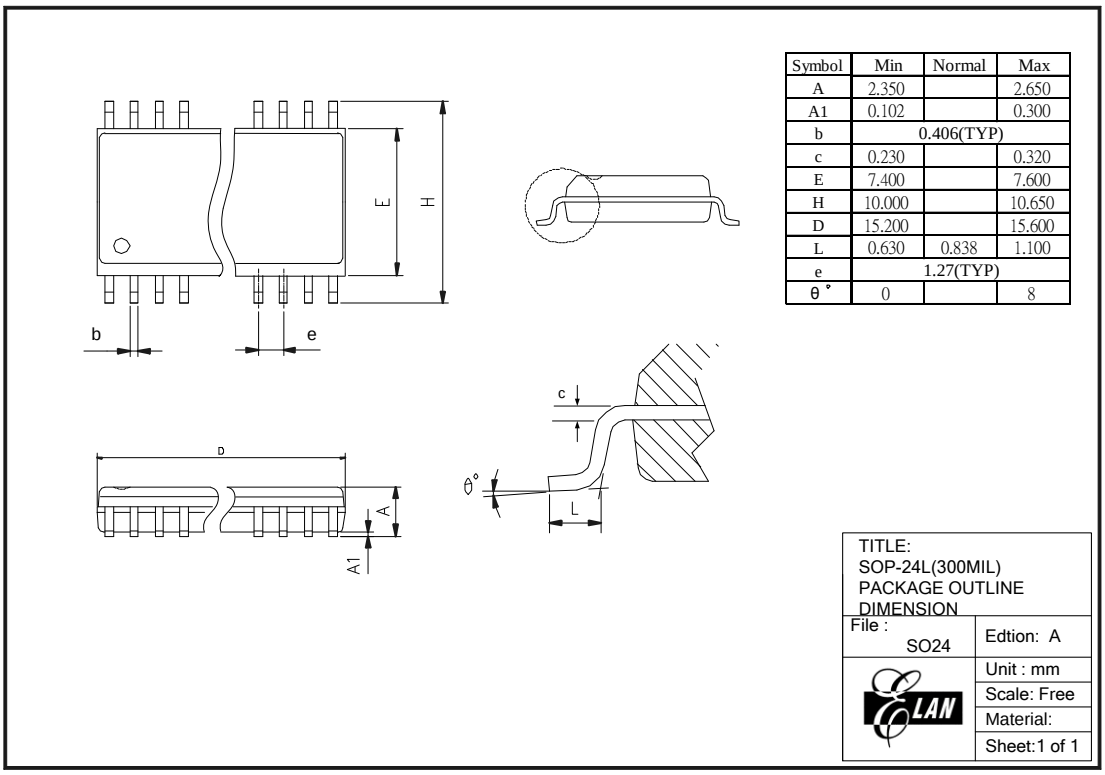
Symbol	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	31.750	31.801	31.852
E1	6.426	6.628	6.830
E	7.370	7.620	7.870
eB	8.380	8.950	9.520
B	0.356	0.457	0.559
B1	1.470	1.520	1.630
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE:
PDIP-24L SKINNY 300MIL
PACKAGE OUTLINE
DIMENSION

File : K24 | Edtion: A
Unit : mm
Scale: Free
Material:
Sheet:1 of 1

Figure C-4 EM78P210N 24-pin Skinny DIP Package Type

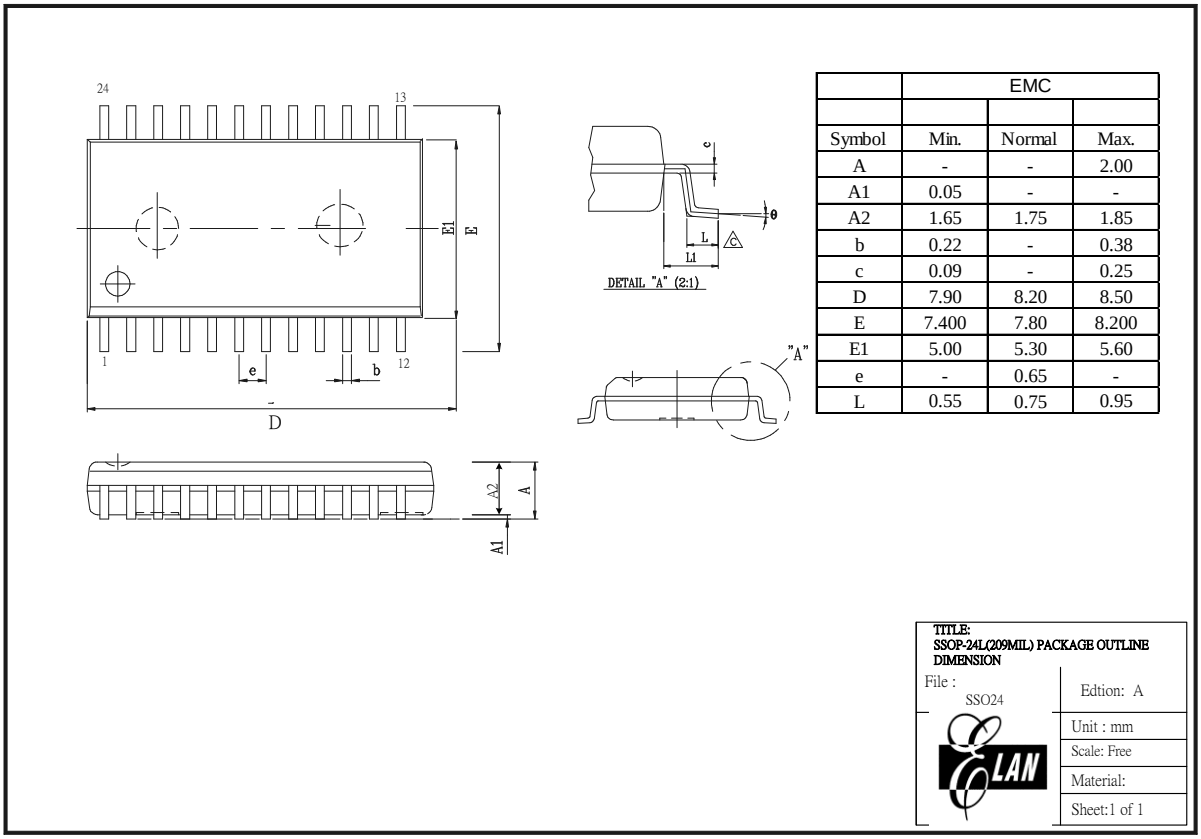
C.5 EM78P210NSO24



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

Figure C-5 EM78P210N 24-pin SOP Package Type

C.6 EM78P210NSS24A



	EMC		
Symbol	Min.	Normal	Max.
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	7.90	8.20	8.50
E	7.400	7.80	8.200
E1	5.00	5.30	5.60
e	-	0.65	-
L	0.55	0.75	0.95

Figure C-6 EM78P210N 24-pin SSOP Package Type

D Quality Assurance and Reliability

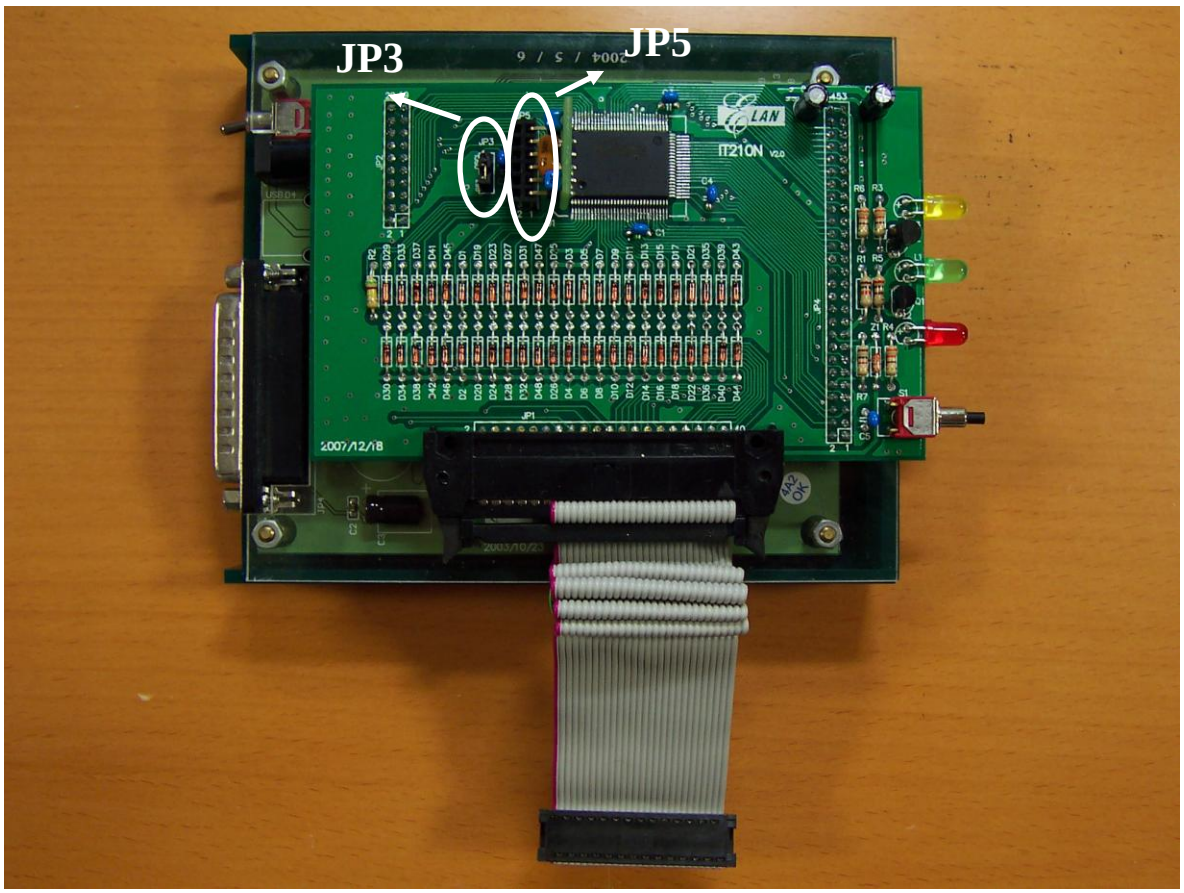
Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5℃, for 5 seconds up to the stopper using a rosin-type flux	
Pre-condition	Step 1: TCT, 65℃ (15 mins)~150℃ (15 mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125℃, TD (endurance)=24 hrs	
	Step 3: Soak at 30℃/60% , D (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness: 2.5mm or Pkg volume: 350mm^3 ----225±5°C) (Pkg thickness: 2.5mm or Pkg volume: 350mm^3 ----240±5°C)	
Temperature cycle test	-65℃ (15 mins) ~ 150℃ (15 mins), 200 cycles	
Pressure cooker test	TA =121℃, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	
High temperature / High humidity test	TA=85℃, RH=85% , TD (endurance)=168, 500 hrs	
High-temperature storage life	TA=150℃, TD (endurance)=500, 1000 hrs	
High-temperature operating life	TA=125℃, VCC=Max. operating voltage, TD (endurance) =168, 500, 1000 hrs	
Latch-up	TA=25℃, VCC=Max. operating voltage, 150mA/20V	
ESD (HBM)	TA=25℃, ± 3KV	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25℃, ± 300V	

D.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.

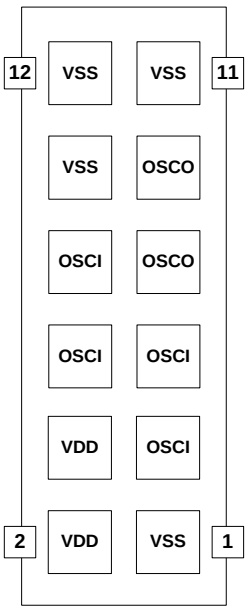
E How to Use the ICE210N

ICE210N for EM78P210N



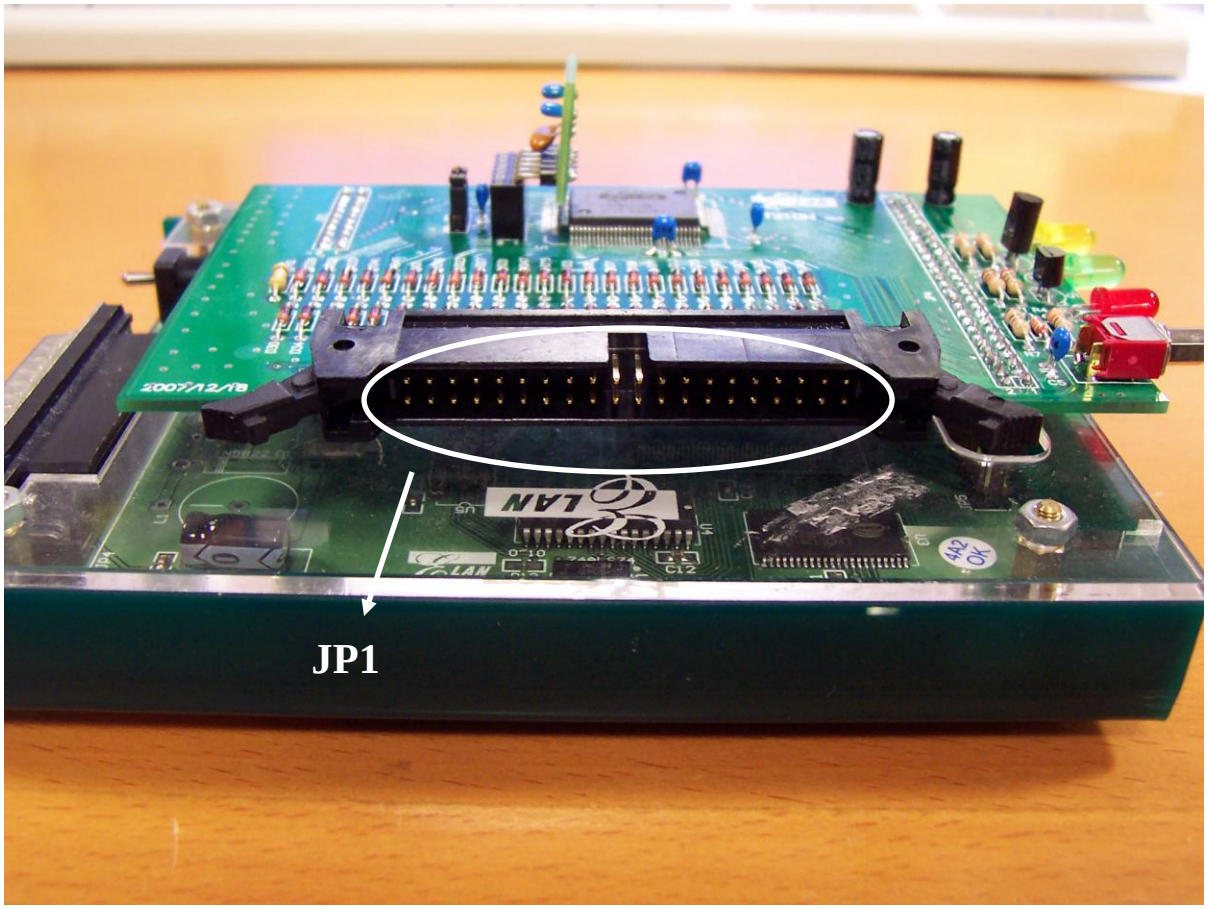
JP3	P53/OSCI Pin Select
OSCI P53	Crystal, ERC (OSCI)
OSCI P53	I/O Port (P53)

JP5

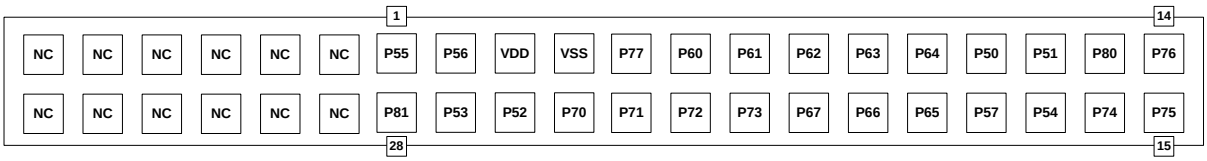


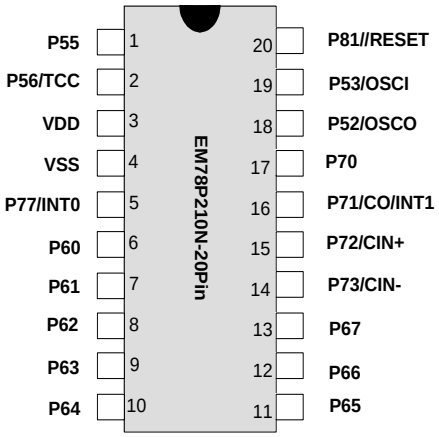
Oscillator Crystal, ERC Modes select **Crystal (OSCI)**

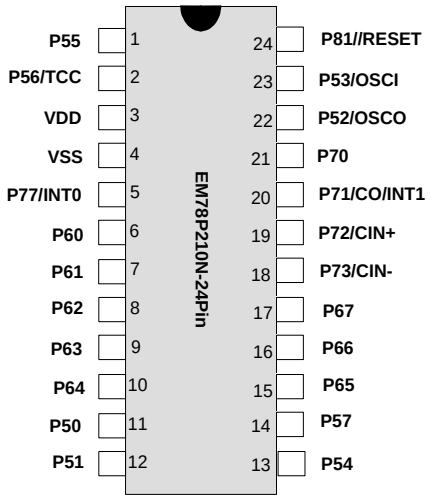
Oscillator IRC Modes select **I/O Port (P53)**

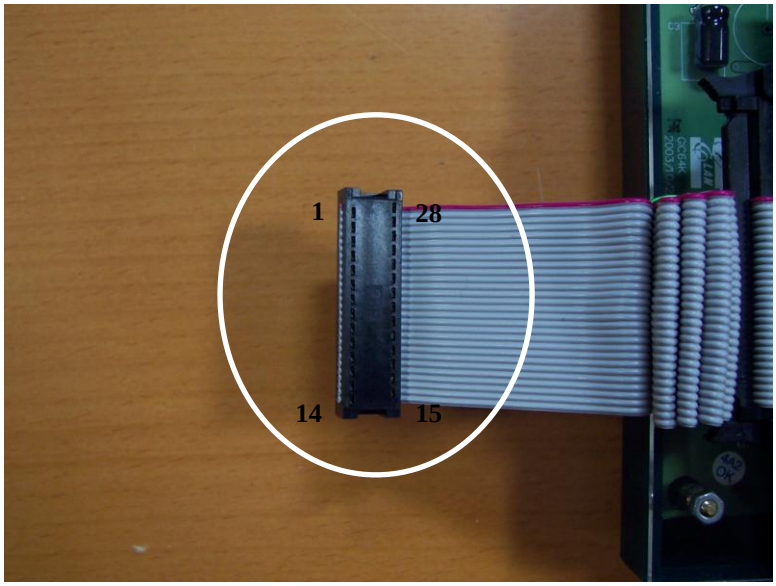

JP1

JP1


1
14
NC NC NC NC NC NC P55 P56 VDD VSS P77 P60 P61 P62 P63 P64 P50 P51 P80 P76
NC NC NC NC NC NC P81 P53 P52 P70 P71 P72 P73 P67 P66 P65 P57 P54 P74 P75
28
15


EM78P210N-20Pin
P55 1
P56/TCC 2
VDD 3
VSS 4
P77/INT0 5
P60 6
P61 7
P62 8
P63 9
P64 10
20 P81//RESET
19 P53/OSCI
18 P52/OSCO
17 P70
16 P71/CO/INT1
15 P72/CIN+
14 P73/CIN-
13 P67
12 P66
11 P65


EM78P210N-24Pin
P55 1
P56/TCC 2
VDD 3
VSS 4
P77/INT0 5
P60 6
P61 7
P62 8
P63 9
P64 10
P50 11
P51 12
24 P81//RESET
23 P53/OSCI
22 P52/OSCO
21 P70
20 P71/CO/INT1
19 P72/CIN+
18 P73/CIN-
17 P67
16 P66
15 P65
14 P57
13 P54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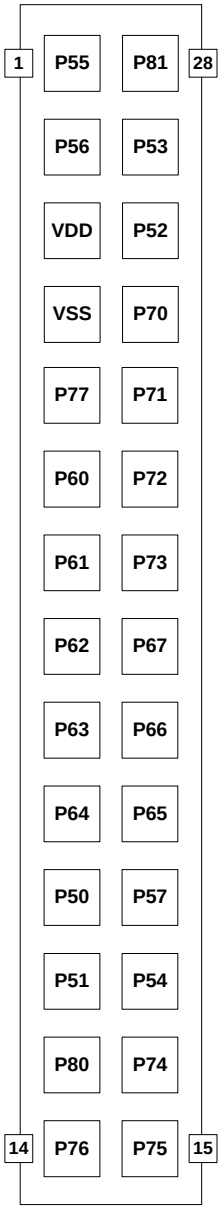
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P53
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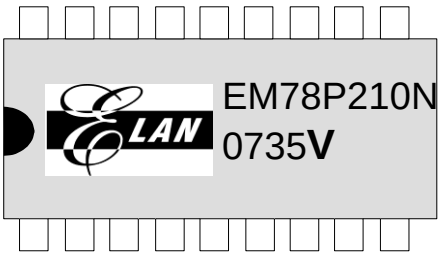
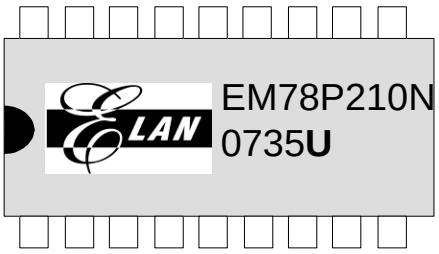
F Comparison between V-Package and U-Package Version

This microcontroller device is comprised of the older V-package version and the newer U-package version. In the newer U-package version, a Code Option NRM is added along with various features such as Crystal mode Operating frequency range, IRC mode wake-up time, WDT Time-out time, Comparator function and Pins function have been modified to favorably meet users' requirements. The following table is provided for quick comparison between the two package version and for user convenience in the choice of the most suitable product for their application.

Item	EM78P210N-V	EM78P210N-U
Crystal mode Operating frequency range at 0°C~ 70°C	**DC ~ 12MHz, 4.0V** **DC ~ 8MHz, 3.0V** **DC ~ 4MHz, 2.1V**	**DC ~ 16MHz, 4.5V** **DC ~ 8MHz, 3.0V** **DC ~ 4MHz, 2.1V**
IRC mode wake-up time (Sleep → Normal) Condition: 5V, 4MHz	**64 μs**	**10 μs**
P52, P53 Function	**Output only**	**Input / Output**
Comparator Function	**Comparator only**	**Comparator / OPA**
WDT Time-out time (Prescaler = 1 : 1) Condition: VDD = 5V	**16.5 ms ± 30%**	**15.2 ms ± 30%**
Code Option	×	**Added with a Code Option NRM**
Operating Mode	**Sleep, Normal**	**Sleep, Idle, Green, Normal**



EM78P210N-V Package Version



EM78P210N-U Package Version