TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

67,108,864-WORD BY 72-BIT DDR SYNCHRONOUS DRAM MODULE

DESCRIPTION

The THMD51N01B is a 67,108,864-word by 64-bit Double Data Rate synchronous dynamic RAM module consisting of 16 TC59WM807BFT DRAMs on a printed circuit board.

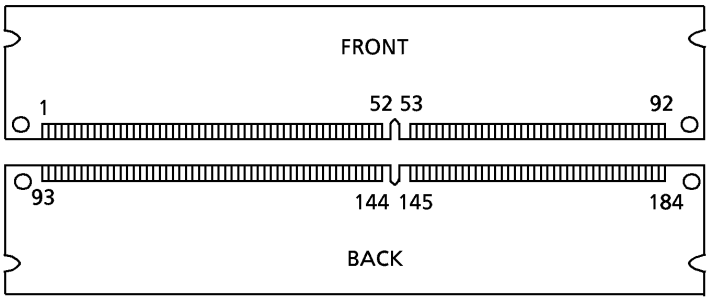
FEATURES

- 67,108,864-word by 64-bit (double-bank) organization

		70	75	80
t_{CK} Clock Cycle Time (min.)	CL = 2	7.5 ns	8 ns	10 ns
	CL = 2.5	7 ns	7.5 ns	8 ns
t_{RAS} Active-to-Precharge Command Period (min)		45 ns	45 ns	50 ns
t_{RC} Ref/Active-to-Ref/Active Command Period (min)		65 ns	65 ns	70 ns

- Fully Synchronous Operation
  Double Data Rate (DDR)
  Differential Clock inputs
- Auto Refresh and Self Refresh capability
- All inputs and outputs SSTL-2 compatible
- 8192 refresh cycles / 64 ms
- V_{DD} Power supply of 2.5V ± 0.2V
- $V_{DD}Q$ Power supply of 2.5V ± 0.2V
- Based on JEDEC Rev. 1.0

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A12	Address Inputs
BA0, 1	Bank Select
DQ0 to DQ63	Data Inputs / Outputs
/CS0, 1	Chip Select
/RAS	Row Address Strobe
/CAS	Colum Address Strobe
/WE	Write Enable
DQS0 to DQS7	Write / Read Data Strobe
DM0 to DM7	Write Mask
CLK0~2 , /CLK0~2	Clock Input
CKE0, 1	Clock Enable
SCL	Clock for PD
SDA	Serial Data / Address for PD
SA0 to 2	Address for PD
VDD	Power (+2.5 V)
VDDQ	Power (+2.5 V) for I/O buffer
VREF	Reference Voltage
VSS	Ground
VDDSPD	Serial EEPROM Power
VDDID	VDD Indentification Flag
NC	No Connection

1	VREF	93	VSS	24	DQ17	116	VSS	47	NC	139	VSS	70	VDD	162	DQ47
2	DQ0	94	DQ4	25	DQS2	117	DQ21	48	A0	140	NC	71	NC	163	NC
3	VSS	95	DQ5	26	VSS	118	A11	49	NC	141	A10	72	DQ48	164	VDDQ
4	DQ1	96	VDDQ	27	A9	119	DM2	50	VSS	142	NC	73	DQ49	165	DQ52
5	DQS0	97	DM0	28	DQ18	120	VDD	51	NC	143	VDDQ	74	VSS	166	DQ53
6	DQ2	98	DQ6	29	A7	121	DQ22	52	BA1	144	NC	75	/CLK2	167	NC
7	VDD	99	DQ7	30	VDDQ	122	A8	53	DQ32	145	VSS	76	CLK2	168	VDD
8	DQ3	100	VSS	31	DQ19	123	DQ23	54	VDDQ	146	DQ36	77	VDDQ	169	DM6
9	NC	101	NC	32	A5	124	VSS	55	DQ33	147	DQ37	78	DQS6	170	DQ54
10	NC	102	NC	33	DQ24	125	A6	56	DQS4	148	VDD	79	DQ50	171	DQ55
11	VSS	103	NC	34	VSS	126	DQ28	57	DQ34	149	DM4	80	DQ51	172	VDDQ
12	DQ8	104	VDDQ	35	DQ25	127	DQ29	58	VSS	150	DQ38	81	VSS	173	NC
13	DQ9	105	DQ12	36	DQS3	128	VDDQ	59	BA0	151	DQ39	82	VDDID	174	DQ60
14	DQS1	106	DQ13	37	A4	129	DM3	60	DQ35	152	VSS	83	DQ56	175	DQ61
15	VDDQ	107	DM1	38	VDD	130	A3	61	DQ40	153	DQ44	84	DQ57	176	VSS
16	CLK1	108	VDD	39	DQ26	131	DQ30	62	VDDQ	154	/RAS	85	VDD	177	DM7
17	/CLK1	109	DQ14	40	DQ27	132	VSS	63	/WE	155	DQ45	86	DQS7	178	DQ62
18	VSS	110	DQ15	41	A2	133	DQ31	64	DQ41	156	VDDQ	87	DQ58	179	DQ63
19	DQ10	111	CKE1	42	VSS	134	NC	65	/CAS	157	/CS0	88	DQ59	180	VDDQ
20	DQ11	112	VDDQ	43	A1	135	NC	66	VSS	158	/CS1	89	VSS	181	SA0
21	CKE0	113	BA2	44	NC	136	VDDQ	67	DQS5	159	DM5	90	NC	182	SA1
22	VDDQ	114	DQ20	45	NC	137	CLK0	68	DQ42	160	VSS	91	SDA	183	SA2
23	DQ16	115	A12	46	VDD	138	/CLK0	69	DQ43	161	DQ46	92	SCL	184	VDDSPD

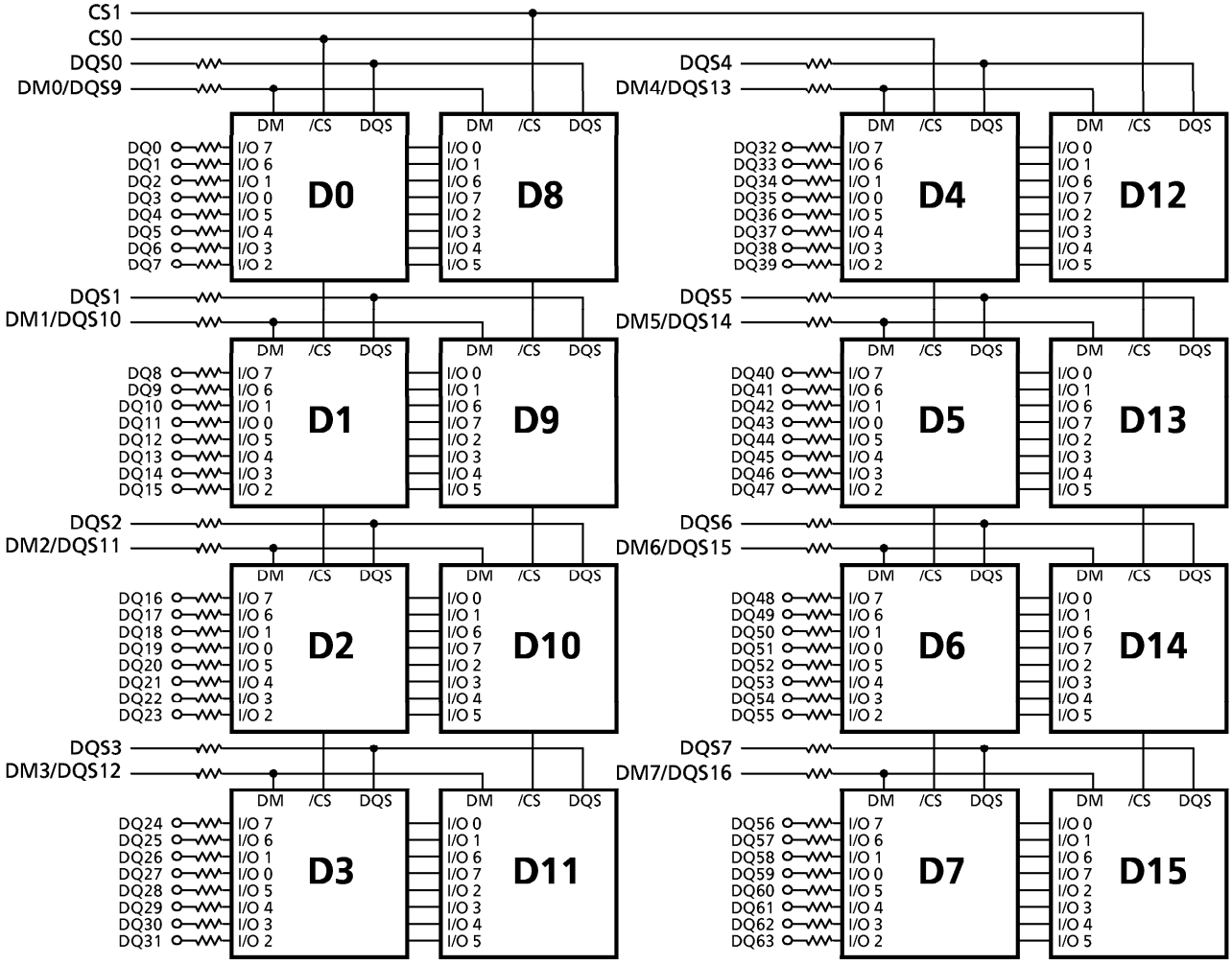
SERIAL PRESENCE DETECT

Byte Number	Function Described	70		75		80	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
0	Number of Serial PD Bytes Written during Production	128 Bytes	80h	128 Bytes	80h	128 Bytes	80h
1	Total Number of Bytes in Serial PD Device	256 Bytes	08h	256 Bytes	08h	256 Bytes	08h
2	Fundamental Memory Type	DDR SDRAM	07h	DDR SDRAM	07h	DDR SDRAM	07h
3	Number of Row Addresses on Assembly	RA0-RA12	0Dh	RA0-RA12	0Dh	RA0-RA12	0Dh
4	Number of Column Addresses on Assembly	CA0-CA9	0Ah	CA0-CA9	0Ah	CA0-CA9	0Ah
5	Number of DIMM Banks on DIMM	2 Bank	02h	2 Bank	02h	2 Bank	02h
6	Data Width of Assembly	x64	40h	x64	40h	x64	40h
7	Data Width of Assembly	x64	00h	x64	00h	x64	00h
8	Voltage Interface Level of this Assembly	SSTL 2.5V	04h	SSTL 2.5V	04h	SSTL 2.5V	04h
9	SDRAM Device Cycle Time at Maximum CL (CLX = 2.5)	7.0 ns	70h	7.5 ns	75h	8.0 ns	80h
10	SDRAM Device Access Time from Clock at CL = 2.5	±0.75 ns	75h	±0.75 ns	75h	±0.8 ns	80h
11	DIMM Configuration Type	Non - ECC	00h	Non - ECC	00h	Non - ECC	00h
12	Refresh Rate/Type	7.8 μs/Self	82h	7.8 μs/Self	82h	7.8 μs/Self	82h
13	Primary SDRAM Device Width	x8	08h	x8	08h	x8	08h
14	Error Checking SDRAM Device Width		00h		00h		00h
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access	1 CLK	01h	1 CLK	01h	1 CLK	01h
16	SDRAM Device Attributes: Burst Lengths Supported	2,4,8	0Eh	2,4,8	0Eh	2,4,8	0Eh
17	SDRAM Device Attributes: Number of Device Banks	4 Banks	04h	4 Banks	04h	4 Banks	04h
18	SDRAM Device Attributes: CAS Latency	2,2.5	0Ch	2,2.5	0Ch	2,2.5	0Ch
19	SDRAM Device Attributes: CS Latency	0	01h	0	01h	0	01h
20	SDRAM Device Attributes: WE Latency	1	02h	1	02h	1	02h
21	SDRAM Module Attributes		20h		20h		20h
22	SDRAM Device Attributes: General	Vdd±0.2V	01h	Vdd±0.2V	01h	Vdd±0.2V	01h
23	Minimum Clock Cycle Time at CLX-0.5 (CL = 2)	7.5 ns	75h	8.0 ns	80h	10 ns	A0h
24	Maximum Data Access Time (tAC) from Clock at CLX-0.5 (CL = 2)	±0.75 ns	75h	±0.75 ns	75h	±0.8 ns	80h
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)	N/A	00h	N/A	00h	N/A	00h
26	Maximum Data Access Time (tAC) from Clock at CLX-1 (CL = 1.5)	N/A	00h	N/A	00h	N/A	00h
27	Minimum Row Precharge Time (tRP)	20 ns	50h	20 ns	50h	20 ns	50h
28	Minimum Row Active to Row Active Delay (tRRD)	15 ns	3Ch	15 ns	3Ch	15 ns	3Ch
29	Minimum RAS to CAS Delay (tRCD)	15 ns	3Ch	15 ns	3Ch	20 ns	50h
30	Minimum Active to Precharge Time (tRAS)	45 ns	2Dh	45 ns	2Dh	50 ns	32h
31	Module Bank Density	256 MB	40h	256 MB	40h	256 MB	40h
32	Address and Command Setup Time before Clock	0.9 ns	90h	0.9 ns	90h	1.2 ns	C0h
33	Address and Command Hold Time after Clock	0.9 ns	90h	0.9 ns	90h	1.2 ns	C0h
34	Data/Data Mask input Setup Time before Clock	0.5 ns	50h	0.5 ns	50h	0.6 ns	60h
35	Data/Data Mask Input Hold Time after Clock	0.5 ns	50h	0.5 ns	50h	0.6 ns	60h
36-61	Reserved	Undefined	00h	Undefined	00h	Undefined	00h
62	SPD Revision	0	00h	0	00h	0	00h
63	Checksum for Bytes 0-62	67Dh	7Dh	68Dh	8Dh	767h	67h

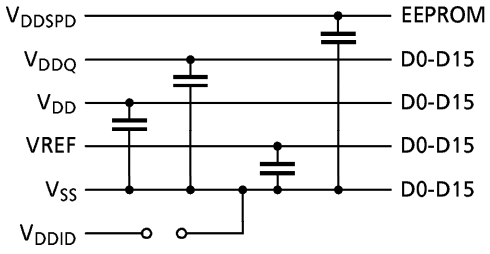
OPTION

64	Manufacturers JEDEC ID Code						
65-71							
72	Module Manufacturing Location						
73-90	Module Part Number						
91-92	Module Revision Code						
93-94	Module Manufacturing Data						
95-98	Module Serial Number						
99-125	Reserved						
126	Reserved						
127	Reserved						
128-255	Open for Customer Use						

BLOCK DIAGRAM

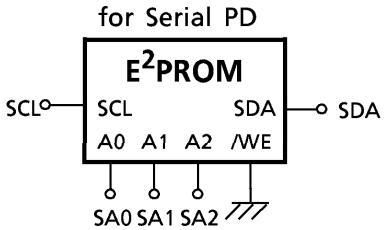


BA0-BA1 → BA0-BA1 : SDRAMs D0-D15
A0-A13 → A0-A13 : SDRAMs D0-D15
CKE1 → CKE : SDRAMs D8-D15
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0-D15
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0-D15
CKE0 → CKE : SDRAMs D0-D7
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0-D15



Clock Wiring

CLK0 / $\overline{CLK0}$ — 4 SDRAMS
CLK1 / $\overline{CLK1}$ — 6 SDRAMS
CLK2 / $\overline{CLK2}$ — 6 SDRAMS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	– 0.3 to V_{DD} + 0.3	V	1
V_{OUT}	Output Voltage	– 0.3 to V_{DD} + 0.3	V	1
V_{DD}	Power Supply Voltage	– 0.3 to 3.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	– 55 to 125	°C	1
P_D	Power Dissipation	8.3	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

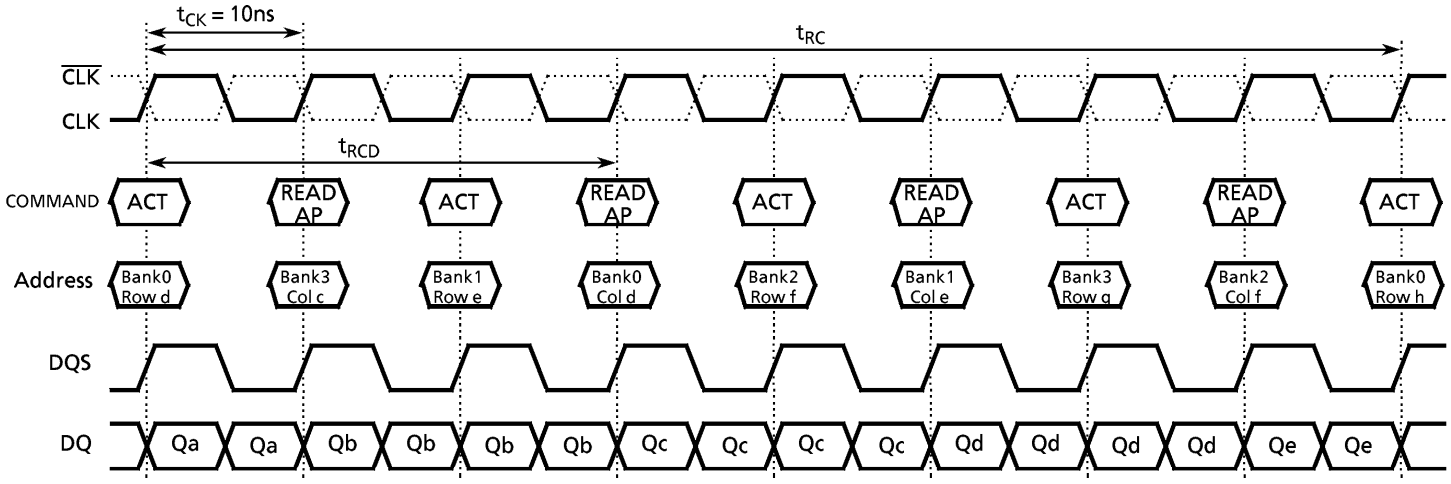
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Power Supply Voltage	2.3	2.5	2.7	V	2
$V_{DD}Q$	Power Supply Voltage (for I/O buffer)	2.3	2.5	V_{DD}	V	2
V_{REF}	Input Reference Voltage	0.48x$V_{DD}Q$	0.50x$V_{DD}Q$	0.52x$V_{DD}Q$	V	2, 3
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	2
$V_{IH\ (DC)}$	Input High Voltage (DC)	V_{REF} + 0.15	–	$V_{DD}Q$ + 0.3	V	2
$V_{IL\ (DC)}$	Input Low Voltage (DC)	- 0.30	–	V_{REF} - 0.15	V	2
$V_{ICK\ (DC)}$	Differential Clock DC Input Voltage	- 0.1	–	$V_{DD}Q$ + 0.1	V	16
$V_{ID\ (DC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.4	–	$V_{DD}Q$ + 0.2	V	14, 16
$V_{IH\ (AC)}$	Input High Voltage (AC)	V_{REF} + 0.31	–	–	V	2
$V_{IL\ (AC)}$	Input Low Voltage (AC)	–	–	V_{REF} - 0.31	V	2
$V_{ID\ (AC)}$	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.7	–	$V_{DD}Q$ + 0.2	V	14, 16
$V_{X\ (AC)}$	Differential AC Input Cross Point Voltage	$V_{DD}Q/2$ - 0.2	–	$V_{DD}Q/2$ + 0.2	V	13, 16
$V_{ISO\ (AC)}$	Differential Clock AC Middle Point	$V_{DD}Q/2$ - 0.2	–	$V_{DD}Q/2$ + 0.2	V	15, 16
$V_{IH\ (/RESET)}$	Input High Voltage (/RESET pin)	1.7	–	–	V	2
$V_{IL\ (/RESET)}$	Input Low Voltage (/RESET pin)	–	–	0.7	V	2

Note : Undershoot limit : V_{IL}(min) = -0.9V with a pulsewidth ≦ 5ns
Overshoot limit : V_{IH}(max) = $V_{DD}Q$ + 0.9V with a pulsewidth ≦ 5ns
$V_{IH(DC)}$ and $V_{IL(DC)}$ are levels to maintain the current logic state.
$V_{IH(AC)}$ and $V_{IL(AC)}$ are levels to change to the new logic state.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	ITEM	Max.			UNITS	NOTES
		– 70	– 75	– 80		
I_{DD0}	OPERATING CURRENT : One Bank Active-Precharge; $t_{RC} = t_{RC}$ min; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	1240	1200	1080	mA	7
I_{DD1}	OPERATING CURRENT : One Bank Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}$ min; CL = 2.5; $t_{CK} = t_{CK}$ min; I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	1240	1200	1080		7, 9
I_{DD2P}	Precharge Power-Down Standby Current: All Banks Idle; Power down mode; CKE ≦ V_{IL} max; $t_{CK} = t_{CK}$ min; Vin = Vref for DQ, DQS and DM	36	36	36		
I_{DD2F}	Idle Floating Standby Current: $\overline{CS}$ ≧ V_{IH} min; All Banks Idle; CKE ≧ V_{IH} min; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DQS and DM	720	640	560		7
I_{DD2N}	Idle Standby Current: $\overline{CS}$ ≧ V_{IH} min; All Banks Idle; CKE ≧ V_{IH} min; $t_{CK} = t_{CK}$ min; Address and other control inputs changing once per clock cycle; Vin ≧ VIH min or Vin ≦ V_{IL} max for DQ, DQS and DM	720	640	560		7
I_{DD2Q}	Idle Quiet Standby Current : $\overline{CS}$ ≧ V_{IH} min; All Banks Idle; CKE ≧ V_{IH} min; $t_{CK} = t_{CK}$ min; Address and other control inputs stable; Vin ≧ Vref for DQ, DQS and DM	640	560	480		7
I_{DD3P}	Active Power-Down Standby Current : One Bank Active; Power down mode; CKE ≦ V_{IL} max; $t_{CK} = t_{CK}$ min	320	320	320		
I_{DD3N}	Active Standby Current : $\overline{CS}$ ≧ V_{IH} min; CKE ≧ V_{IH} min; One Bank Active-Precharge; $t_{RC} = t_{RAS}$ max; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	920	840	760		7
I_{DD4R}	Operating Current : Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; $t_{CK} = t_{CK}$ min; I_{OUT} = 0mA	1680	1560	1480		7, 9
I_{DD4W}	Operating Current : Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; $t_{CK} = t_{CK}$ min; DQ, DM and DQS inputs changing twice per clock cycle	1680	1560	1480		7
I_{DD5}	Auto Refresh Current : $t_{RC} = t_{RFC}$ min	3040	3040	2720		7
I_{DD6}	Self Refresh Current : CKE ≦ 0.2V	48	48	48		
I_{DD7}	Random Read Current : 4 banks active read with activate every 20ns, Auto-Precharge read every 20ns; Burst = 4; $t_{RCD} = 3$; I_{OUT} = 0mA; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	2520	2480	2440		

Random Read Current Timing ($I_{DD}7$)



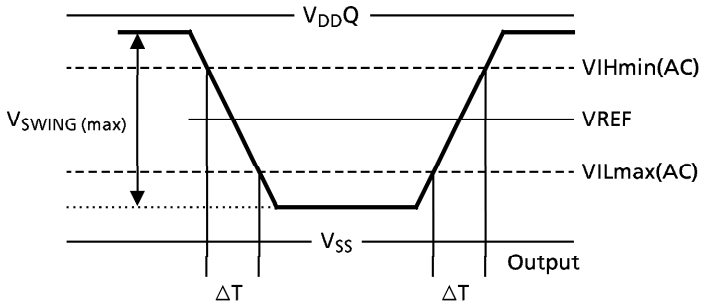
ITEM		SYMBOL	MIN.	MAX.	UNITS	NOTES
INPUT LEAKAGE CURRENT (0V≦V_{IN}≦V_{DD}Q All other pins not under test = 0V)	A0~A12, BA0, BA1, CK, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CS	$I_{I(L)}$	−10	10	μA	
	DQ, DQS		−2	2		
OUTPUT LEAKAGE CURRENT (Output disabled, 0V≦V_{OUT}≦V_{DD}Q)		$I_{O(L)}$	−5	5	μA	
OUTPUT HIGH VOLTAGE (Under AC test load condition)	Full Strength	V_{OH}	V_{TT} + 0.76	−	V	
OUTPUT LOW VOLTAGE (Under AC test load condition)		V_{OL}	−	V_{TT} − 0.76	V	
OUTPUT MINIMUM SOURCE DC CURRENT		$I_{OH(DC)}$	−15.2	−	mA	4, 6
OUTPUT MINIMUM SINK DC CURRENT		$I_{OL(DC)}$	15.2	−	mA	4, 6
OUTPUT MINIMUM SOURCE DC CURRENT	Half Strength	$I_{OH(DC)}$	−10.4	−	mA	5
OUTPUT MINIMUM SINK DC CURRENT		$I_{OL(DC)}$	10.4	−	mA	5

AC CHARACTERISTICS AND OPERATING CONDITIONS (Notes : 10, 12)

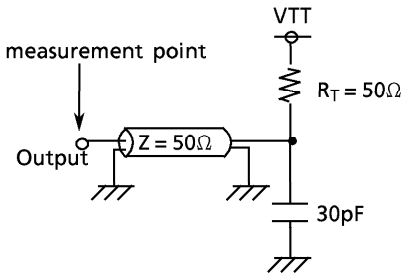
SYMBOL	PARAMETER		– 70		– 75		– 80		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Active to Ref/Active Command Period		65		65		70		ns	
t_{RFC}	Ref to Ref/Active Command Period		75		75		80			
t_{RAS}	Active to Precharge Command Period		45	100000	45	100000	50	100000		
t_{RCD}	Active to Read/Write Command Delay Time		15		15		20			
t_{RAP}	Active to Read with Auto Precharge enable		15		15		20			
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1		1		1		t_{CK}	
t_{RP}	Precharge to Active Command Period		20		20		20		ns	
t_{RRD}	Active(a) to Active(b) Command Period		15		15		15			
t_{WR}	Write Recovery Time		15		15		15			
t_{DAL}	Auto Precharge Write Recovery + Precharge time		30		30		35			
t_{CK}	CLK Cycle Time	CL = 2	7.5	15	8	15	10	15		
		CL = 2.5	7	15	7.5	15	8	15		
t_{AC}	Data Access time from CLK, $\overline{CLK}$		– 0.75	0.75	– 0.75	0.75	– 0.8	0.8		16
t_{DQSCK}	DQS output access time from CLK, $\overline{CLK}$		– 0.75	0.75	– 0.75	0.75	– 0.8	0.8		
t_{DQSQ}	Data Strobe Edge to Output Data Edge Skew			0.5		0.5		0.6		
t_{CH}	CLK High level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	11
t_{CL}	CLK Low level width		0.45	0.55	0.45	0.55	0.45	0.55		
t_{HP}	CLK half period (minimum of actual t_{CH}, t_{CL})		min(t_{CL},t_{CH})		min(t_{CL},t_{CH})		min(t_{CL},t_{CH})		ns	
t_{QH}	DQ output data hold time from DQS		t_{HP} – 0.75		t_{HP} – 0.75		t_{HP} – 1.0			
t_{RPRE}	DQS Read Preamble Time		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	11
t_{RPST}	DQS Read Postamble Time		0.4	0.6	0.4	0.6	0.4	0.6		
t_{DS}	DQ and DM Setup Time		0.5		0.5		0.6		ns	
t_{DH}	DQ and DM Hold Time		0.5		0.5		0.6			
t_{DIPW}	DQ and DM input pulse width (for each input)		1.75		1.75		2			
t_{DQSH}	DQS input high pulse width		0.35		0.35		0.35		t_{CK}	11
t_{DQSL}	DQS input low pulse width		0.35		0.35		0.35			
t_{DSS}	DQS falling edge to CLK setup time		0.2		0.2		0.2			
t_{DSH}	DQS falling edge hold time from CLK		0.2		0.2		0.2			
t_{WPRES}	Clock to DQS Write Preamble Set-Up Time		0		0		0		ns	
t_{WPRE}	DQS Write Preamble Time		0.25		0.25		0.25		t_{CK}	11
t_{WPST}	DQS Write Postamble Time		0.4		0.4		0.4			
t_{DQSS}	Write command to first DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25		
t_{DSSK}	UDQS - LDQS Skew (x16)		– 0.25	0.25	– 0.25	0.25	– 0.25	0.25		
t_{IS}	Input Setup Time		0.9		0.9		1.2		ns	
t_{IH}	Input Hold Time		0.9		0.9		1.2			
t_{IPW}	Control & Address input pulse width (for each input)		2.2		2.2		2.5			
t_{HZ}	Data-out High Impedance Time from CLK, $\overline{CLK}$		– 0.75	0.75	– 0.75	0.75	– 0.8	0.8		
t_{LZ}	Data-out Low Impedance Time from CLK, $\overline{CLK}$		– 0.75	0.75	– 0.75	0.75	– 0.8	0.8		
$t_{T\,(SS)}$	SSTL Input Transition		0.5	1.5	0.5	1.5	0.5	1.5		
t_{WTR}	Internal Write to Read command delay		1		1		1		t_{CK}	
t_{XSNR}	Exit Self Refresh to non-Read comand		75		75		80		ns	
t_{XSRD}	Exit Self Refresh to Read command		10		10		10		t_{CK}	
t_{REF}	Refresh Time (8k)			64		64		64	ms	
t_{MRD}	Mode Register Set cycle time		15		15		16		ns	

AC TEST CONDITIONS

SYMBOL	PARAMETER	VALUE	UNITS	NOTES
V_{IH}	Input High voltage (AC)	V_{REF} + 0.31	V	
V_{IL}	Input Low voltage (AC)	V_{REF} - 0.31	V	
V_{REF}	Input reference voltage	0.5 x $V_{DD}Q$	V	
V_{TT}	Termination voltage	0.5 x $V_{DD}Q$	V	
V_{SWING}	Input signal peak to peak swing	1.0	V	
Vr	Differential Clock Input Reference Voltage	V_X (AC)	V	
V_{ID} (AC)	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	1.5	V	
SLEW	Input signal minimum slew rate	1.0	V/ns	
V_{OTR}	Output timing measurement reference voltage	0.5 x $V_{DD}Q$	V	



SLEW = (VIHmin(AC) - VILmax(AC)) / ΔT



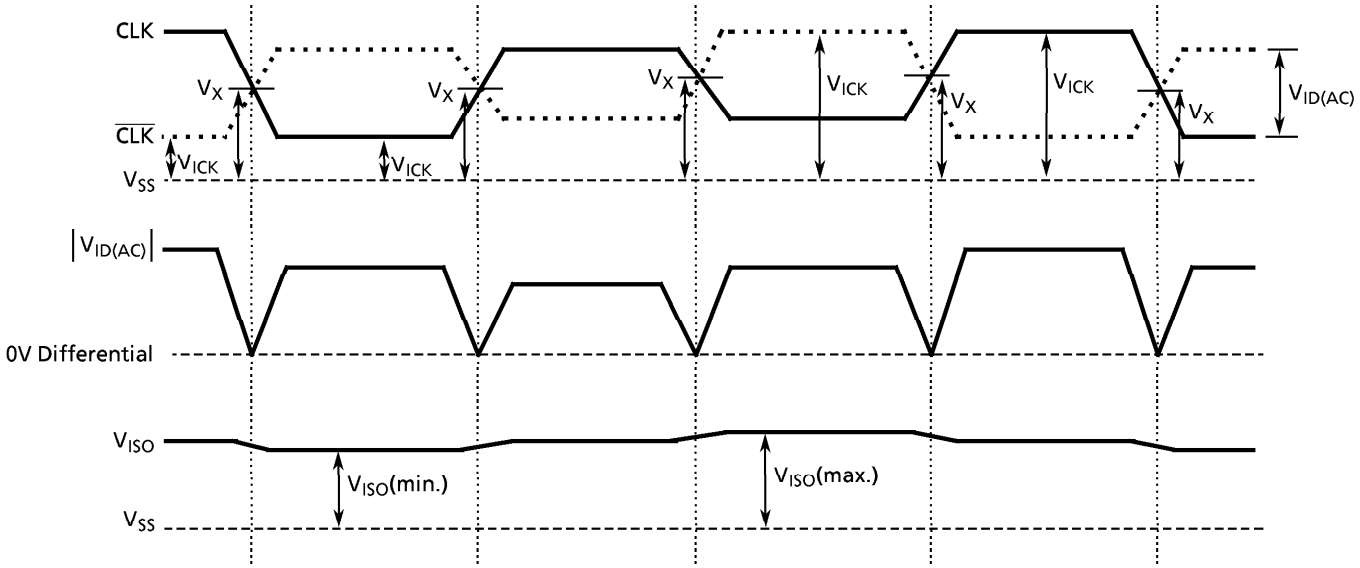
A.C. TEST LOAD

CAPACITANCE (V_{DD} = 2.5V , f = 1MHz , Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_1	Input Capacitance (A0~A12)	–	TBD	pF
C_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1)	–	TBD	pF
C_3	Input Capacitance (CLK0~CLK2, $\overline{CLK}$0~$\overline{CLK}$2)	–	TBD	pF
C_4	Input Capacitance ($\overline{CS}$0, $\overline{CS}$1)	–	TBD	pF
C_5	Input Capacitance (CKE0, CKE1)	–	TBD	pF
C_6	Input Capacitance (DM0~DM7)	–	TBD	pF
C_{DQ1}	I/O Capacitance (DQ0~DQ63)	–	TBD	pF
C_{DQ2}	I/O Capacitance (DQS0~DQS7)	–	TBD	pF

NOTES:

1. Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.
2. All voltages are referenced to Vss, $V_{SS}Q$.
3. Peak to peak AC noise on VREF may not exceed $\pm 2\%$ $V_{REF\,(DC)}$.
4. $V_{OH} = 1.95V$, $V_{OL} = 0.35V$
5. $V_{OH} = 1.9V$, $V_{OL} = 0.4V$
6. The values of $I_{OH}(DC)$ is based on $V_{DD}Q = 2.3V$ and $V_{TT} = 1.19V$.
   The values of $I_{OL}(DC)$ is based on $V_{DD}Q = 2.3V$ and $V_{TT} = 1.11V$.
7. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
8. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
9. These parameters depend on the output loading. Specified values are obtained with the output open.
10. Transition times are measured between $V_{IH\,min\,(AC)}$ and $V_{IL\,max\,(AC)}$. Transition (rise and fall) of input signals have a fixed slope.
11. If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
    (i.e., $t_{DQSS} = 0.75 \times t_{CK}$, $t_{CK} = 7.5ns$, $0.75 \times 7.5ns = 5.625ns$ is rounded up to 5.6ns.)
12. V_X is the differential clock cross point voltage where input timing measurement is referenced.
13. V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.
14. V_{ISO} means $\{V_{ICK}(CLK) + V_{ICK}(\overline{CLK})\} / 2$.
15. Refer to the figure below.



16. t_{AC} and t_{DQSCK} depend on the clock jitter. These timing are measured at stable clock.

Power Up Sequence

1. Apply power and attempt to CKE at a low state (≦0.2V).
   (all other inputs may be undefined)

   (1) Apply V_{DD} before or at the same time as $V_{DD}Q$.

   (2) Apply $V_{DD}Q$ before or at the same time as V_{TT} and V_{REF}.

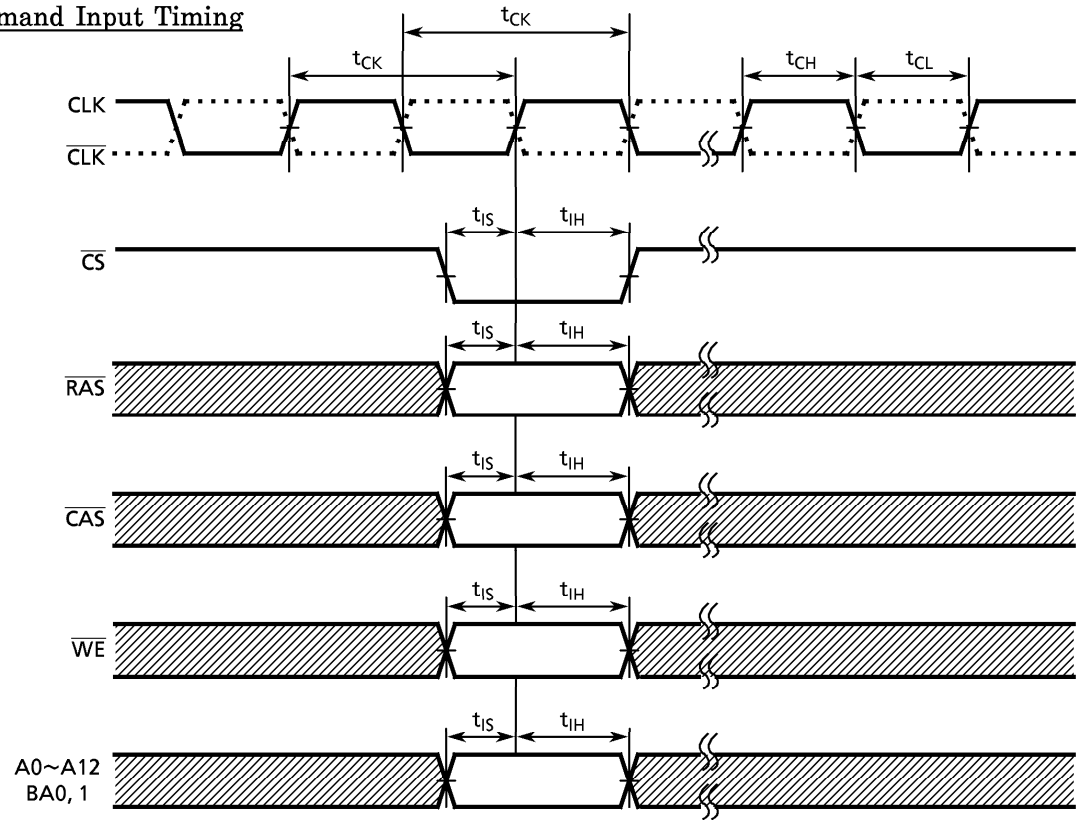
2. Start Clock and maintain stable condition for 200μs(min).
3. After stable power and clock, apply NOP and take CKE high.
4. Issue EMRS - enable DLL and establish Output Driver Type.
5. Issue MRS - reset DLL and set device to idle with bit A8.
   (an additional 200cycles(min) of clock are required for DLL Lock)
6. Issue precharge command for all banks of the device.
7. Issue two or more Auto Refresh commands.
8. Issue MRS - Initialize device operation.
   (If device operation mode is set at sequence 5, sequence 8 can be skipped.)

   EMRS : Extended Mode Register Set

   MRS : Mode Register Set

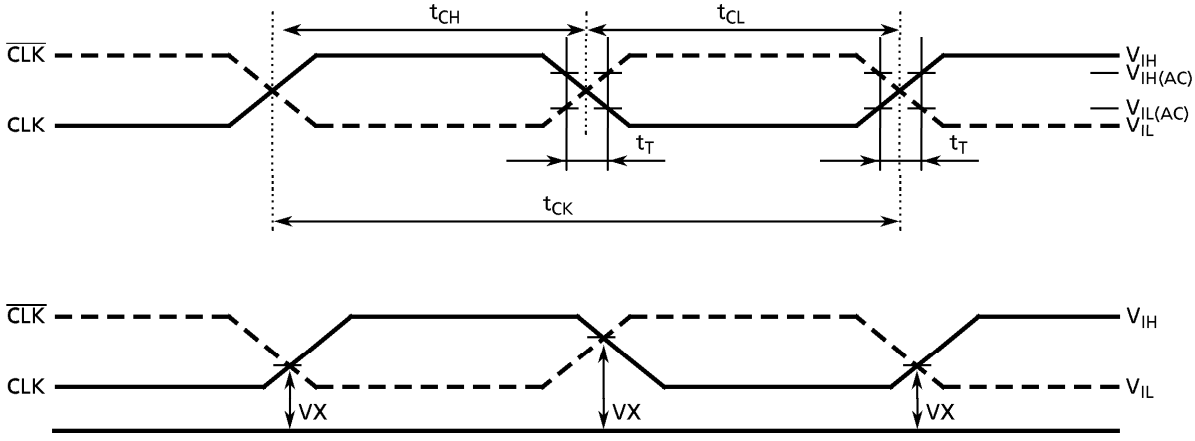
TIMING DIAGRAMS

Command Input Timing

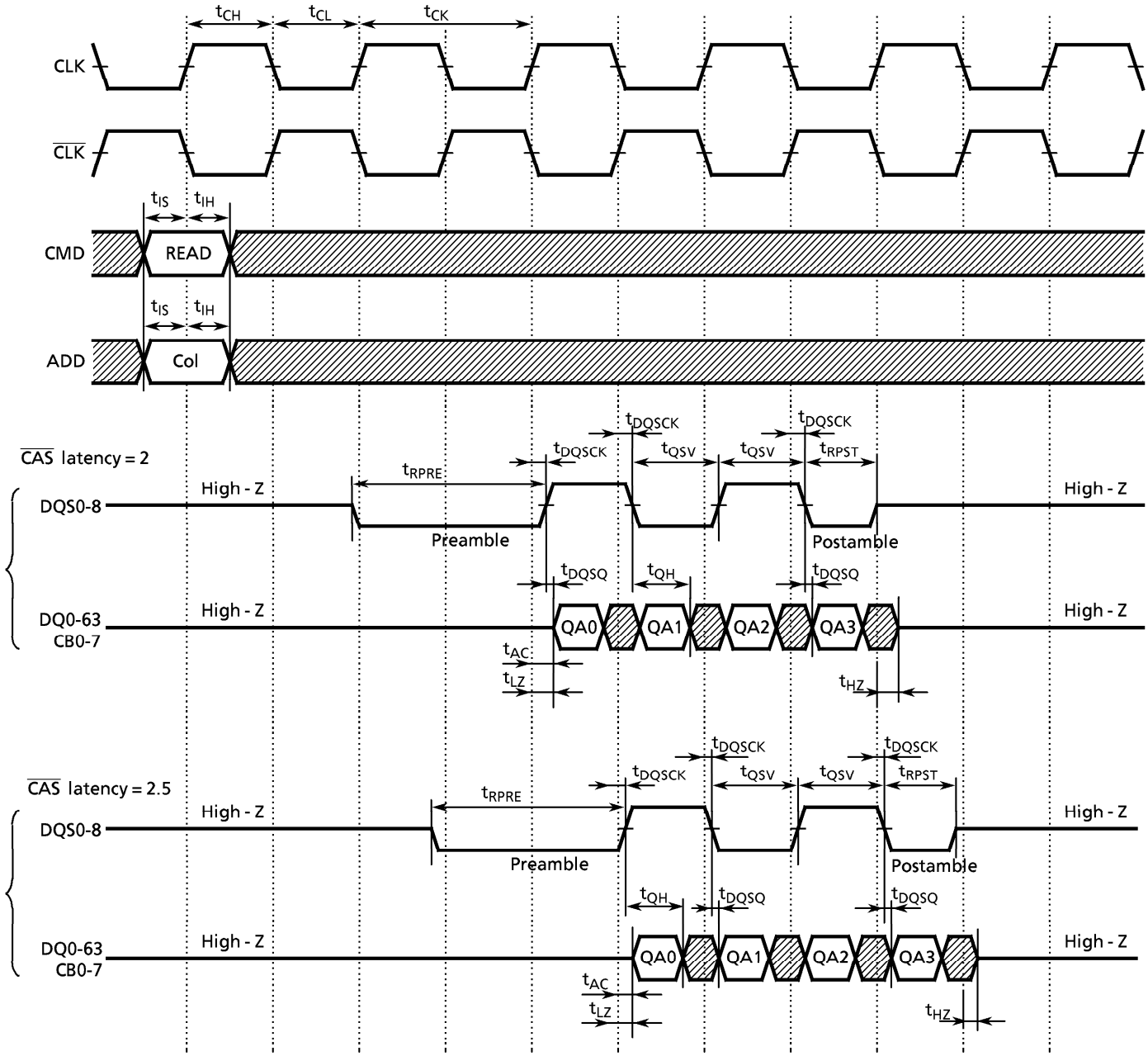


Refer to the Command Truth Table.

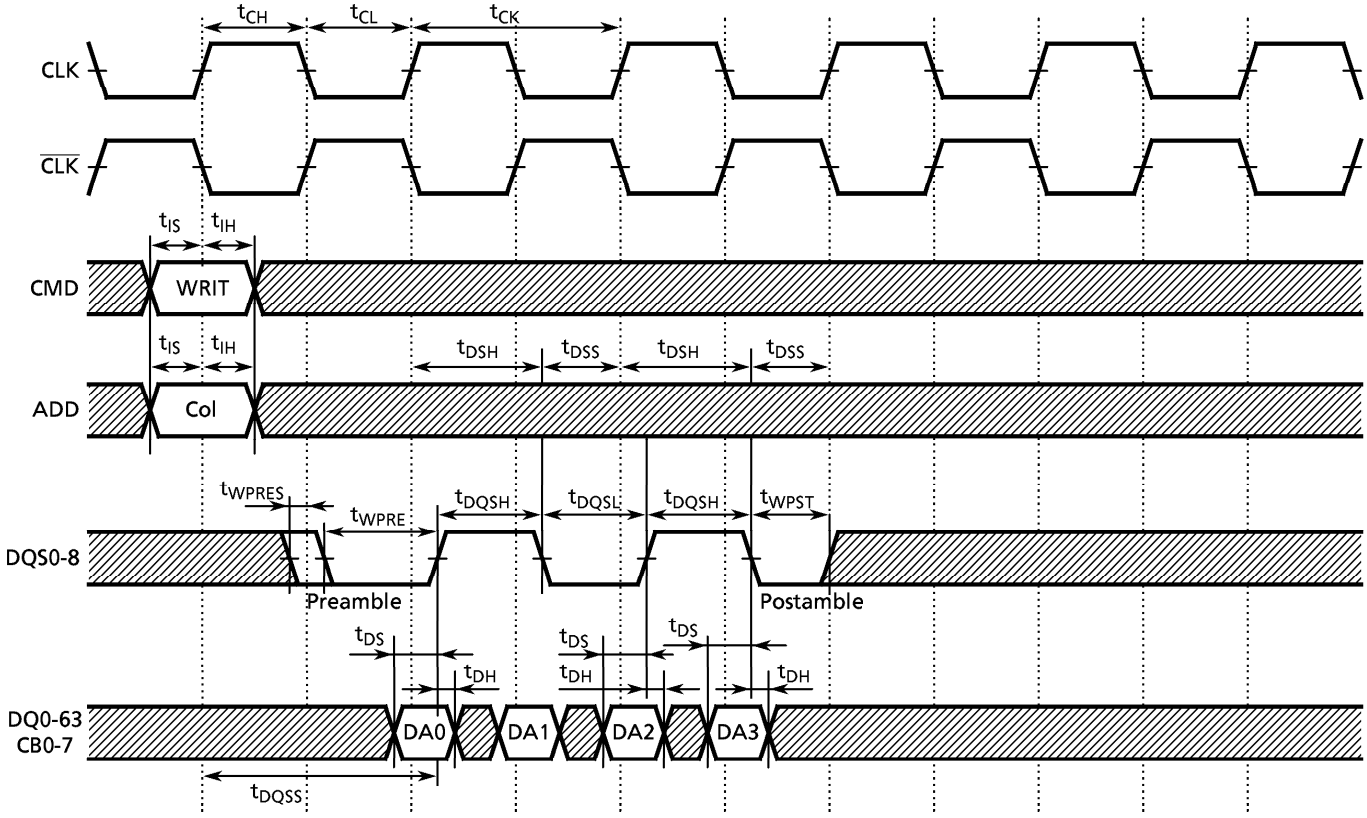
Timing of the CLK, $\overline{CLK}$



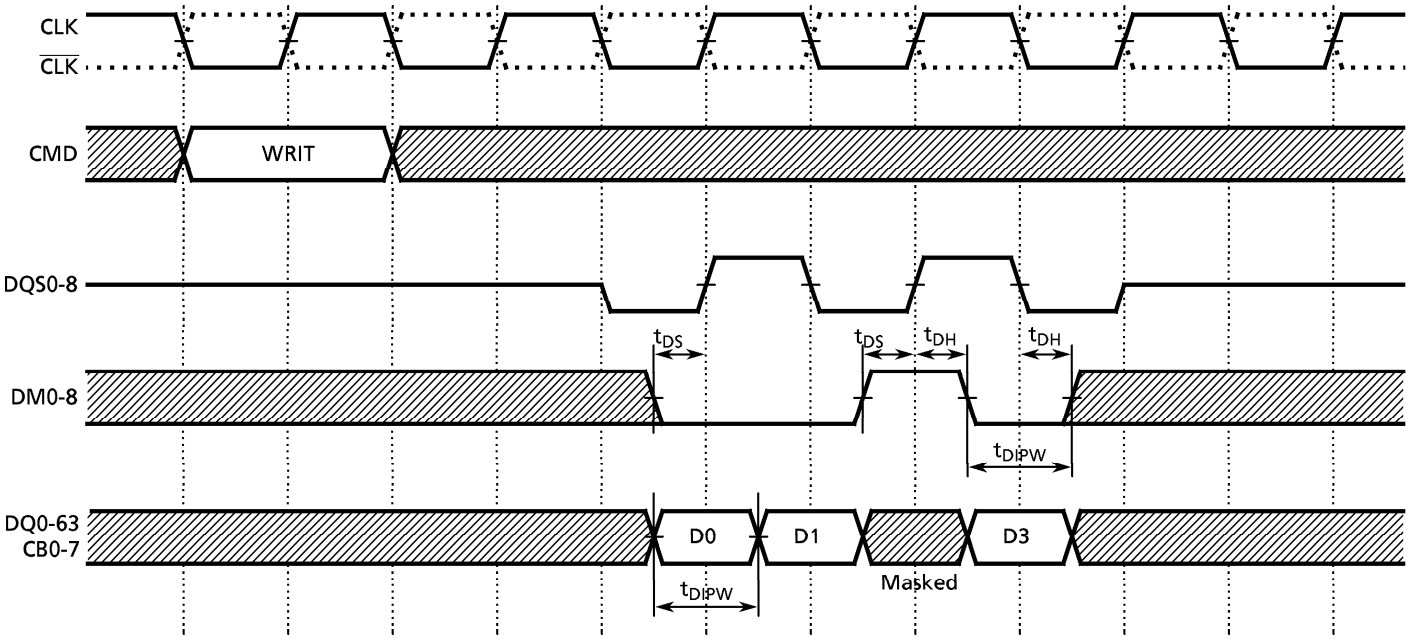
Read Timing (Burst Length = 4)



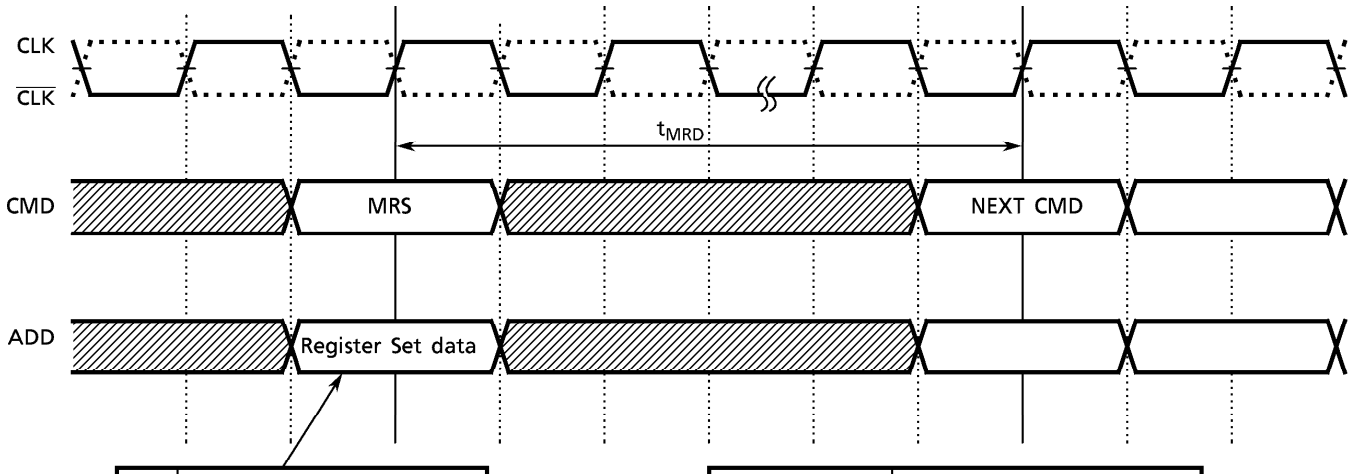
Write Timing (Burst Length = 4)



DM, DATA MASK


CLK
CLK
CMD
WRIT
DQS0-8
DM0-8
DQ0-63
CB0-7
tDS
tDS
tDH
tDH
tDIPW
tDIPW
D0
D1
D3
Masked

Mode Register Set (MRS) Timing



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	Reserved
A8	DLL Reset	
A9	"0"	Reserved
A10	"0"	
A11	"0"	
A12	"0"	
BA0	"0"	Mode Register Set or Extended Mode Register Set
BA1	"0"	

※ "Reserved" should stay "0" during MRS cycle.

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1		

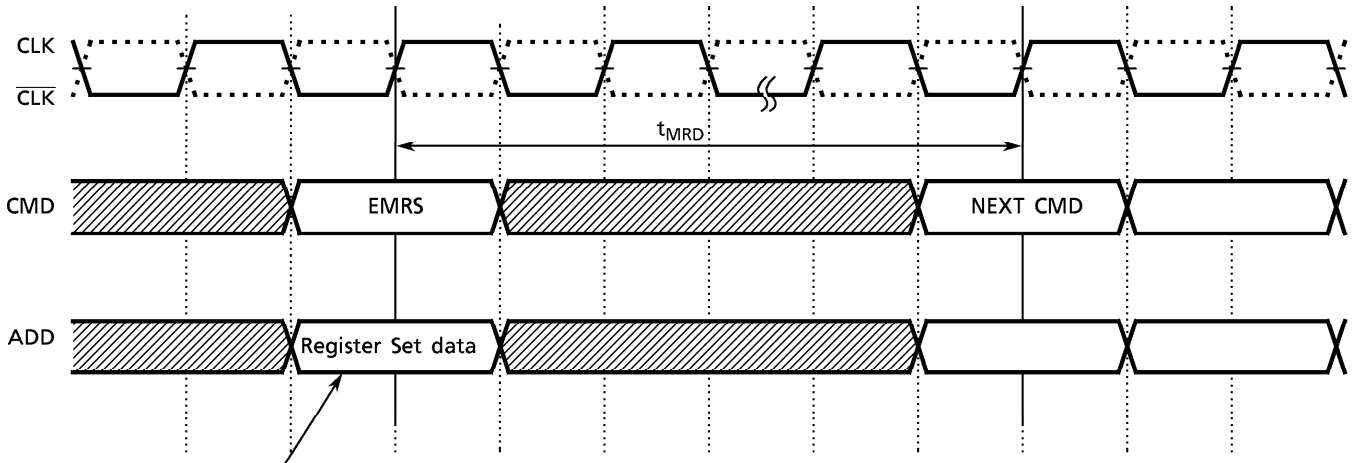
A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	Reserved
1	0	0	
1	0	1	
1	1	0	2.5
1	1	1	Reserved

A8	DLL Reset
0	No
1	Yes

BA1	BA0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

Extended Mode Register Set (EMRS) Timing



A0	DLL Switch	
A1	Output Driver	
A2	"0"	Reserved
A3	"0"	
A4	"0"	
A5	"0"	
A6	"0"	
A7	"0"	
A8	"0"	
A9	"0"	
A10	"0"	
A11	"0"	
A12	"0"	
BA0	"1"	Mode Register Set or Extended Mode Register Set
BA1	"0"	

A0	DLL Switch
0	Enable
1	Disable

A1	Output Driver Size
0	Full Strength
1	Half Strength

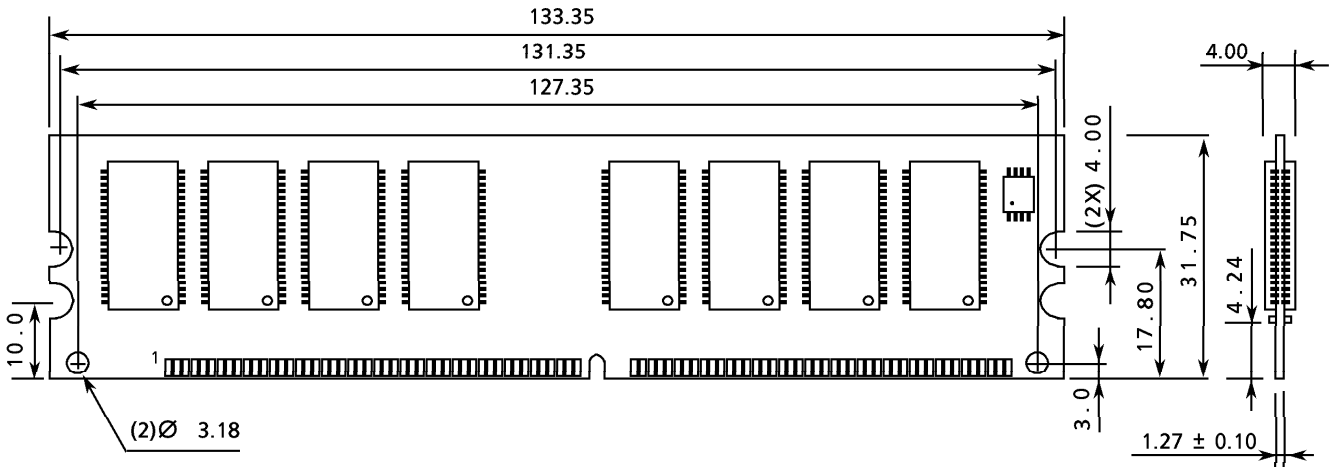
BA1	BA0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

※ "Reserved" should stay "0" during EMRS cycle.

PACKAGE DIMENSIONS (THMD51N01B)

Unit: mm

FRONT



BACK