

4-Bit Differential ECL Bus/TTL Bus Transceiver

The MC10H/100H680 is a dual supply 4-bit differential ECL bus to TTL bus transceiver. It is designed to allow the system designer to no longer be limited in bus speed associated with standard TTL busses. Using a differential ECL Bus will increase the frequency of operation and increase noise immunity.

Both the TTL and the ECL ports are capable of driving a bus. The ECL outputs have the ability to drive 25 Ω , allowing both ends of the bus line to be terminated in the characteristic impedance of 50 Ω . The TTL outputs are specified to source 15 mA and sink 48 mA, allowing the ability to drive highly capacitive loads.

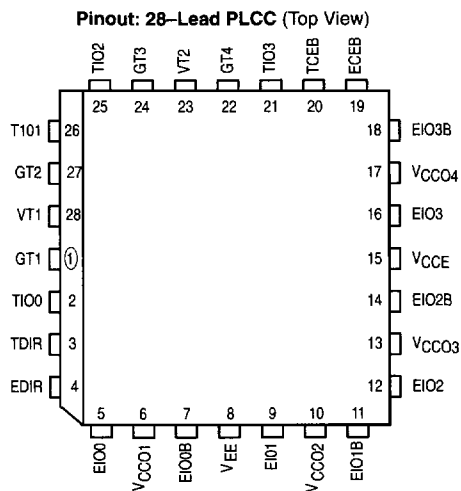
The ECL output levels are V_{OH} approximately equal to -1.0 V and V_{OL} cutoff equal to -2.0 V (V_{TT}). When the ECL ports are disabled both $EIOx$ and $EIOxB$ go to the V_{OL} cutoff level. The ECL input receivers have special circuitry which detects this disabled condition, prevents oscillation, and forces the TTL output to the low state. The noise margin in this disabled state is greater than 600 mV. Multiple ECL V_{CCO} pins are utilized to minimize switching noise.

The TTL ports have standard levels. The TTL input receivers have PNP input devices to significantly reduce loading. Multiple TTL power and ground pins are utilized to minimize switching noise.

The control pins (EDIR and ECEB) of the 10H version is compatible with MECL 10H ECL logic levels. The control pins of the 100H version are compatible with 100K levels.

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- Differential ECL Bus (25 Ω) I/O Ports
- High Drive TTL Bus I/O Ports
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- Direction and Chip Enable Control Pins



MC10H680
MC100H680



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

PIN DESCRIPTIONS

Pin	Symbol	Function
1	GT1	TTL Ground 1
2	TIO0	TTL I/O Bit 0
3	TDIR	TTL Direction Control
4	EDIR	ECL Direction Control
5	EIO0	ECL I/O Bit 0
6	VCCO1	ECL VCC 1 (0V) – Outputs
7	EIO0B	ECL I/O Bit 0 Bar
8	VEE	ECL Supply ($-5.2/-4.5$ V)
9	EIO1	ECL I/O Bit 1
10	VCCO2	ECL VCC 2 (0V) – Outputs
11	EIO1B	ECL I/O Bit 1 Bar
12	EIO2	ECL I/O Bit 2
13	VCCO3	ECL VCC 3 (0V) – Outputs
14	EIO2B	ECL I/O Bit 2 Bar
15	VCCE	ECL VCC (0V)
16	EIO3	ECL I/O Bit 3
17	VCCO4	ECL VCC 4 (0V) – Outputs
18	EIO3B	ECL I/O Bit 3 Bar
19	ECEB	ECL Chip Enable Bar Control
20	TCEB	TTL Chip Enable Bar Control
21	TIO3	TTL I/O Bit 3
22	GT4	TTL Ground 4
23	VT2	TTL Supply 2 (5V)
24	GT3	TTL Ground 3
25	TIO2	TTL I/O Bit 2
26	TIO1	TTL I/O Bit 1
27	GT2	TTL Ground 2
28	VT1	TTL Supply 1 (5V)



TRUTH TABLE

TDIR — Direction Control TTL Levels
 EDIR — Direction Control ECL Levels
 TCEB — Chip Enable Bar Control TTL Levels
 ECEB — Chip Enable Bar Control ECL Levels
 TIN — TTL Input
 TOUT — TTL Output
 EIN — ECL Input
 EINB — ECL Input Bar
 EOUT — ECL Output
 EOUTB — ECL Output Bar

H — HIGH
 L — LOW
 LC — ECL Low Cutoff ($V_{TT} = -2.0\text{ V}$)
 X — Don't Care
 Z — High Impedance

ECEB	TCEB	EDIR	TDIR	EIN	EINB	EOUT	EOUTB	TIN	TOUT	COMMENTS
H	X	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
X	H	X	X	X	X	LC	LC	X	Z	ECL and TTL Outputs Disabled
L	L	H	X	H	LC			NA	H	ECL to TTL Direction
L	L	H	X	LC	H			NA	L	ECL to TTL Direction
L	L	H	X	LC	LC			NA	L	ECL to TTL Direction (L-L Cond.)
L	L	X	H	H	LC			NA	H	ECL to TTL Direction
L	L	X	H	LC	H			NA	L	ECL to TTL Direction
L	L	X	H	LC	LC			NA	L	ECL to TTL Direction (L-L Cond.)
L	L	L	L	NA	NA	H	LC	H		TTL to ECL Direction
L	L	L	L	NA	NA	LC	H	L		TTL to ECL Direction

2**ABSOLUTE RATINGS (Do not exceed):**

Power Supply Voltage	V_{EE} (ECL)	-8.0 to 0	Vdc
Power Supply Voltage	V_{CCT} (TTL)	-0.5 to +7.0	Vdc
Input Voltage	V_i (ECL) V_i (TTL)	0.0 to V_{EE} -0.5 to +7.0	Vdc
Disabled 3-State Output	V_{out} (TTL)	0.0 to V_{CCT}	Vdc
Output Source Current Continuous	I_{out} (ECL)	100	mA _{dc}
Output Source Current Surge	I_{out} (ECL)	200	mA _{dc}
Storage Temperature	T_{stg}	-65 to 150	°C
Operating Temperature	T_{amb}	0.0 to +75	°C

MC10H680 MC100H680

ECL DC CHARACTERISTICS: $V_{CCCT} = +5.0\text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H Version)

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{EE}	Supply Current/ECL		-110		-110		-110	mA	
I_{INH}	Input HIGH Current		225		145		145	μA	
I_{INL}	Input LOW Current	0.5		0.5		0.3		μA	
V_{OH}	Output HIGH Voltage	-1100	-840	-1100	-810	-1100	-735	mV	25 Ω to -2.1 V
V_{OL}	Output LOW Voltage	-2.1	-2.03	-2.1	-2.03	-2.1	-2.03	V	

CONTROL INPUTS ONLY

10H ECL DC CHARACTERISTICS: $V_{CCCT} = +5.0 \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	-1170	-840	-1130	-810	-1070	-735	mV	
V_{IL}	Input LOW Voltage	-1950	-1480	-1950	-1480	-1950	-1450		

CONTROL INPUTS ONLY

100H ECL DC CHARACTERISTICS: $V_{CCCT} = +5.0 \pm 10\%$, $V_{EE} = -4.2\text{ V}$ to -5.5 V

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Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	-1165	-880	-1165	-880	-1165	-880	mV	
V_{IL}	Input LOW Voltage	-1810	-1475	-1810	-1475	-1810	-1475		

TTL DC CHARACTERISTICS: $V_{CCCT} = +5.0\text{ V} \pm 10\%$, $V_{EE} = -5.2 \pm 5\%$ (10H Version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H Version)

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH}	Standard Input	2.0		2.0		2.0		Vdc	
V_{IL}	Standard Input		0.8		0.8		0.8		
V_{IK}	Input Clamp		-1.2		-1.2		-1.2	Vdc	$I_{IN} = -18\text{ mA}$
V_{OH}	Output HIGH Voltage	2.5		2.5		2.5		V	$I_{OH} = -3.0\text{ mA}$ $I_{OH} = -15\text{ mA}$
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	$I_{OL} = 48\text{ mA}$
I_{IH}^*	TTL (Input HIGH)		20		20		20	μA	$V_{in} = 2.7\text{ V}$ $V_{in} = 7.0\text{ V}$
I_{IL}^*	TTL (Input LOW)		-0.6		-0.6		-0.6	mA	$V_{in} = 0.5\text{ V}$
I_{CCL}	Supply Current		75		75		75	mA	
I_{CCH}	Supply Current		70		70		70	mA	
I_{CCZ}	Supply Current		70		70		70	mA	
I_{OS}	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	$V_{OUT} = 0\text{ V}$

* NOTE: TTL Control Inputs only

TTL I/O DC CHARACTERISTICS ONLY

Test Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = 25^\circ\text{C}$		$T_A = 75^\circ\text{C}$		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_{IH}/I_{OZH}	Output Disable		70		70		70	μA	$V_{OUT} = 2.7\text{ V}$
I_{IL}/I_{OZL}	Current		200		200		200		$V_{OUT} = 0.5\text{ V}$

ECL TO TTL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T _A = 0°C		T _A = 25°C		T _A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay to Output	2, 4	2.7	4.8	2.7	4.8	2.7	4.8	ns	C _L = 50 pF
t _{PZH} t _{PZL}	ECEB to Output Enable Time	2, 5, 6	3.5	6.5	3.5	6.5	3.7	6.7	ns	C _L = 50 pF
t _{PHZ} t _{PLZ}	ECEB to Output Disable Time	2, 5, 6	3.5	8.6	3.5	8.6	3.7	8.8	ns	C _L = 50 pF
t _{PZH} t _{PZL}	TCEB to Output Enable Time	2, 5, 6	5.7	7.7	5.7	7.7	5.9	7.9	ns	C _L = 50 pF
t _{PHZ} t _{PLZ}	TCEB to Output Disable Time	2, 5, 6	4.0	8.5	4.1	8.4	4.2	8.3	ns	C _L = 50 pF
t _r /t _f	1.0 to 2.0 Vdc	3	0.4	1.5	0.4	1.5	0.4	1.5	ns	C _L = 50 pF

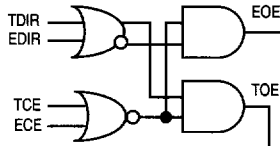
TTL TO ECL DIRECTION / AC TEST

Test Symbol	Parameter	Waveforms	T _A = 0°C		T _A = 25°C		T _A = 75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay to Output	1, 4	1.8	4.6	1.8	4.6	2.0	4.9	ns	25 Ω to -2.0 V
t _{PLH} t _{PHL}	ECEB to Output	1, 4	2.9	5.1	3.0	5.2	3.4	5.7	ns	25 Ω to -2.0 V
t _{PLH} t _{PHL}	TCEB to Output	1, 4	3.4	6.3	3.5	6.6	3.8	7.4	ns	25 Ω to -2.0 V
t _r /t _f	Output Rise/Fall Time 20%–80%	1, 3	1.0	3.4	1.0	3.4	1.0	3.4	ns	25 Ω to -2.0 V

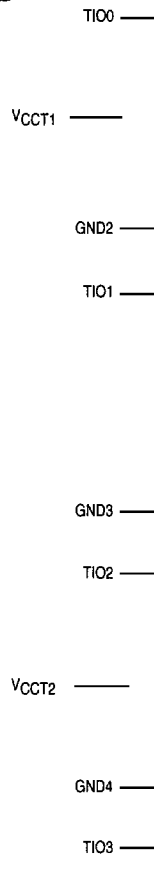
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BLOCK DIAGRAM

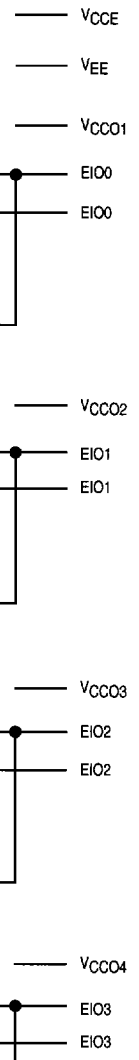
CONTROL INPUTS



TTL I/O



ECL I/O



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SWITCHING CIRCUIT AND WAVEFORMS

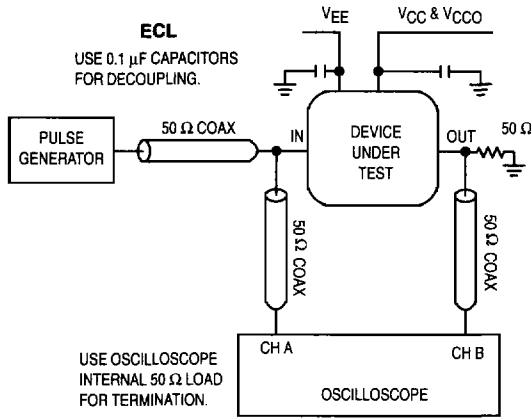


Figure 1. Switching Circuit ECL

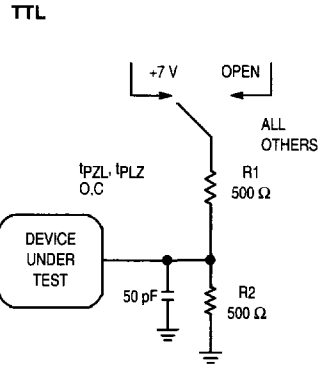


Figure 2.

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ECL/TTL

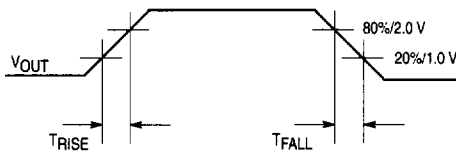


Figure 3. WAVEFORMS: Rise and Fall Times

ECL/TTL

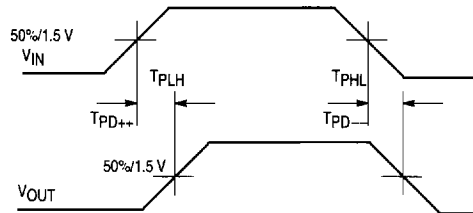


Figure 4. Propagation Delay — Single Ended

TTL

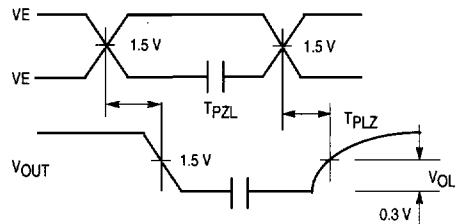


Figure 5. 3-State Output Low Enable and Disable Times

TTL

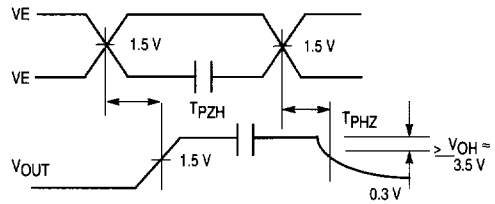


Figure 6. 3-State Output High Enable and Disable Times