

P29FCT520/A/B (P29PCT520/A/B) P29FCT521/A/B (P29PCT521/A/B) PIPELINE REGISTERS

★ FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-B speed at 7.5ns max. (Com'I)
FCT-A speed at 14.0ns max. (Com'I)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'I), 48 mA (MII)
15 mA Source Current (Com'I), 12 mA (MII)
- Single and Dual Pipeline Operation Modes
- Multiplexed Data Inputs and Outputs
- Functionally Equivalent to Bipolar 29520/29521 Type Products
- Manufactured in 0.8 micron PACE Technology™

★ DESCRIPTION

The 'FCT520 and 'FCT521 are multi-level 8-bit wide pipeline registers. Each device consists of 4 registers A1, A2, B1 and B2 which are configured by the instruction inputs I_0 , I_1 as a single 4-level pipeline or as two 2-level pipelines. The contents of any register may be read at the multiplexed output at any time by using the mux-selection controls S_0 and S_1 .

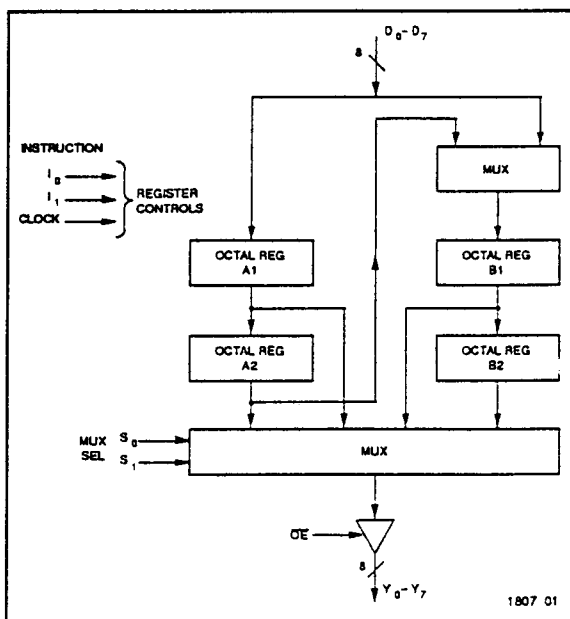
The pipeline registers are positive edge triggered and data is shifted by the rising edge of the clock input. Instruction $I = 0$ selects the 4-level pipeline mode. Instruction $I = 1$ selects the 2-level B pipeline while $I = 2$ selects the 2-level

A pipeline. $I = 3$ is the HOLD instruction; no shifting is performed by the clock in this mode.

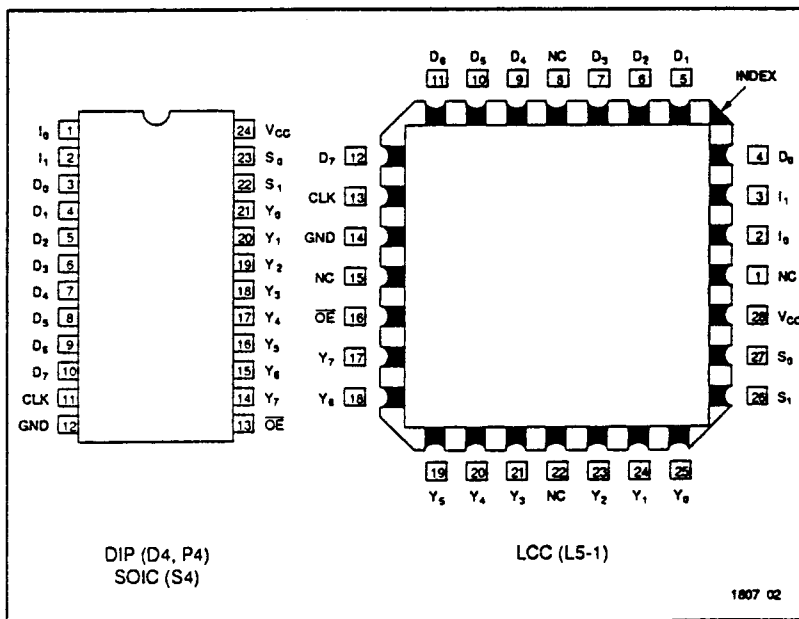
The 'FCT520 and 'FCT521 differ only in the 2-level operation mode. For the 'FCT520, data is shifted from level 2 to level 1 and new data is loaded into level 2. In the 'FCT521, new data is overwritten into level 1. To shift data from level 1 to level 2 in the 'FCT521, the 4-level pipeline mode must be used. Note that new data will also be clocked into both A1 and B1 during this 4-level shift operation.

The 'FCT520 and 'FCT521 are available in standard 24-pin 300 mil DIP, SOIC and 28-pad square LCC package.

★ LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS^{1,2}

| Symbol | Parameter | Value | Unit |
|------------------|-------------------------------------|--------------|------|
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| T _A | Ambient Temperature Under Bias | -65 to +135 | °C |
| V _{CC} | V _{CC} Potential to Ground | -0.5 to +7.0 | V |
| I _{IN} | Input Current | -30 to +5.0 | mA |

Notes: 1807 Tbl 01
 1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

| Symbol | Parameter | Value | Unit |
|---------------------|---------------------------|-------------------------------|------|
| I _{OUTPUT} | Current Applied to Output | 120 | mA |
| V _{IN} | Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _{OUT} | Voltage Applied to Output | -0.5 to V _{CC} + 0.5 | V |

1807 Tbl 02
 2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

| Free Air Ambient Temperature | Min | Max |
|------------------------------|-------|--------|
| Military | -55°C | +125°C |
| Commercial | 0°C | +70°C |

1807 Tbl 03

| Supply Voltage (V _{CC}) | Min | Max |
|-----------------------------------|--------|--------|
| Military | +4.5V | +5.5V |
| Commercial | +4.75V | +5.25V |

1807 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Symbol | Parameter | Min | Typ ¹ | Max | Units | V _{CC} | Conditions | |
|------------------|---|---|-----------------------|-----------------------|-----------------|-----------------|------------------------------------|-------------------------|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | | |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | | |
| V _H | Hysteresis | | 0.35 | | V | | All inputs | |
| V _{IK} | Input Clamp Diode Voltage | | -0.7 | -1.2 | V | MIN | I _{IN} = -18mA | |
| V _{OH} | Output HIGH Voltage | V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V | | V _{CC} - 0.2 | V _{CC} | V | I _{OH} = -32μA | |
| | | Military/Commercial (CMOS) | V _{CC} - 0.2 | | V | MIN | I _{OH} = -300μA | |
| | | Military (TTL) | 2.4 | 4.3 | V | MIN | I _{OH} = -12mA | |
| | | Commercial (TTL) | 2.4 | 4.3 | V | MIN | I _{OH} = -15mA | |
| V _{OL} | Output LOW Voltage | V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V | | | GND | 0.2 | V | I _{OL} = 300μA |
| | | Military/Commercial (CMOS) | | GND | 0.2 | V | MIN | I _{OL} = 300μA |
| | | Military (TTL) | | 0.3 | 0.5 | V | MIN | I _{OL} = 32mA |
| | | Commercial (TTL) | | 0.3 | 0.5 | V | MIN | I _{OL} = 48mA |
| | Commercial (TTL) | | 0.3 | 0.5 | V | MIN | I _{OL} = 64mA | |
| I _{IH} | Input HIGH Current | | | 5 | μA | MAX | V _{IN} = V _{CC} | |
| I _{IL} | Input LOW Current | | | -5 | μA | MAX | V _{IN} = GND | |
| I _{IH} | Input HIGH Current ³ | | | 5 | μA | MAX | V _{IN} = 2.7V | |
| I _{IL} | Input LOW Current ³ | | | -5 | μA | MAX | V _{IN} = 0.5V | |
| I _{OZH} | Off State I _{OUT} HIGH-Level Output Current | | | 10 | μA | MAX | V _{OUT} = V _{CC} | |
| I _{OZL} | Off State I _{OUT} LOW-Level Output Current | | | -10 | μA | MAX | V _{OUT} = GND | |
| I _{OZH} | Off State I _{OUT} HIGH-Level Output Current ³ | | | 10 | μA | MAX | V _{OUT} = 2.7V | |
| I _{OZL} | Off State I _{OUT} LOW-Level Output Current ³ | | | -10 | μA | MAX | V _{OUT} = 0.5V | |
| I _{OS} | Output Short Circuit Current ² | -60 | -120 | -225 | mA | MAX | V _{OUT} = 0.0V | |
| C _{IN} | Input Capacitance ³ | | 5 | 10 | pF | MAX | All inputs | |
| C _{OUT} | Output Capacitance ³ | | 9 | 12 | pF | MAX | All outputs | |

Notes: 1807 Tbl 05
 1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
 2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
 3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Typ ¹ | Max | Units | Conditions |
|-----------------|--|------------------|-------------------|------------|---|
| I_{CC} | Quiescent Power Supply Current (CMOS inputs) | 0.003 | 0.5 | mA | $V_{CC} = \text{MAX}$, $f_1 = 0$, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs) | 0.5 | 2.0 | mA | $V_{CC} = \text{MAX}$, Outputs Open, $f_1 = 0$, $V_{IN} = 3.4V$ |
| I_{CCD} | Dynamic Power Supply Current ³ | 0.15 | 0.25 | mA/ mHz | $V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, $\overline{OE} = \text{GND}$, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| I_C | Total Power Supply Current ⁵ | 1.7 | 4.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 2.2 | 6.0 | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |
| | | 7.0 | 12.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling $f_1 = 5\text{MHz}$, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ |
| | | 9.2 | 21.8 ⁴ | mA | $V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, $\overline{OE} = \text{GND}$, $f_1 = 5\text{MHz}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$ |

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$$

$$I_{CC} = \text{Quiescent Current with CMOS input levels}$$

- 1807 Tbl 06
- ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 - D_H = Duty Cycle for TTL Inputs High
 - N_T = Number of TTL Inputs at D_H
 - I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 - f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 - f_1 = Input Frequency
 - N_1 = Number of Inputs at f_1
- All currents are in milliamps and all frequencies are in megahertz.

OUTPUT SELECTION MUX TABLE

| S_1 | S_0 | Output |
|-------|-------|--------|
| 1 | 1 | A1 |
| 1 | 0 | A2 |
| 0 | 1 | B1 |
| 0 | 0 | B2 |

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PIPELINE INSTRUCTION TABLE

| | I = 0 | I = 1 | I = 2 | I = 3 |
|-----------|----------------|--------------|-------|-------|
| P29FCT520 | | | | |
| P29FCT521 | | | | |
| | Single 4-level | Dual 2-level | | Hold |

1807 Tbl 08

AC CHARACTERISTICS (P29FCT520/521)

| Symbol | Parameter | P29FCT520/521 | | | | Units | Fig. No. |
|------------------------|--|-------------------|------|-------------------|------|-------|----------|
| | | MIL | | COM'L | | | |
| | | Min. ¹ | Max. | Min. ¹ | Max. | | |
| t_{PLH} t_{PHL} | Propagation Delay Clock to Data Output | — | 24.0 | — | 21.0 | ns | 5 |
| t_{PLH} t_{PHL} | Propagation Delay S0, S1 To Data Output | — | 22.0 | — | 20.0 | ns | 5 |
| t_S | Setup Time Input Data to Clock | 10.0 | — | 10.0 | — | ns | |
| t_H | Hold Time Input Data to Clock | 10.0 | — | 10.0 | — | ns | |
| t_S | Setup Time Instruction to Clock | 10.0 | — | 10.0 | — | ns | |
| t_H | Hold Time Instruction to Clock | 10.0 | — | 10.0 | — | ns | |
| t_{PHZ} t_{PLZ} | Output Disable Time | — | 14.0 | — | 13.0 | ns | 8, 7 |
| t_{PZH} t_{PZL} | Output Enable Time | — | 22.0 | — | 20.0 | ns | 8, 7 |
| t_w (H) t_w (L) | Clock Pulse Width, High or Low | 10.0 | — | 10.0 | — | ns | 5 |

1807 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
AC Characteristics guaranteed with $C_L = 50\text{pF}$ as shown in Figure 1.

AC CHARACTERISTICS (P29FCT520A/521A—P29FCT520B/521B)

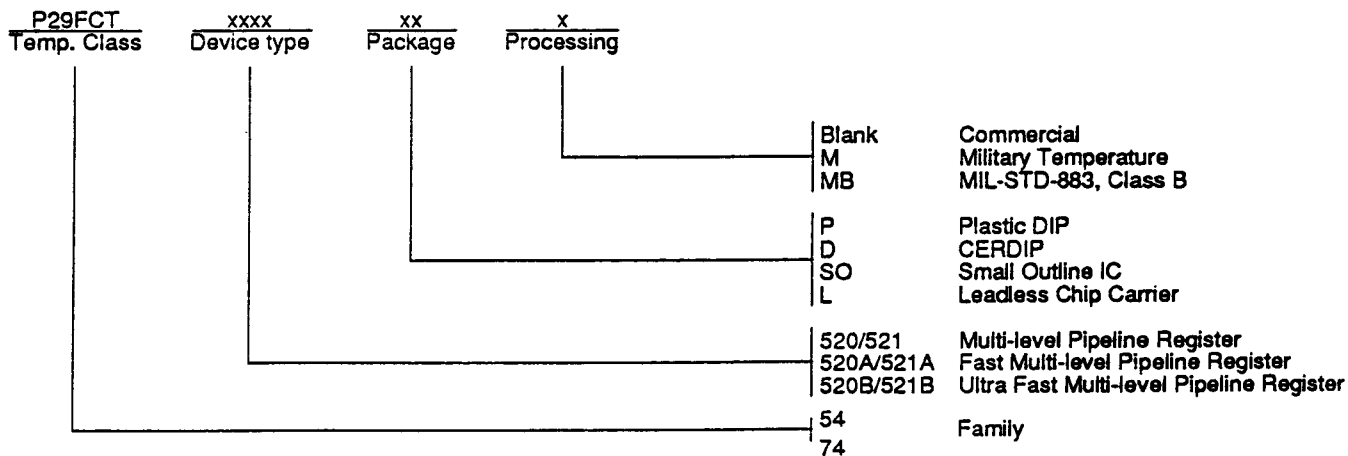
| Symbol | Parameter | P29FCT520A/521A | | | | P29FCT520B/521B | | | | Units | Fig. No. |
|------------------------|---|-------------------|------|-------------------|------|-------------------|------|-------------------|------|-------|----------|
| | | MIL | | COM'L | | MIL | | COM'L | | | |
| | | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | Min. ¹ | Max. | | |
| t_{PLH} t_{PHL} | Clock to Data Output | 2.0 | 16.0 | 2.0 | 14.0 | 2.0 | 8.0 | 2.0 | 7.5 | ns | 5 |
| t_{PLH} t_{PHL} | S0, S1 To Data Output | 2.0 | 15.0 | 2.0 | 13.0 | 2.0 | 8.0 | 2.0 | 7.5 | ns | 5 |
| t_s | Setup Time Input Data to Clock | 6.0 | — | 5.0 | — | 2.8 | — | 2.5 | — | ns | |
| t_H | Hold Time Input Data to Clock | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | |
| t_s | Setup Time Instruction (Reg. Enable) to Clock | 6.0 | — | 5.0 | — | 4.5 | — | 4.0 | — | ns | |
| t_H | Hold Time Instruction (Reg. Enable) to Clock | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | |
| t_{PHZ} t_{PLZ} | Output Disable Time | 6.0 | — | 5.0 | — | 4.5 | — | 4.0 | — | ns | 8, 7 |
| t_{PZH} t_{PZL} | Output Enable Time | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | 8, 7 |
| $t_W(H)$ $t_W(L)$ | Clock Pulse Width, High or Low | 8.0 | — | 7.0 | — | 6.0 | — | 5.5 | — | ns | 5 |

1807 Tbl 10

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
AC Characteristics guaranteed with $C_L = 50pF$ as shown in Figure 1.

ORDERING INFORMATION



1807 03