7-Bit Analog-to-Digital Converter (ADC 7) SDA 7509

Preliminary Data

Type	Ordering Code	Package
SDA 7509	Q67100-H8693	P-DIP-24

The SDA 7509 is a monolithic NMOS 7-bit analog-to-digital converter (ADC) designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22 MHz.

The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge triggered and can be switched into 3-state mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

Features

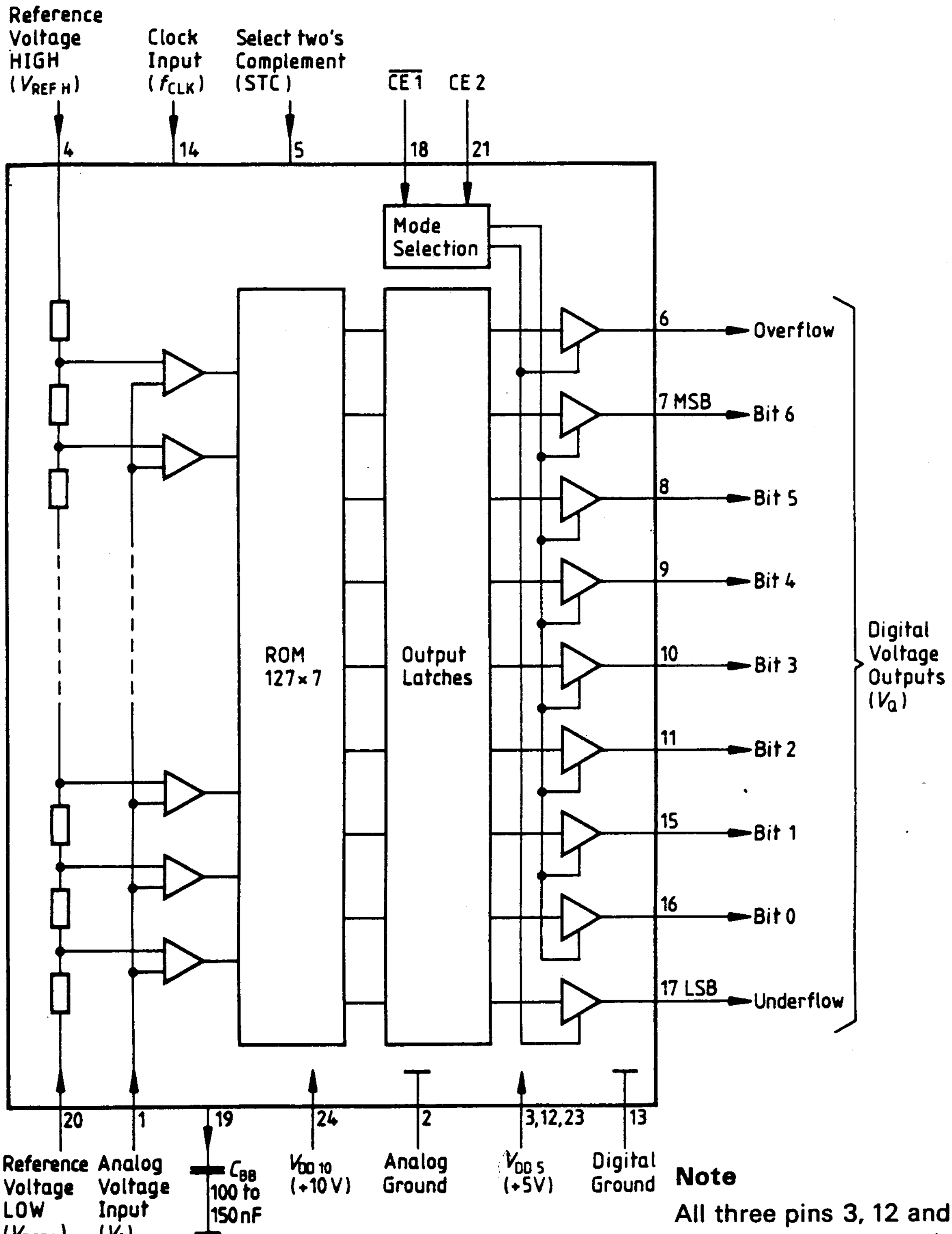
- 7-bit resolution
- No external sample and hold required
- High input impedance
- Binary or two's complement 3-state TTL outputs
- Overflow and underflow 3-state TTL outputs
- All outputs positive-edge triggered
- Standard 24-pin package

Applications

- High-speed A/D conversion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research

Block Diagram

Figure 1

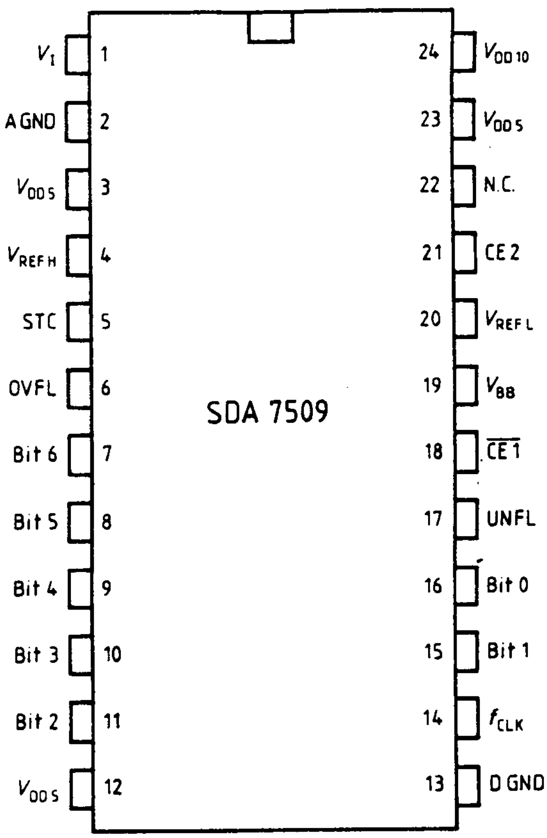


Note

All three pins 3, 12 and 23 must be connected to positive supply voltage + 5 V.

Pin Configuration

Figure 2



Pin Description

Pin	Symbol	Function
1	V_I	Analog voltage input
2	AGND	Analog ground
3	V_{DD5}	Positive supply voltage (+5 V)
4	$V_{REF\,H}$	Reference voltage HIGH
5	STC	Select two's complement
6	OVFL	Overflow
7	Bit 6	Most-significant bit (MSB)
8	Bit 5	
9	Bit 4	
10	Bit 3	
11	Bit 2	
12	V_{DD5}	Positive supply voltage (+5 V)
13	D GND	Digital ground
14	f_{CLK}	Clock input
15	Bit 1	
16	Bit 0	Least-significant bit (LSB)
17	UNFL	Underflow
18	$\overline{CE\,1}$	Chip enable input 1
19	V_{BB}	Back bias output
20	$V_{REF\,L}$	Reference voltage LOW
21	CE 2	Chip enable input 2
22	N.C.	Not connected
23	V_{DD5}	Positive supply voltage (+5 V)
24	V_{DD10}	Positive supply voltage (+10 V)

Maximum Ratings

T_A = 0 to 70 °C (all voltages are referenced to V_{SS})

Description	Symbol	min.	max.	Unit
Supply voltage range (pins 3, 12, 23)	V_{DD5}	−0.5	7	V
Supply voltage range (pin 24)	V_{DD10}	−0.5	12	V
Input voltage range	V_I	−0.5	7	V
Output current	I_Q		5	mA
Total power dissipation	P_{tot}		1	W
Storage temperature range	T_{stg}	−65	150	°C

MOS Handling

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

Maximum ratings are absolute ratings; exceeding even one of these values may cause irreversible damage to the integrated circuit. In the operating range the functions given in the circuit description will be fulfilled. However, deviations from the characteristics are possible.

Operating Range

Description	Symbol	min.	max.	Unit
Supply voltage range (pins 3, 12, 23)	V_{DD5}	4.5	5.5	V
Supply voltage (pin 24)	V_{DD10}	9.5	10.5	V
Supply current (pins 3, 12, 23)	I_{DD5}		85	mA
Supply current (pin 24)	I_{DD10}		18	mA
Ambient temperature	T_A	0	70	°C

Characteristics

$V_{DD5} = V_{3,12,23\text{-}13} = 4.5$ to 5.5 V; $V_{DD10} = V_{24\text{-}2} = 9.5$ to 10.5 V; $C_{BB} = 100$ nF;
$T_A = 0$ to $+70$ °C

Description	Symbol	min.	typ.	max.	Unit
Reference voltages					
L reference voltage (pin 20)	$V_{REF\,L}$	2.4	2.5	2.6	V
H reference voltage (pin 4)	$V_{REF\,H}$	5.0	5.1	5.2	V
Reference current	I_{REF}	150		450	µA

Input signals

Description	Symbol	min.	typ.	max.	Unit
Clock input (pin 14)					
L input voltage	V_{IL}	−0,3		0.8	V
H input voltage[1]	V_{IH}	3.0		V_{DD5}	V
Digital input levels (pins 5, 18, 21)[2]					
L input voltage	V_{IL}	0		0.8	V
H input voltage	V_{IH}	2.0		V_{DD5}	V
Input current					
at $V_5 = 0$ V; V_{13} = GND	$-I_5$	15		70	µA
at $V_{18} = 5$ V; V_{13} = GND	I_{18}	15		70	µA
at $V_{21} = 0$ V; V_{13} = GND	$-I_{21}$	25		120	µA
Input leakage current					
(except pins 5, 18 and 21)	I_{LI}			10	µA
Analog input levels (pin 1)					
at $V_{REF\,L} = 2.5$ V; $V_{REF\,H} = 5.1$ V					
Input voltage amplitude					
(peak-to-peak value)	$V_{I(p\text{-}p)}$		2.6		V
Input capacitance[3]	$C_{1\text{-}2}$			60	pF

[1] Maximum input voltage must not exceed 5.0 V.
[2] If pin 5 is LOW binary coding is selected.
If pin 5 is HIGH two's complement is selected.
If pin 5, 18 and 21 are open-circuit, pin 5, 21 are HIGH and pin 18 is LOW.
For output coding see **table 1** and mode selection see **table 2.**
[3] Tested on sample base.

Description	Symbol	min.	max.	Unit
Outputs				
Digital voltage outputs (pins 6 to 11 and 15 to 17)				
L output voltage at I_Q = 2 mA	V_{QL}	0	–0.4	V
H output voltage at $-I_Q$ = 0.5 mA	V_{QL}	2.4	V_{DD5}	V

Table 1 Output Coding ($V_{REF\,L}$ = 2.50 V; $V_{REF\,H}$ = 5.08 V)

Step	$V_{1\text{-}2}$ [1]	UNFL	OVFL	Binary bit 6 – bit 0	Two's complement bit 6 – bit 0	
Underflow	<2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0	
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1	
.	.	.	.	. . . .	. . . .	Steps
.	.	.	.	. . . .	. . . .	2-125
.	.	.	.	. . . .	. . . .	
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0	
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1	
Overflow	≥5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1	

[1] Approximate values.

Table 2 Mode Selection

$\overline{\text{CE 1}}$	CE 2	bit 0 to bit 6	UNFL, OVFL
X	0	HIGH impedance	HIGH impedance
0	1	active	active
1	1	HIGH impedance	active

Characteristics

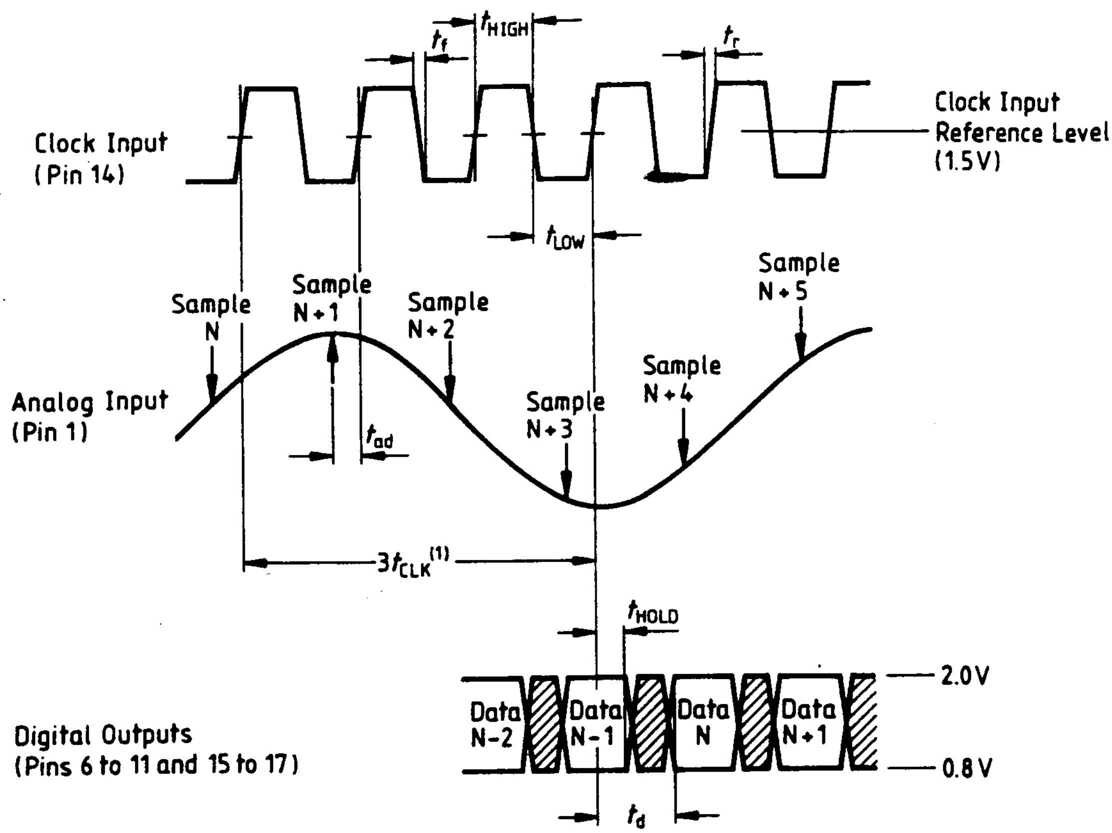
$V_{DD5} = V_{3,12,23\text{-}13} = 4.5$ to 5.5 V; $V_{DD10} = V_{24\text{-}2} = 9.5$ V to 10.5 V; $V_{REF\,L} = 2.5$ V; $V_{REF\,H} = 5.1$ V; $f_{CLK} = 22$ MHz; $C_{BB} = 100$ nF; $T_A = 0$ to $+70$ °C

Description	Symbol	min.	max.	Unit
Switching characteristics (see also fig. 3)				
Clock input (pin 14)				
Clock frequency	f_{CLK}	1	22	MHz
L clock cycle time	t_{LOW}	20		ns
H clock cycle time	t_{HIGH}	20		ns
Input rise and fall times (pin 1)				
rise time	t_r		3	ns
fall time	t_f		3	ns
Analog input[1]				
Bandwidth (– 3 dB)	B	11		MHz
Differential gain[2]	*dG*		±5	%
Differential phase[2]	*dP*		±2.5	deg
Phase error[3]	P_e		±12	deg
Non-harmonic noise			–36	dB
Peak error (non-harmonic noise)			3	LSB
Harmonics (full scale)				
fundamental	f_0		0	dB
r.m.s. (2nd + 3rd harmonic)	$f_{2,3}$		–28	dB
r.m.s. (4th + 5th + 6th + 7th harmonic)	$f_{4\text{-}7}$		–35	dB
Digital outputs[1] [4]				
Output hold time	t_{HOLD}	6		ns
Output delay time at $C_L = 15$ pF	t_d		38	ns
Output delay time at $C_L = 50$ pF	t_d		48	ns
3-state delay time	t_{dt}		25	ns
Capacitive output load	C_{QL}	0	15	pF
Transfer function				
Non-linearity at $f_i = 1.1$ kHz				
integral	INL		±½	LSB
differential	DNL		±½	LSB

[1] Clock input rise and fall times are at the maximum clock frequency (10 % and 90 % levels).
[2] Low frequency sinewave (peak-to-peak value of the analog input voltage at $V_{I(p\text{-}p)} = 1.8$ V) combined with a sinewave voltage ($V_{I(p\text{-}p)} = 0.7$ V) at $f_i = 5$ MHz.
[3] Sinewave voltage with increasing amplitude at $f_i = 5$ MHz (minimum amplitude $V_{I(p\text{-}p)} = 0.25$ V; maximum amplitude $V_{I(p\text{-}p)} = 2.5$ V).
[4] The timing values of the digital outputs at pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5 V.

Timing Diagram

Figure 3



(1) There is a delay of 3 clock cycles between sampling of an analog input signal and the corresponding digital output.

Application Note

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behaviour under nominal conditions; V_{DD5} = 5 V, V_{DD10} = 10 V.

Description	Symbol	typ.	Unit
Supply			
Supply current (pins 3, 12, 23)	I_{DD5}	55	mA
Supply current (pin 24)	I_{DD10}	12	mA
Maximum clock frequency	f_{CLK}	25	MHz
Bandwidth (– 3 dB)	B	20	MHz
Total power dissipation	P_{tot}	400	mW
Peak error (non-harmonic noise)		1.5	LSB
Suppression of harmonics			
sum of:			
$f_{2nd} + f_{3rd}$		31	dB
$f_{4th} + f_{5th} + f_{6th} + f_{7th}$		39	dB
Non-linearity			
integral	INL	± ¼	LSB
differential	DNL	± ⅓	LSB
Differential gain	*dG*	± 3	%
Differential phase	*dP*	± 1	%
Large signal phase error	P_e	10	deg
Non-harmonic noise		40	dB

Application Note (cont'd)

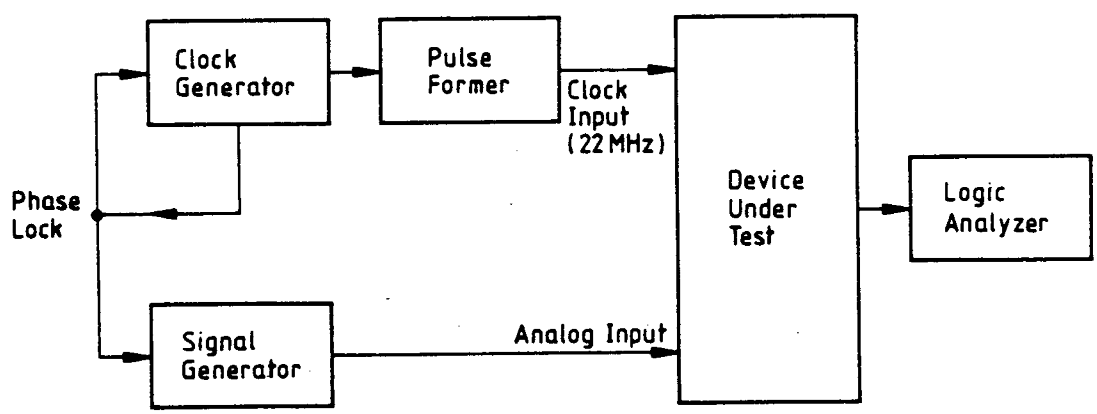
Test Philosophy

Figure 4 is a block diagram showing analog-to-digital testing with a phase locked signal source. The signal generator provides a 5 MHz sinewave for the device under test (except for the linearity test). The 22 MHz clock input is provided by the clock generator. The phase relationship between signal and clock generator is shifted by 100 pico sec. each signal period to provide an effective clock rate of 10 GHz for analysis.
Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.
The successive processing completes the specific measurement **(figures 5, 6, 7 and 8)**.

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps the output signal of the converter randomly switches.
After lowpass filtering the different step width is used for calculating the line of least squares to obtain integral non-linearity.
To calculate differential non-linearity a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation **(figure 7)**.

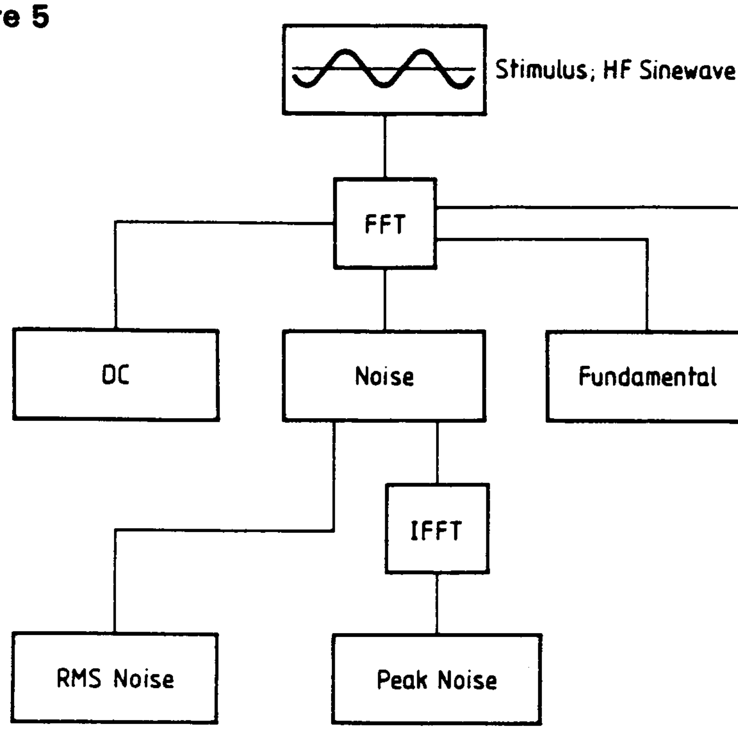
Analog-to-Digital Converter Testing with Locked Signal Source.

Figure 4



Sinewave Test; Non-Harmonic Noise and Peak Error

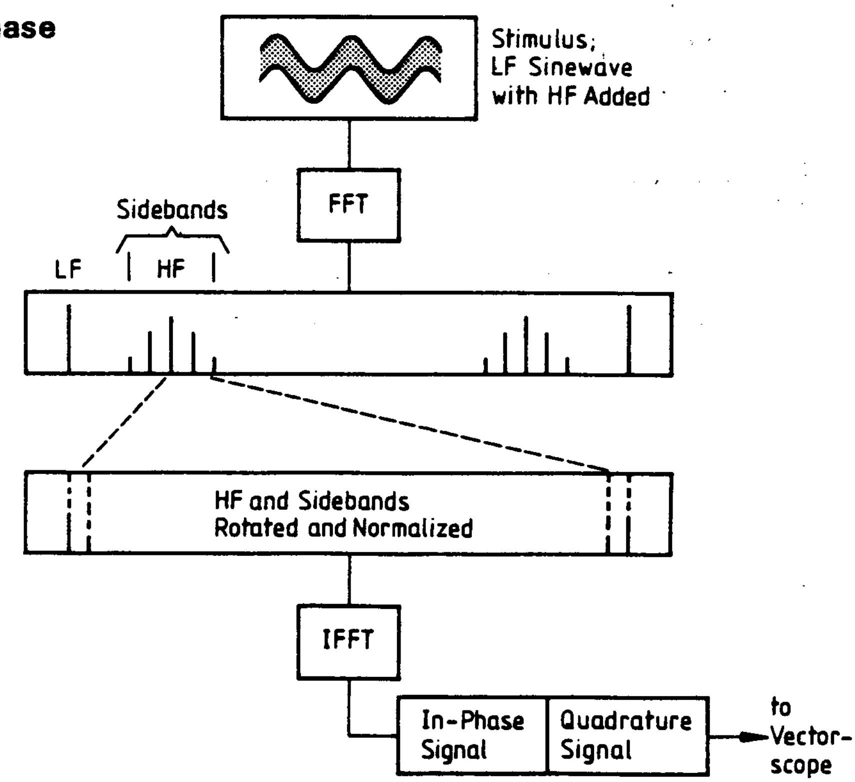
Figure 5



Where : FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Differential Gain and Phase

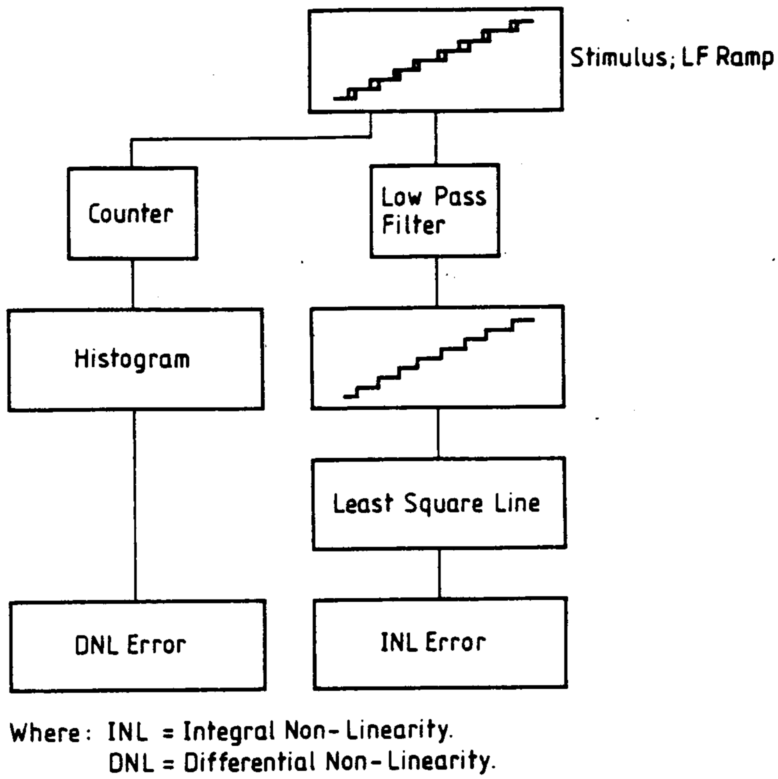
Figure 6



Application Note (cont'd)

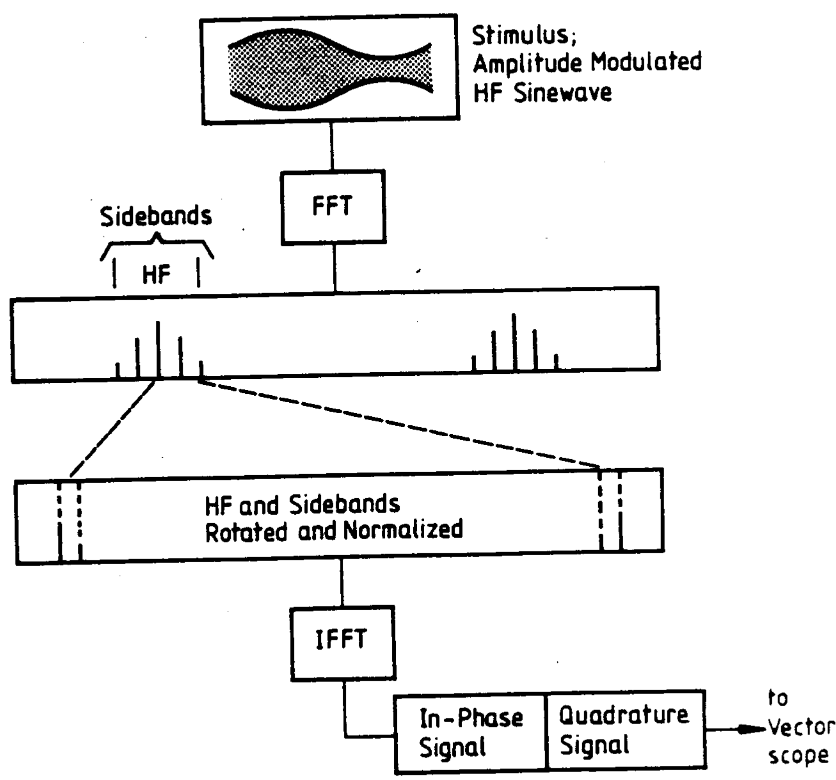
Low Frequency Ramp Test; Linearity

Figure 7

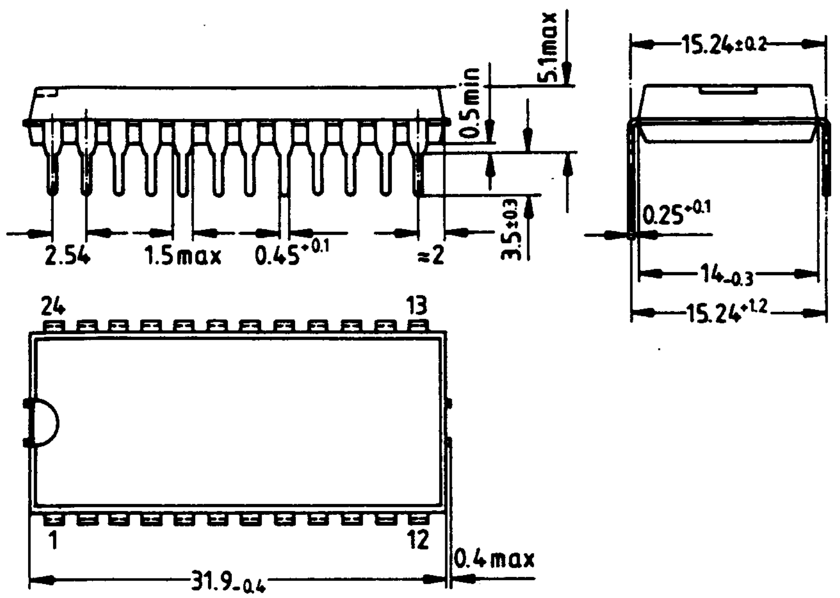


Large Signal Phase Error

Figure 8



Plastic Dual-in-Line Package P-DIP-24
20 B 24 DIN 41870T 10



Approx. weight 2.5 g
Dimension in mm

Published by Siemens AG, Bereich Bauelemente, Vertrieb, Produkt-Information, Balanstraße 73, D-8000 München 80.

As far as patents or other rights of third parties are concerned, liability is only assumed for components per se, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery, and prices please contact the Offices of Siemens Aktiengesellschaft in the Federal Republic of Germany and Berlin (West) or the Siemens Companies and Representatives worldwide.

Due to technical requirements components may contain dangerous substances. For information on the type in question please contact your nearest Siemens Office, Components Division.