

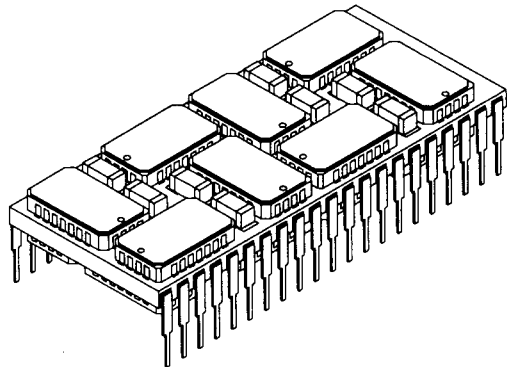
DESCRIPTION:

The DPS1037 is a 64K X 16 high-speed, low-power static RAM module comprised of sixteen 64K X 1 monolithic SRAM's, and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

The DPS1037 operates from a single +5V supply and all input and output pins are completely TTL-compatible. The DPS1037 is best suited for high speed military computers and signal processing applications.

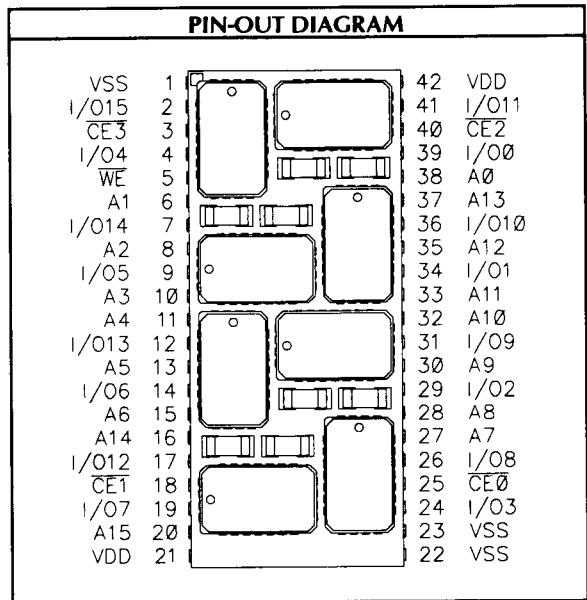
FEATURES:

- Organizations available:
64K X 16, 128K X 8, or 256K X 4
- Access Times: 15*, 25, 35, 45, 55ns (max.)
- Low Power Dissipation
- Completely Static Operation - No Clock or Refresh Needed
- Three State Output
- All Inputs and Outputs are TTL-Compatible
- 900 mil, 42-pin DIP pinout
- Commercial Only

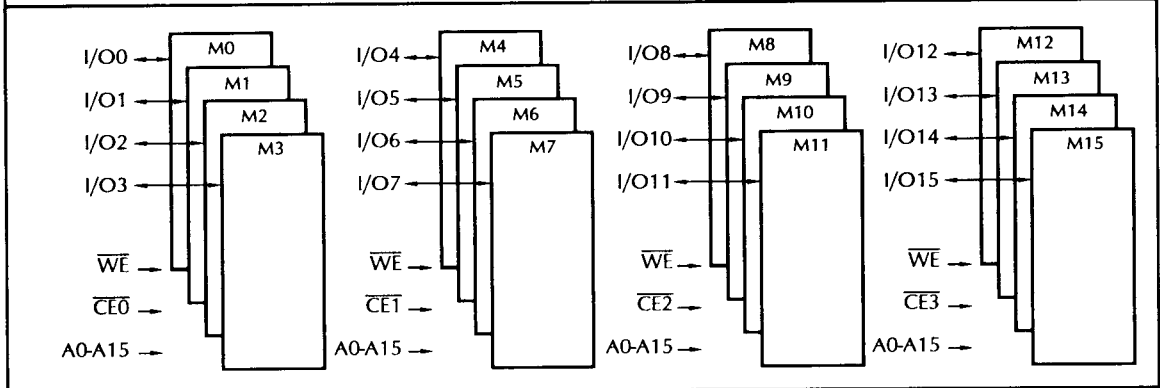


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PIN NAMES	
A0 - A15	Address Inputs
I/O0 - I/O15	Data Input/Output
CE0 - CE3	Chip Enables
WE	Write Enable
VDD	Power (+5V)
Vss	Ground



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE ¹					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.5	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	160	pF	V _{IN} = 0V
C _{CE}	Chip Enable	50		
C _{WE}	Write Enable	80		
C _{I/O}	Data Input/Output	30		

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to + 150	°C
T _{BIAS}	Temperature Under Bias	-55 to + 125	°C
V _{DD}	Supply Voltage ¹	-0.5 to + 7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} + 0.5	V

TRUTH TABLE				
Mode	\overline{CE}	WE	I/O Pin	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	D _{OUT}	Active
Write	L	L	D _{IN}	Active

H=HIGH L=LOW X=Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	X4		X8		X16		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-160	+160	-160	+160	-160	+160	µA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , \overline{CE} or \overline{OE} = V _{IH} , or WE = V _{IL}	-40	+40	-20	+20	-10	+10	µA
I _{CC1}	Operating Power Supply Current	\overline{CE} = V _{IL} , f = 0 Outputs Open		1080		1280		1680	mA
I _{CC2}	Dynamic Operating Supply Current	Outputs Open \overline{CE} = V _{IL} , f = max.		1340		1640		2240	mA
I _{SB1}	Standby Supply Current (TTL)	\overline{CE} = V _{IH}		880		880		880	mA
I _{SB2}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V, \overline{CE} ≥ V _{DD} -0.2V		400		400		400	mA
V _{OL}	Output Low Voltage	V _{OL} = 8.0mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	V _{OH} = -4.0mA	2.4		2.4		2.4		V

NOTE: DensePac has other specialized suppliers that may provide better A.C. or D.C. Characteristics.

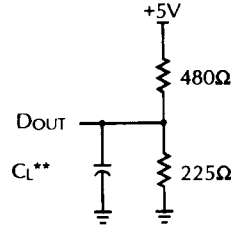
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

Output Load		
Load	C _L	Parameters Measured
1	30 pF	except t _{CHZ} , t _{CLZ} , t _{WHZ} , and t _{WLZ}
2	5 pF	t _{CHZ} , t _{CLZ} , t _{WHZ} , and t _{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.

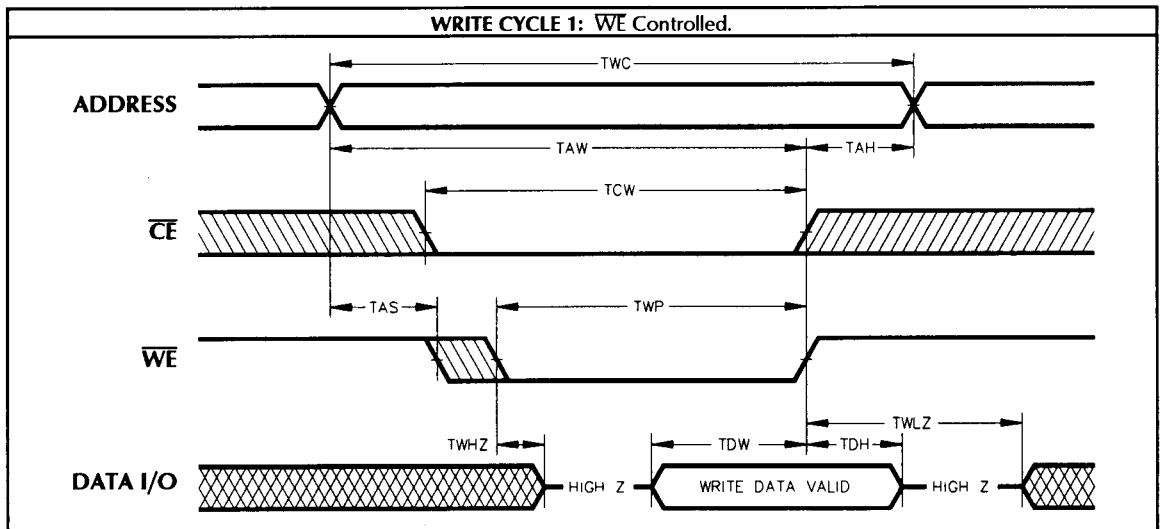
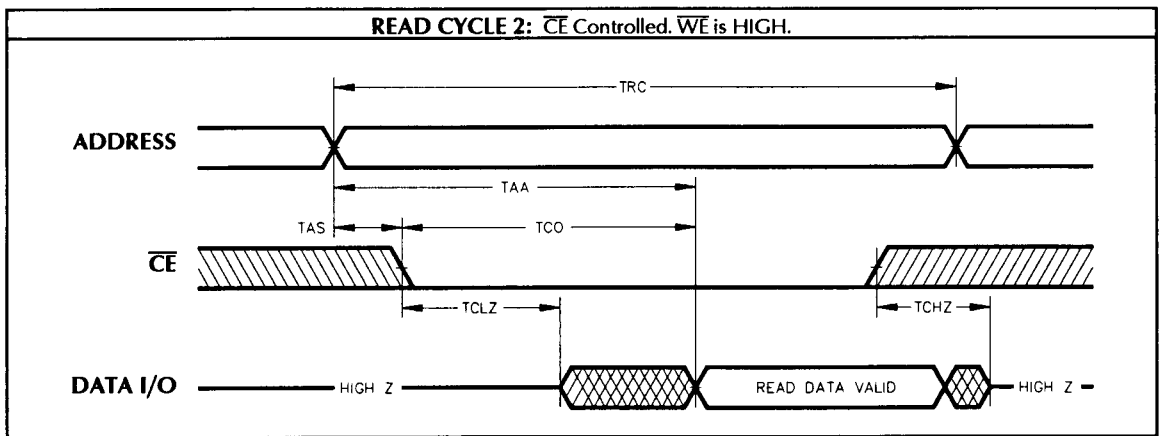
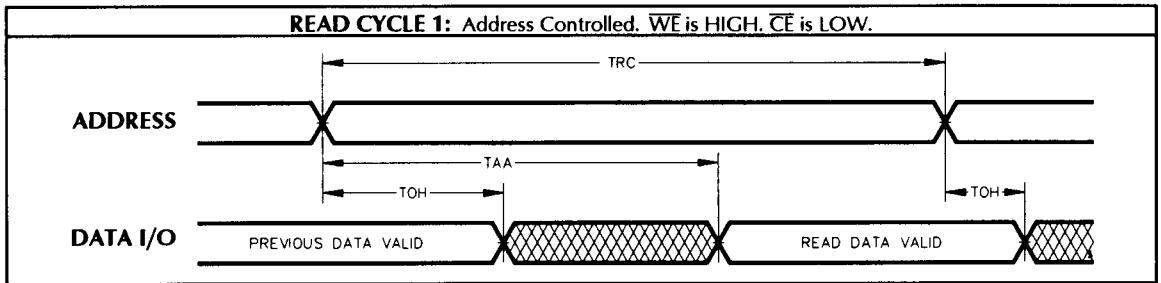


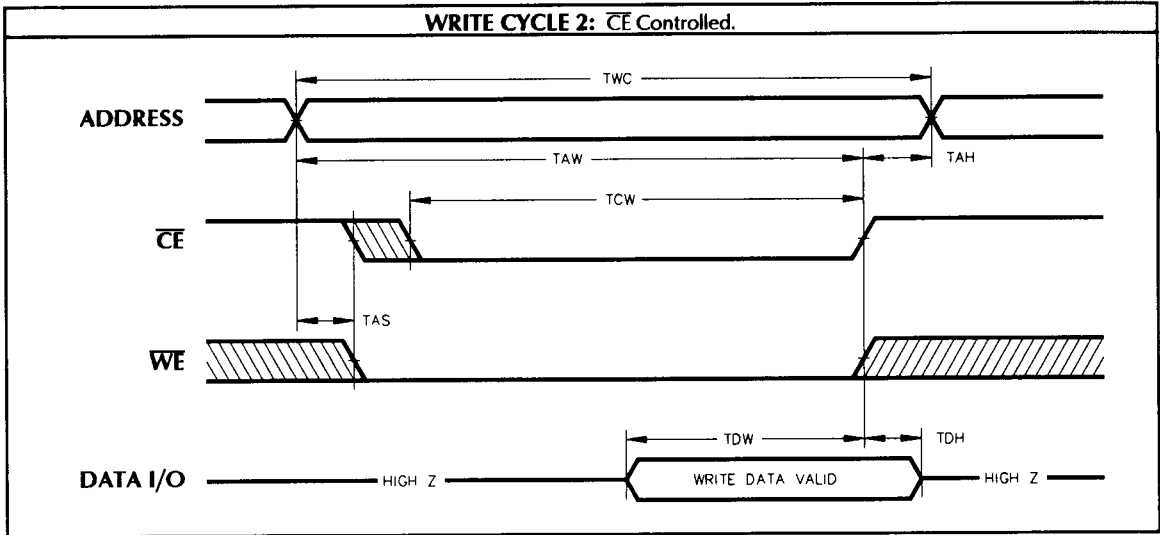
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AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	-15		-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	15		25		35		45		55		ns
2	t _{AA}	Address Access Time		15		25		35		45		55	ns
3	t _{CO}	Chip Enable to Output Valid		15		25		35		45		55	ns
4	t _{OH}	Output Hold for Address Change	5		5		5		5		5		ns
5	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		5		ns
6	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4, 6}		8		15		20		35		35	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷													
No.	Symbol	Parameter	-15		-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	15		25		35		45		55		ns
11	t _{AW}	Address Valid to End of Write	12		20		30		40		50		ns
12	t _{CW}	Chip Enable to End of Write	12		20		30		40		50		ns
13	t _{DW}	Data Valid to End of Write	14		25		25		25		25		ns
14	t _{DH}	Data Hold Time	0		0		0		0		0		ns
15	t _{WP}	Write Pulse Width	10		15		20		25		35		ns
16	t _{AS}	Address Set-up Time**	5		5		5		5		5		ns
17	t _{AH}	Address Hold Time	5		5		5		5		5		ns
18	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4, 6}		15		20		20		25		25	ns
19	t _{WLZ}	Write Enable to Output in LOW-Z ^{4, 6}	5		5		5		5		5		ns

*** Valid for both Read and Write Cycles.

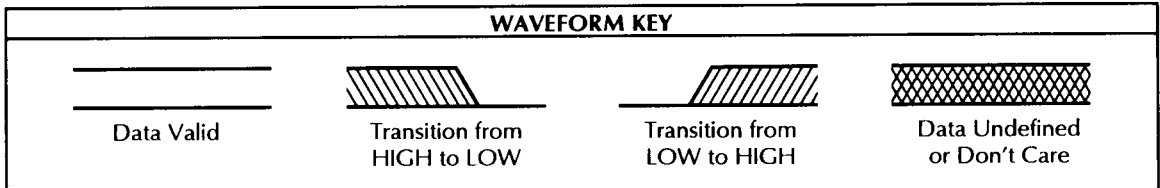




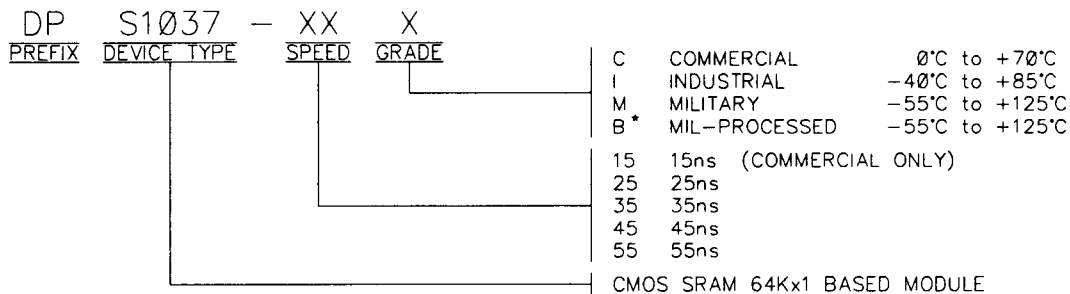
NOTES:

1. All voltages are with respect to V_{SS} .
2. -3.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage.
6. When \overline{CE} is LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.

WAVEFORM KEY

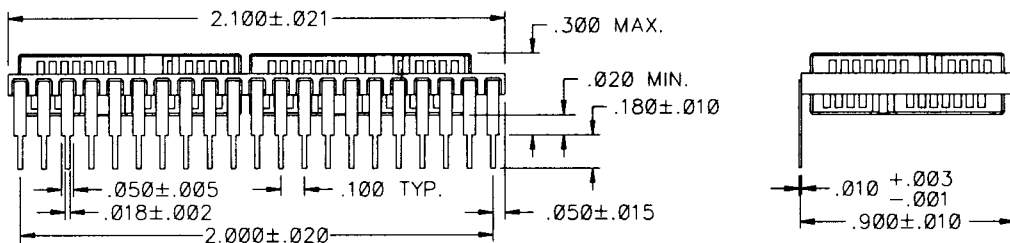


PART NUMBERING SYSTEM



* B grade modules are constructed with 883 devices.

MECHANICAL DRAWING



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