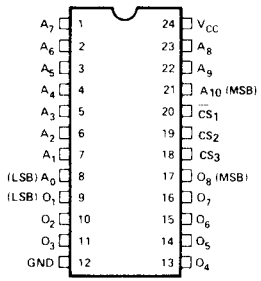
M3636
16K (2K x 8) BIPOLAR PROM

- **−55°C to +125°C Operation**
- **Fast Access Time: 80ns Maximum**
- **Low Power Dissipation: 0.05mW/Bit Typically**
- **Three Chip Select Inputs for Easy Memory Expansion**
- **Pin Compatible to 8K PROMs**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability/Higher Programmability**

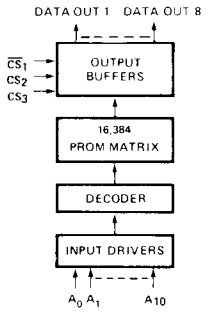
The Intel® M3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 80 ns is specified over the − 55°C to + 125°C temperature range and 5% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit M3636, the highest density bipolar PROM available was 8196 bits. The high density of the M3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8-bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The M3636 is packaged in a hermetic 24-pin dual in-line package.

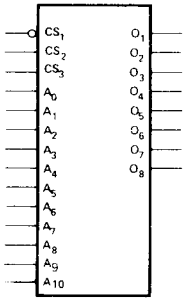
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$\overline{CS}_1, CS_2, CS_3$	CHIP SELECT INPUTS[1]
$\overline{O}_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$

A.C. CHARACTERISTICS $V_{CC} = +5V \pm 5\%$, $T_A = -55°C$ to $125°C$

SYMBOL	PARAMETER	MAX. LIMITS	UNIT	CONDITIONS
T_A	Address to Output Delay	80	ns	$\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	50	ns	
t_{DIS}	Output Disable Time	50	ns	

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

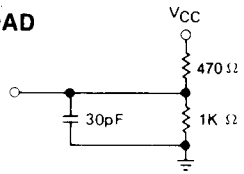
SYMBOL	PARAMETER	TYP. LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

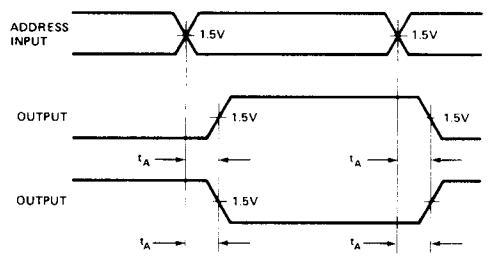
Conditions of Test:
Input pulse amplitudes 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test – 2.5 MHz

10 mA TEST LOAD



WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY