

- Organization . . . 1048576 × 4
- Single 5-V Power Supply ( $\pm 10\%$  Tolerance)
- Performance Ranges:

	ACCESS TIME (t <sub>RAC</sub> ) (MAX)	ACCESS TIME (t <sub>CAC</sub> ) (MAX)	ACCESS TIME (t <sub>AA</sub> ) (MAX)	EDO CYCLE (t <sub>HPC</sub> ) (MIN)
'44409/P-60	60 ns	15 ns	30 ns	25 ns
'44409/P-70	70 ns	18 ns	35 ns	30 ns
'44409/P-80	80 ns	20 ns	40 ns	35 ns

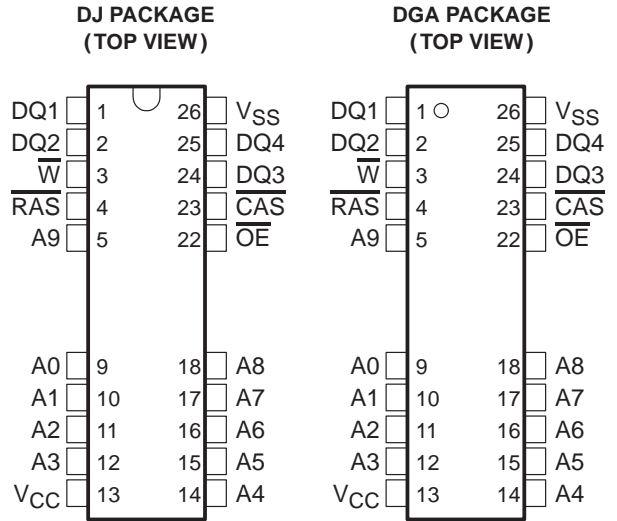
- Extended Data Out (EDO) Operation
- CAS-Before-RAS (CBR) Refresh
- 3-State Unlatched Output
- Low Power Dissipation
- All Inputs/Outputs and Clocks are TTL-Compatible
- Long Refresh Period
  - 1 024 Cycle Refresh in 16 ns (max)
  - 128 ms on Low Power, Self-Refresh Version (TMS44409P Only)
- Operating Free-Air Temperature Range 0°C to 70°C

**description**

The TMS44409 is a high-speed 4194304-bit dynamic random-access memory (DRAM) organized as 1048576 words of four bits each. This device features maximum RAS access times of 60 ns, 70 ns and 80 ns. Maximum power consumption is as low as 385 mW operating and 6 mW standby. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS44409P is a high-speed, low-power, self-refresh version of the TMS44409 DRAM.

All versions of the TMS44409/P are offered in a 300-mil 20/26 J-lead plastic surface-mount SOJ package (DJ suffix) and a 20/26-lead plastic small outline package (DGA suffix). These devices are characterized for operation from 0°C to 70°C.



PIN NOMENCLATURE	
A0–A9	Address Inputs
CAS	Column-Address Strobe
DQ1 – DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V <sub>CC</sub>	5-V Supply
V <sub>SS</sub>	Ground
$\overline{W}$	Write Enable

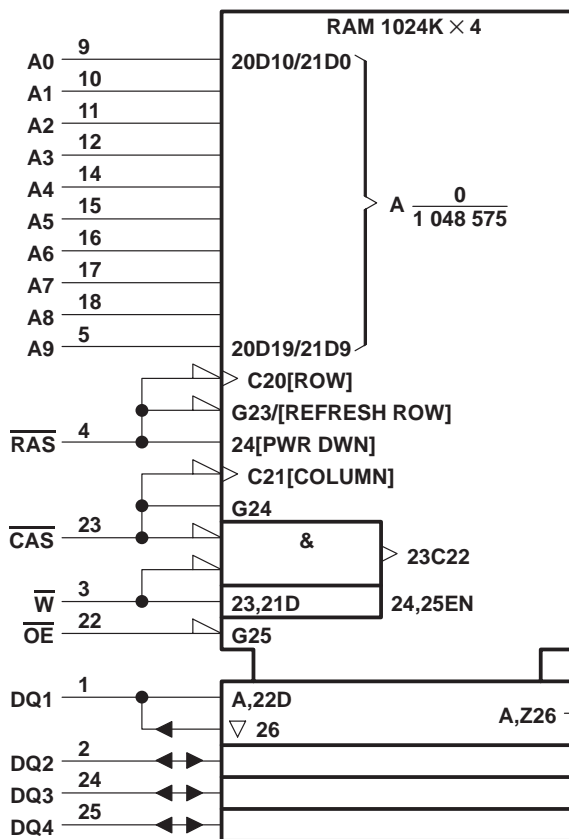
**ADVANCE INFORMATION**

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.



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 1048576-WORD BY 4-BIT  
 DYNAMIC RANDOM-ACCESS MEMORY  
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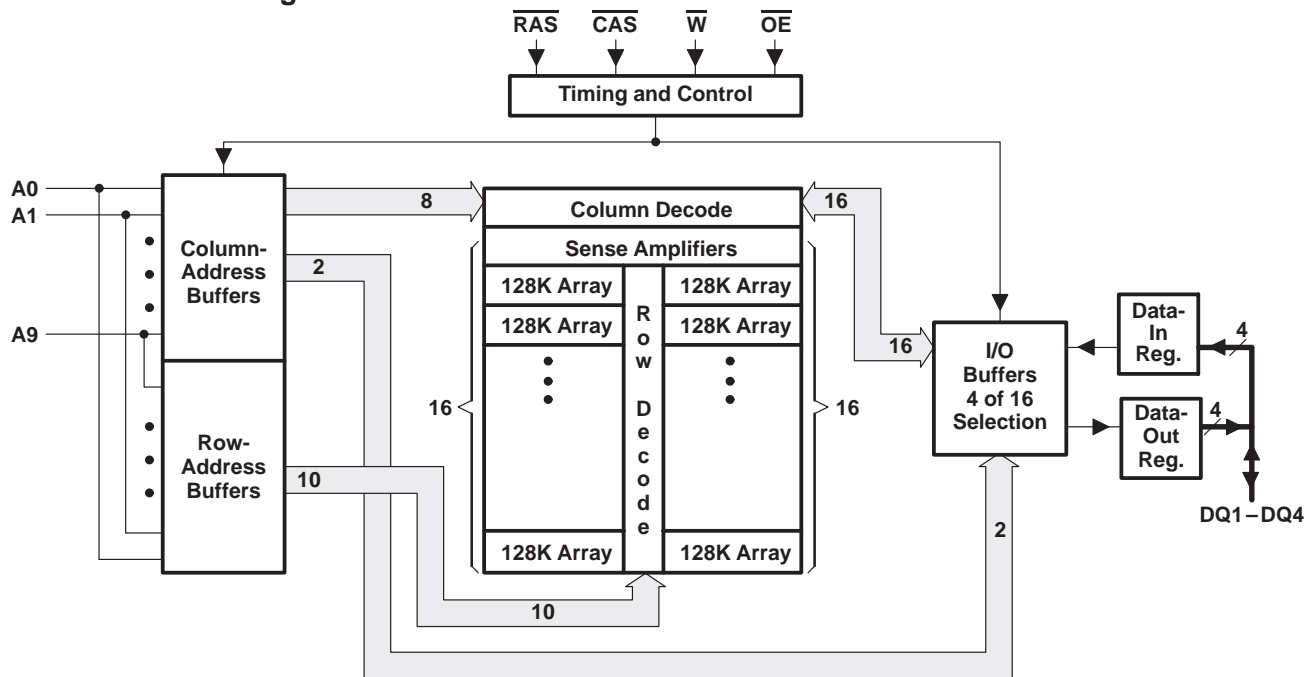
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

ADVANCE INFORMATION

functional block diagram



operation

extended data out

Extended data out allows for data output rates of up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by  $t_{RASP}$ , the maximum RAS low time.

Extended data out does not place the DQs into the high-impedance state with the rising edge of  $\overline{CAS}$ . The output remains valid for the system to latch the data. After  $\overline{CAS}$  goes high, the DRAM decodes the next address.  $\overline{OE}$  and  $\overline{W}$  can be used to control the output impedance. Descriptions of  $\overline{OE}$  and  $\overline{W}$  further explain EDO operation benefit.

address (A0–A9)

Twenty address bits are required to decode one of 1048576 storage cell locations. Ten row-address bits are set up on A0 through A9 and latched onto the chip by the row-address strobe ( $\overline{RAS}$ ). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ( $\overline{CAS}$ ). All addresses must be stable on or before the falling edges of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip-enable in that it activates the sense amplifiers as well as the row decoder.

output enable ( $\overline{OE}$ )

$\overline{OE}$  controls the impedance of the output buffers. While  $\overline{CAS}$  and  $\overline{RAS}$  are low and  $\overline{W}$  is high,  $\overline{OE}$  can be brought low or high and the DQs transition between valid data and high impedance (see Figure 7). There are two methods for placing the DQs into the high-impedance state and keeping them that way during  $\overline{CAS}$  high time. The first method is to transition  $\overline{OE}$  high before  $\overline{CAS}$  transitions high and keep  $\overline{OE}$  high for  $t_{CHO}$  past the  $\overline{CAS}$  transition. This disables the DQs and they remain disabled, regardless of  $\overline{OE}$ , until  $\overline{CAS}$  falls again. The second method is to have  $\overline{OE}$  low as  $\overline{CAS}$  transitions high. Then  $\overline{OE}$  can pulse high for a minimum of  $t_{OEP}$  anytime during  $\overline{CAS}$  high time, thus, disabling the DQs regardless of further transitions on  $\overline{OE}$  until  $\overline{CAS}$  falls again (see Figure 7).

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#### write enable ( $\overline{W}$ )

The read or write mode is selected through the write-enable ( $\overline{W}$ ) input. A logic high on the  $\overline{W}$  input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$  (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation independent of the state of  $\overline{OE}$ . This permits early-write operation to be completed with  $\overline{OE}$  grounded. If  $\overline{W}$  goes low in an extended-data-out read cycle, the DQs are disabled so long as  $\overline{CAS}$  is high (see Figure 8).

#### data in/data out (DQ1–DQ4)

Data is written during a write or a read-modify-write cycle. Depending on the mode of operation, data is strobed in by the later falling edge of  $\overline{CAS}$  or  $\overline{W}$  with setup and hold times referenced to the latter edge. The DQs drive valid data after all access times are met and remain valid except in the cases described in the  $\overline{W}$  and  $\overline{OE}$  descriptions (above).

#### refresh

A refresh operation must be performed at least once every 16 ms to retain data. This is achieved by strobing each of the 1 024 rows (A0–A9). A normal read or write cycle refreshes all bits in each row that is selected. A  $\overline{RAS}$ -only operation can be used by holding  $\overline{CAS}$  at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a  $\overline{RAS}$ -only refresh. Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding  $\overline{CAS}$  at  $V_{IL}$  after a read operation and cycling  $\overline{RAS}$  after a specified precharge period, similar to a  $\overline{RAS}$ -only refresh cycle. The external address is ignored during the hidden-refresh cycle.

#### $\overline{CAS}$ -before- $\overline{RAS}$ (CBR) refresh

CBR refresh is utilized by bringing  $\overline{CAS}$  low earlier than  $\overline{RAS}$  (see parameter  $t_{CSR}$ ) and holding it low after  $\overline{RAS}$  falls (see parameter  $t_{CHR}$ ). For successive CBR-refresh cycles,  $\overline{CAS}$  can remain low while cycling  $\overline{RAS}$ . The external address is ignored and the refresh address is generated internally.

#### self-refresh (TMS44409P)

The self-refresh mode is entered by dropping  $\overline{CAS}$  low prior to  $\overline{RAS}$  going low.  $\overline{CAS}$  and  $\overline{RAS}$  are both held low for a minimum of 100  $\mu$ s. The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both  $\overline{RAS}$  and  $\overline{CAS}$  are brought high to satisfy  $t_{CHS}$ . Upon exiting the self-refresh mode, a burst refresh (refresh of a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

#### power up

To achieve proper device operation, an initial pause of 200  $\mu$ s followed by a minimum of eight initialization cycles is required after power up to the full  $V_{CC}$  level is achieved. These eight initialization cycles need to include at least one refresh ( $\overline{RAS}$  only or CBR) cycle.

#### test mode

A design for test (DFT) mode is incorporated in the TMS44409. A CBR with  $\overline{W}$  low (WCBR) cycle is used to enter the test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins go high. If any one bit is different, a DQ pin goes low. Any combination of read, write, read-write, or page-mode can be used in the test mode. The test-mode function reduces test times by enabling the 1-megabit  $\times$  4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A  $\overline{RAS}$ -only or CBR-refresh cycle is used to exit the DFT mode.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Voltage range on any pin (see Note 1)	– 1 V to 7 V
Voltage range on V <sub>CC</sub>	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>stg</sub>	– 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V<sub>SS</sub>.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply voltage	4.5	5	5.5	V
V <sub>IH</sub> High-level input voltage	2.4		6.5	V
V <sub>IL</sub> Low-level input voltage (see Note 2)	– 1		0.8	V
T <sub>A</sub> Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	High-level output voltage I <sub>OH</sub> = -5 mA	2.4		2.4		2.4		V	
V <sub>OL</sub>	Low-level output voltage I <sub>OL</sub> = 4.2 mA	0.4		0.4		0.4		V	
I <sub>I</sub>	Input current (leakage) V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V, All other pins = 0 V to V <sub>CC</sub>	± 10		± 10		± 10		mA	
I <sub>O</sub>	Output current (leakage) V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to 6.5 V, CAS high	± 10		± 10		± 10		µA	
I <sub>CC1</sub> †	Read- or write-cycle current (see Note 3) V <sub>CC</sub> = 5.5 V, t <sub>RWC</sub> = MIN	105		90		80		mA	
I <sub>CC2</sub>	Standby current After 1 memory cycle, RAS and CAS high, V <sub>IH</sub> = 2.4 V	TTL		2		2		mA	
		CMOS	'44409		1		1		mA
			'44409P		500		500		µA
I <sub>CC3</sub>	Average refresh current (RAS only or CBR) (see Note 3) V <sub>CC</sub> = 5.5 V, t <sub>RWC</sub> = MIN, RAS cycling, CAS high (RAS only); RAS low after CAS low (CBR)	105		90		80		mA	
I <sub>CC4</sub> †	Average EDO page current (see Note 4) V <sub>CC</sub> = 5.5 V, t <sub>HPC</sub> = MIN, RAS low, CAS cycling	90		80		70		mA	
I <sub>CC6</sub> ‡	Self-refresh current CAS, RAS < 0.2 V, Measured after t <sub>RASS</sub> min	500		500		500		µA	
I <sub>CC7</sub> †	Standby current RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> , Data out = enabled	5		5		5		mA	
I <sub>CC10</sub> ‡	Battery-backup current t <sub>RC</sub> = 125 µs, t <sub>RAS</sub> ≤ 1 µs, V <sub>CC</sub> - 0.2 V ≤ V <sub>IH</sub> ≤ 6.5 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V <sub>IH</sub> , Addresses and data stable	500		500		500		µA	

† Measured with outputs open

‡ TMS44409P only

NOTES: 3. Measured with a maximum of one address change while  $\overline{RAS}$  = V<sub>IL</sub>

4. Measured with a maximum of one address change while  $\overline{CAS}$  = V<sub>IH</sub>

**capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)§**

PARAMETER	MIN	MAX	UNIT
C <sub>i(A)</sub> Input capacitance, A0 – A9	5		pF
C <sub>i(OE)</sub> Input capacitance, $\overline{OE}$	7		pF
C <sub>i(RC)</sub> Input capacitance, $\overline{CAS}$ and $\overline{RAS}$	7		pF
C <sub>i(W)</sub> Input capacitance, $\overline{W}$	7		pF
C <sub>O</sub> Output capacitance	7		pF

§ Capacitance measurements are made on a sample basis only.

NOTE 5: V<sub>CC</sub> = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)**

PARAMETER	'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AA</sub> Access time from column address	30		35		40		ns
t <sub>CAC</sub> Access time from $\overline{\text{CAS}}$ low	15		18		20		ns
t <sub>CPA</sub> Access time from column precharge	35		40		45		ns
t <sub>RAC</sub> Access time from $\overline{\text{RAS}}$ low	60		70		80		ns
t <sub>OEa</sub> Access time from $\overline{\text{OE}}$ low	15		18		20		ns
t <sub>CLZ</sub> $\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t <sub>REZ</sub> Output disable time, start of $\overline{\text{RAS}}$ high (see Note 6)	3	15	3	18	3	20	ns
t <sub>CEZ</sub> Output disable time, start of $\overline{\text{CAS}}$ high (see Note 6)	3	15	3	18	3	20	ns
t <sub>OEZ</sub> Output disable time after $\overline{\text{OE}}$ high (see Note 6)	3	15	3	18	3	20	ns
t <sub>WEZ</sub> Output disable time after $\overline{\text{W}}$ high (see Note 6)	3	15	3	18	3	20	ns

NOTE 6: Maximum t<sub>REZ</sub>, t<sub>CEZ</sub>, t<sub>WEZ</sub> and t<sub>OEZ</sub> are specified when the output is no longer driven.

**EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature**

	'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>HPC</sub> Cycle time, EDO page-mode read or write	25		30		35		ns
t <sub>CSH</sub> Hold time, $\overline{\text{CAS}}$ from $\overline{\text{RAS}}$	50		55		60		ns
t <sub>CHO</sub> Hold time, $\overline{\text{OE}}$ from $\overline{\text{CAS}}$	10		10		10		ns
t <sub>DOH</sub> Hold time, output from $\overline{\text{CAS}}$	3		3		3		ns
t <sub>CAS</sub> Pulse duration, $\overline{\text{CAS}}$	10	10000	12	10000	15	10000	ns
t <sub>WPE</sub> Pulse duration, $\overline{\text{W}}$ (output disable only)	5		5		5		ns
t <sub>OCH</sub> Setup time, $\overline{\text{OE}}$ before $\overline{\text{CAS}}$	10		10		10		ns
t <sub>CP</sub> Precharge time, $\overline{\text{CAS}}$	5		5		5		ns
t <sub>OEP</sub> Precharge time, $\overline{\text{OE}}$	5		5		5		ns

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

**ADVANCE INFORMATION**

	'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub> Cycle time, random read or write (see Note 7)	110		130		150		ns
t <sub>RWC</sub> Cycle time, read-write (see Note 7)	150		175		200		ns
t <sub>PRWC</sub> Cycle time, EDO page-mode read-write	80		90		100		ns
t <sub>RASP</sub> Pulse duration, page mode, $\overline{\text{RAS}}$ low, (see Note 8)	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub> Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low, (see Note 8)	60	10 000	70	10 000	80	10 000	ns
t <sub>RP</sub> Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>WP</sub> Pulse duration, $\overline{\text{W}}$	10		10		10		ns
t <sub>ASC</sub> Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub> Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub> Setup time, data before $\overline{\text{W}}$ low (see Note 9)	0		0		0		ns
t <sub>RCS</sub> Setup time, read before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	10		12		15		ns
t <sub>RWL</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	10		12		15		ns
t <sub>WCS</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low (early-write operation only)	0		0		0		ns
t <sub>WSR</sub> Setup time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>CAH</sub> Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DH</sub> Hold time, data after $\overline{\text{CAS}}$ low (see Note 9)	10		15		15		ns
t <sub>RAH</sub> Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub> Hold time, read after $\overline{\text{CAS}}$ high (see Note 10)	0		0		0		ns
t <sub>RRH</sub> Hold time, read after $\overline{\text{RAS}}$ high (see Note 10)	0		0		0		ns
t <sub>WCH</sub> Hold time, write after $\overline{\text{CAS}}$ low (early-write operation only)	10		15		15		ns
t <sub>WHR</sub> Hold time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>ROH</sub> Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$	10		10		10		ns
t <sub>AWD</sub> Delay time, column address to $\overline{\text{W}}$ low (read-write operation only)	55		63		70		ns
t <sub>CHR</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	15		15		20		ns
t <sub>CRP</sub> Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>CSR</sub> Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t <sub>CWD</sub> Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (read-write operation only)	40		46		50		ns
t <sub>OEH</sub> Hold time, $\overline{\text{OE}}$ command	15		18		20		ns
t <sub>OED</sub> Delay time, valid data in after $\overline{\text{OE}}$ high	15		18		20		ns
t <sub>RAD</sub> Delay time, $\overline{\text{RAS}}$ low to column address	15	30	15	35	15	40	ns
t <sub>RAL</sub> Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t <sub>CAL</sub> Delay time, column address to $\overline{\text{CAS}}$ high	20		25		30		ns
t <sub>RCD</sub> Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 11)	20	45	20	52	20	60	ns
t <sub>RPC</sub> Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR refresh only)	0		0		0		ns

- NOTES: 7. All timing requirements assume  $t_T = 5$  ns.  
8. In a read-write cycle, t<sub>RWD</sub> and t<sub>RWL</sub> must be observed.  
9. Referenced to the later of CAS or W in write operations  
10. The minimum value is measured when t<sub>RCD</sub> is set to t<sub>RCD</sub> min as a reference.  
11. The minimum value is specified only to assure access time.

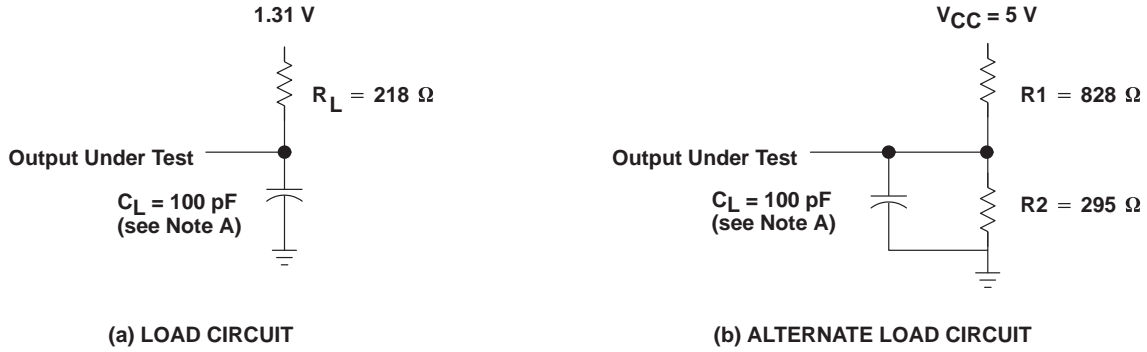


timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'44409-60 '44409P-60		'44409-70 '44409P-70		'44409-80 '44409P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RS</sub> H	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	10		12		15		ns
t <sub>R</sub> W	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low	85		98		110		ns
t <sub>REF</sub>	Refresh time interval	'44409		16		16		ms
		'44409P		128		128		ms
t <sub>T</sub>	Transition time	2	50	2	50	2	50	ms
t <sub>W</sub> H	Hold time, write low (test mode)	10		10		10		ns
t <sub>CH</sub> S	Hold time, $\overline{\text{CAS}}$ low after $\overline{\text{RAS}}$ high (self refresh) (TMS44409P only)	-50		-50		-50		ns
t <sub>W</sub> T	Setup time, write low (test mode)	10		10		10		ns
t <sub>C</sub> P	$\overline{\text{CAS}}$ precharge before self refresh	0		0		0		ns
t <sub>R</sub> P	$\overline{\text{RAS}}$ precharge after self refresh	110		130		150		ns
t <sub>R</sub> SS	Self-refresh entry from $\overline{\text{RAS}}$ low (TMS44409P only)	100		100		100		μs

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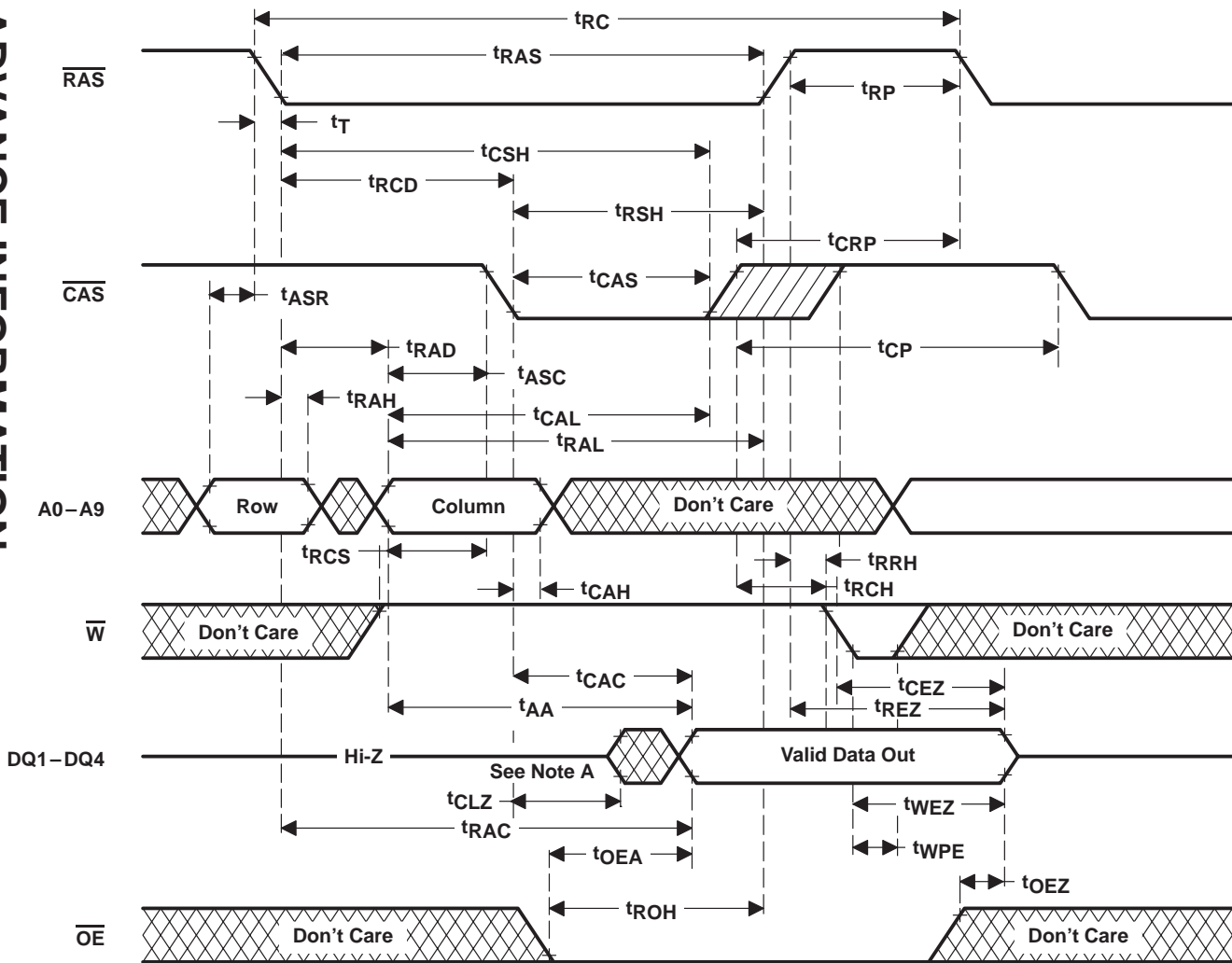
PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

ADVANCE INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

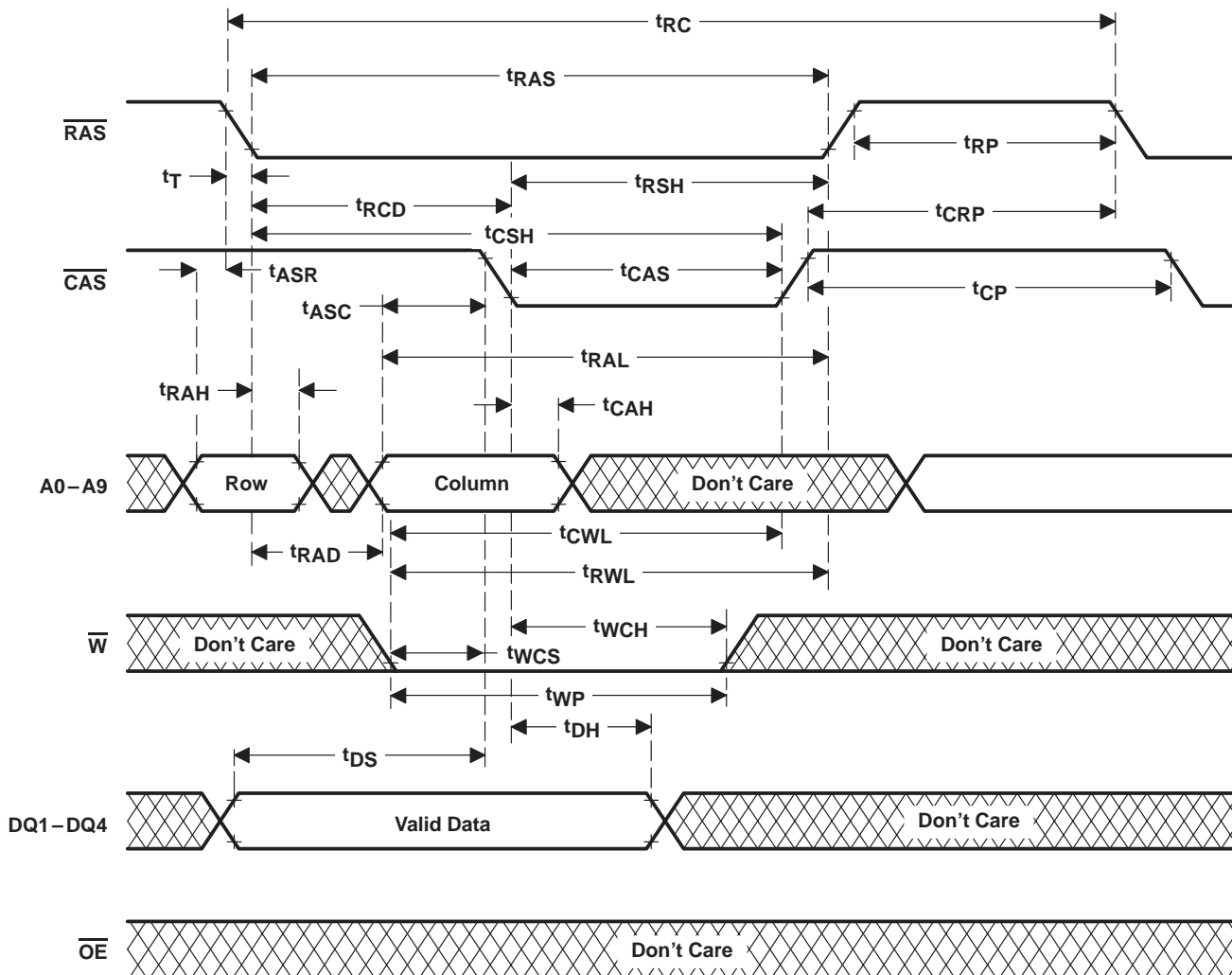


Figure 3. Early-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

ADVANCE INFORMATION

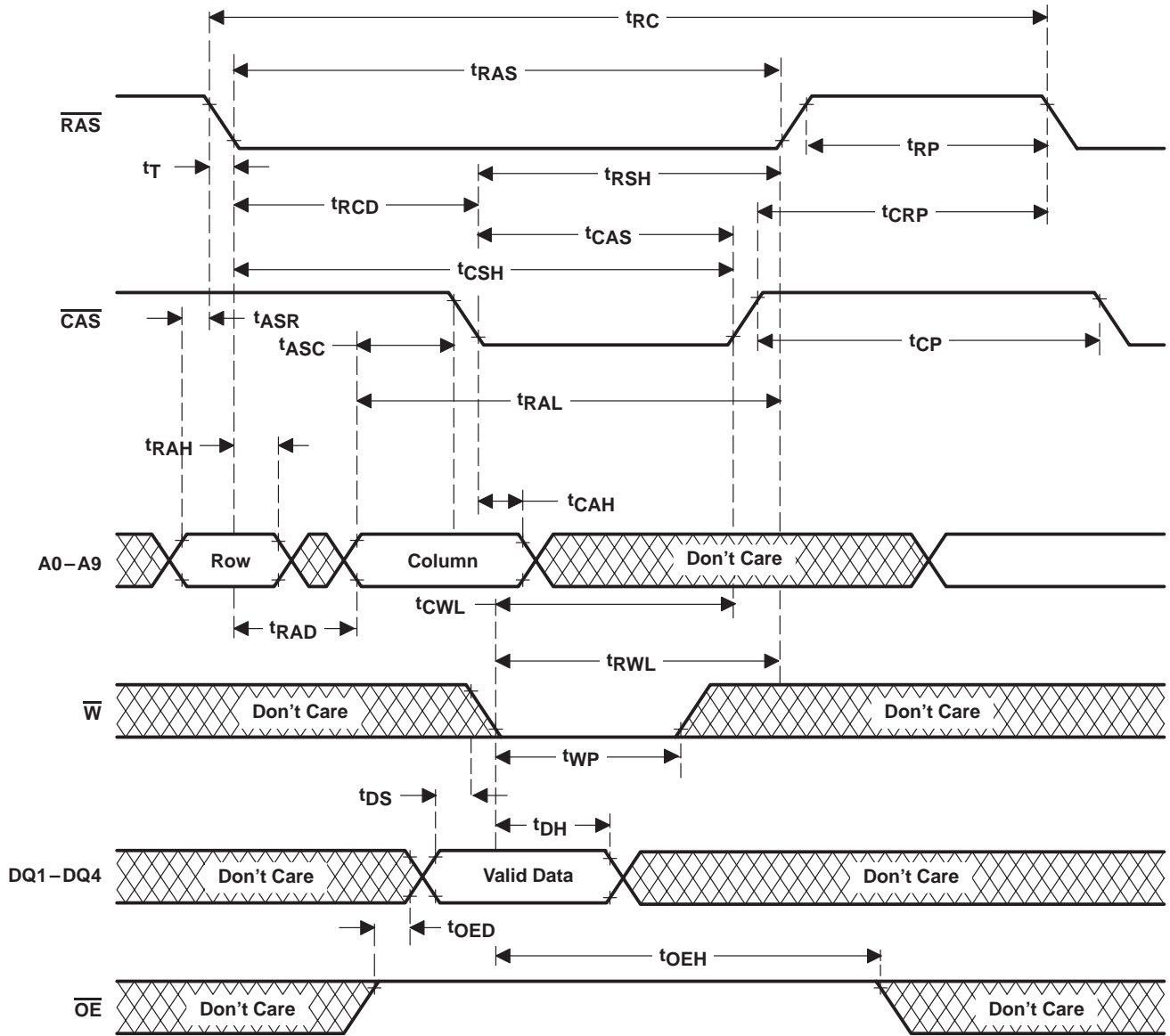
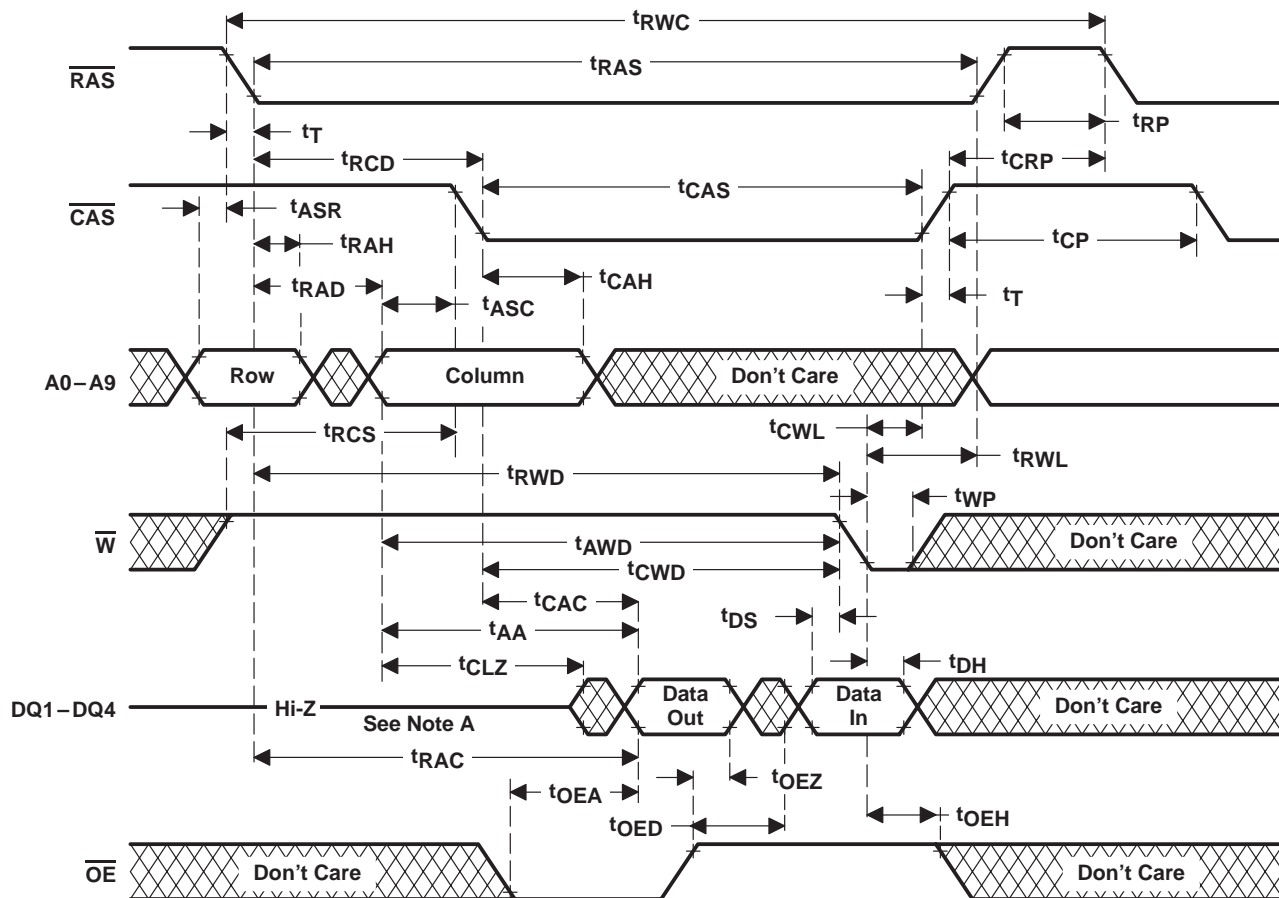


Figure 4. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



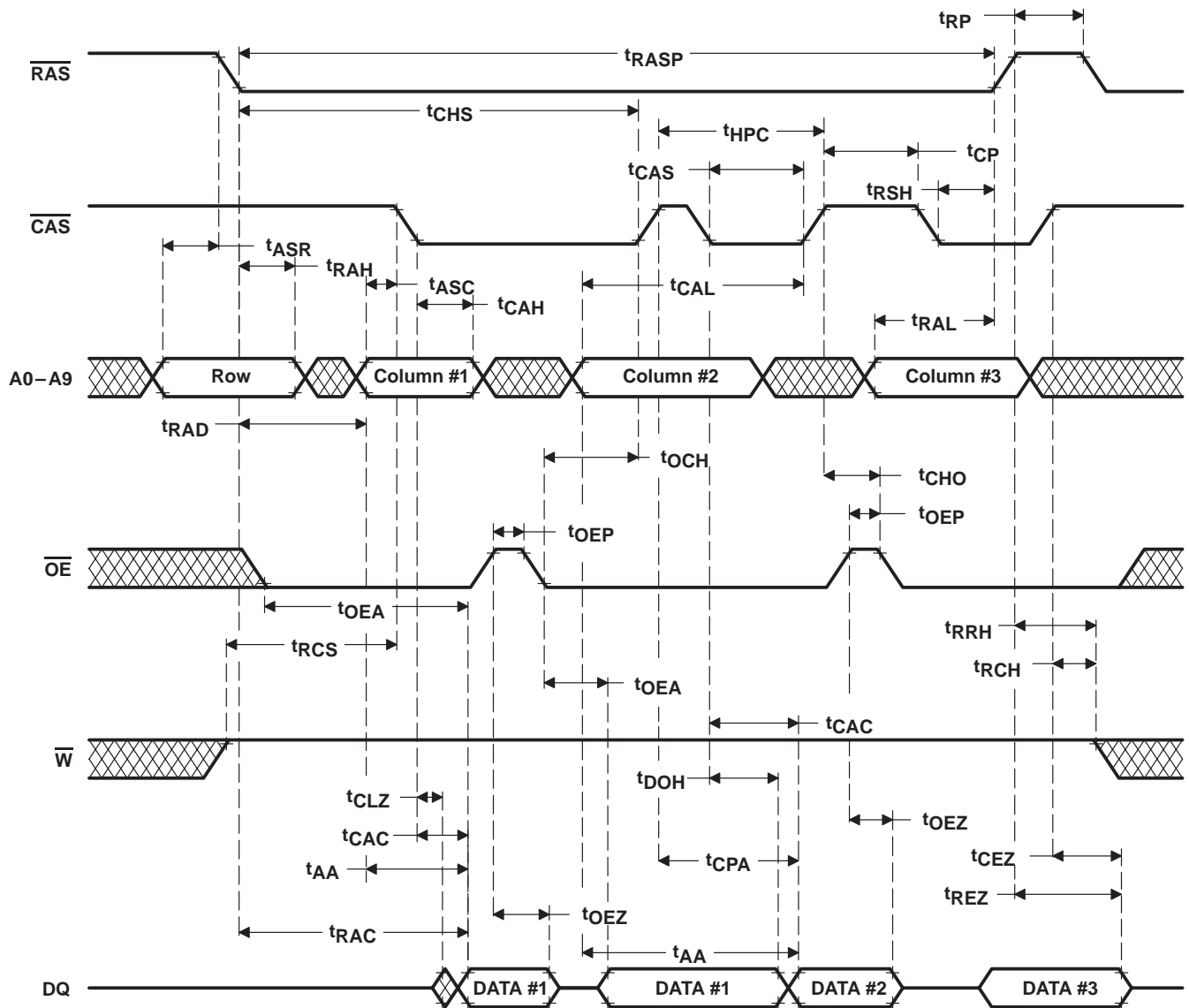
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

ADVANCE INFORMATION



PARAMETER MEASUREMENT INFORMATION



ADVANCE INFORMATION

Figure 7. Extended-Data-Out Read-Cycle With  $\overline{OE}$  Control

PARAMETER MEASUREMENT INFORMATION

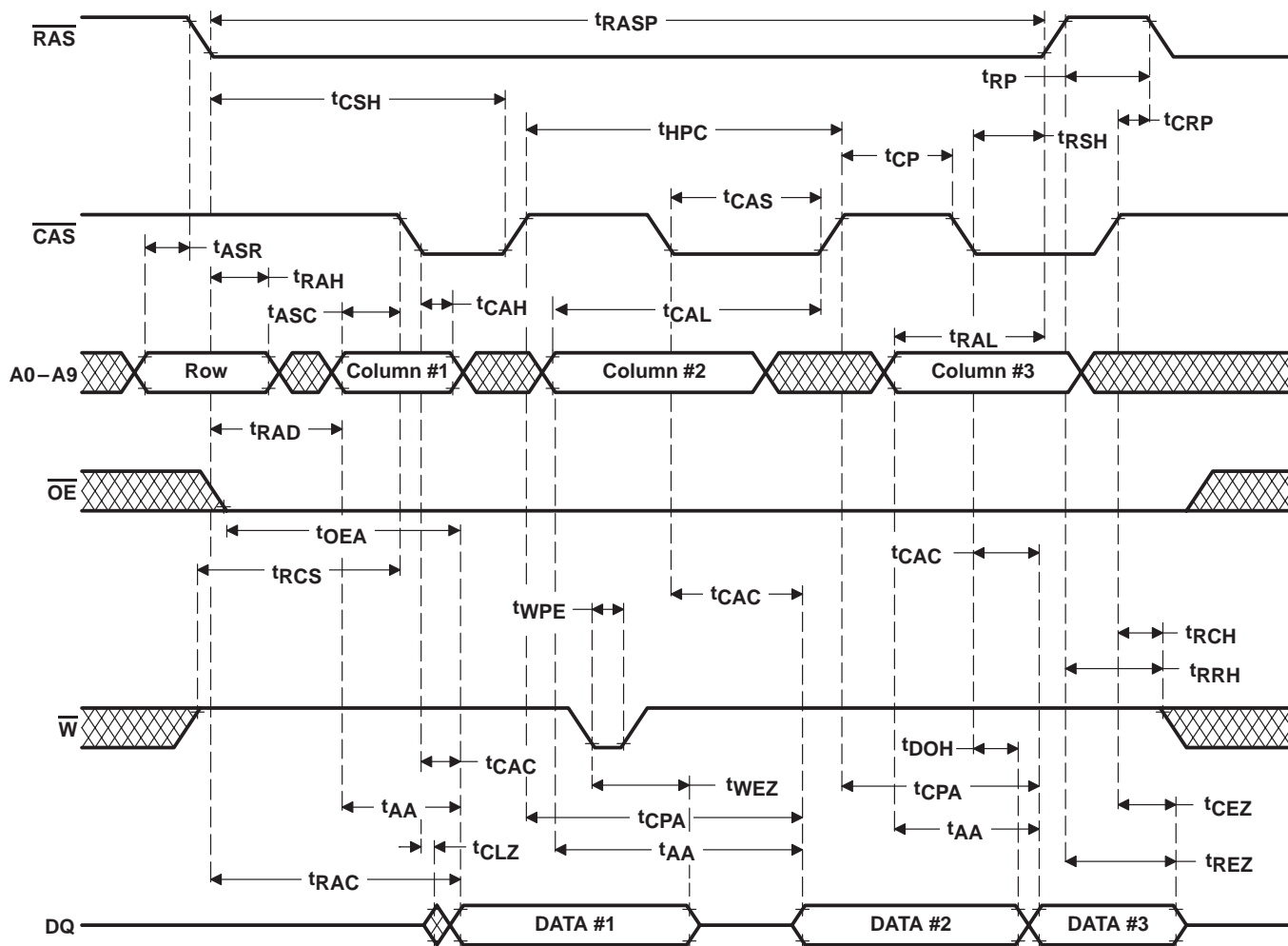
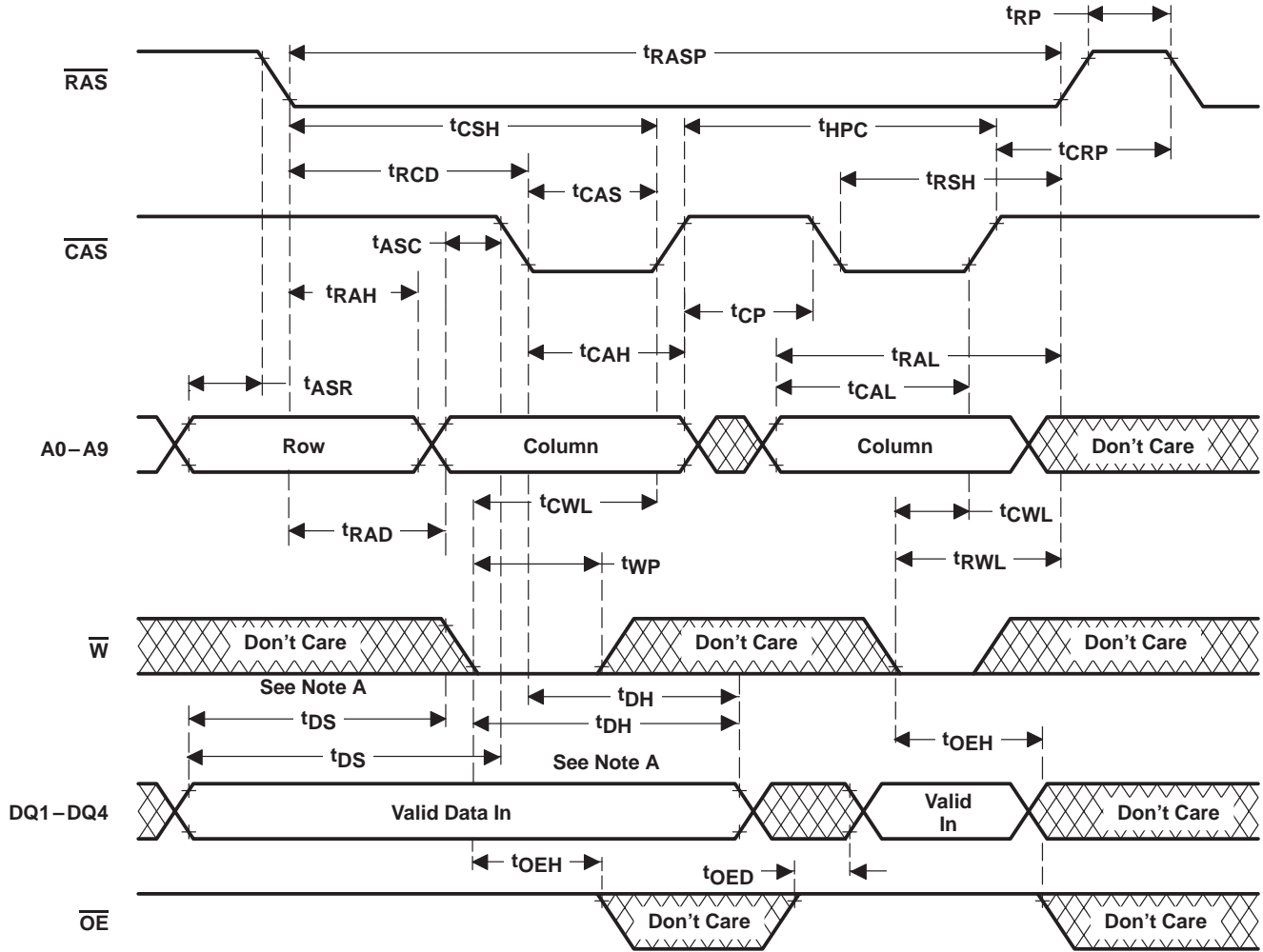


Figure 8. Extended-Data-Out Read-Cycle With  $\bar{W}$  Control

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



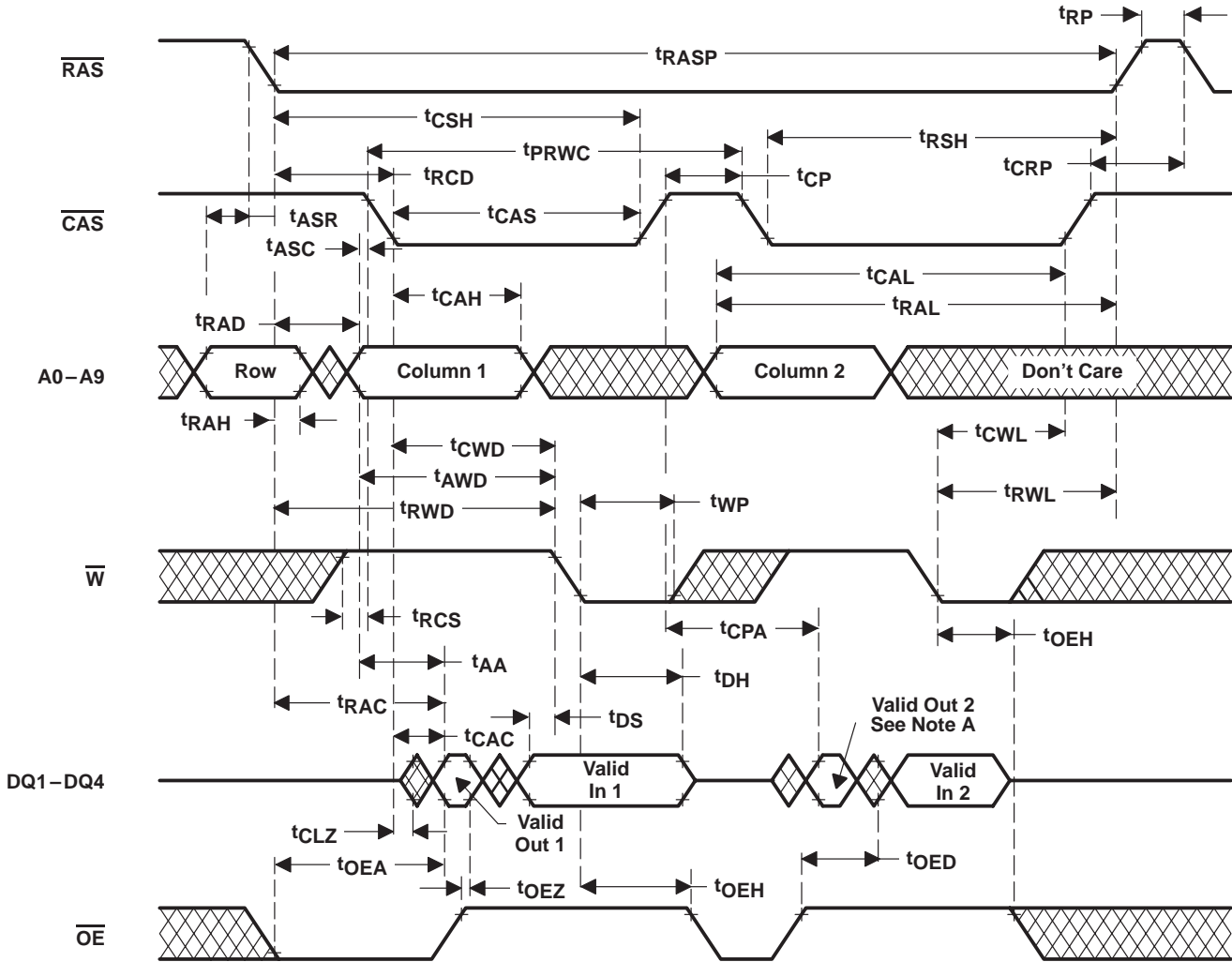
- NOTES: A. Referenced to  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$ , whichever occurs last.  
 B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. EDO-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

ADVANCE INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.  
 B. A read or write cycle can be intermixed with read-write cycles as long as the read- and write-timing specifications are not violated.

Figure 10. EDO Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

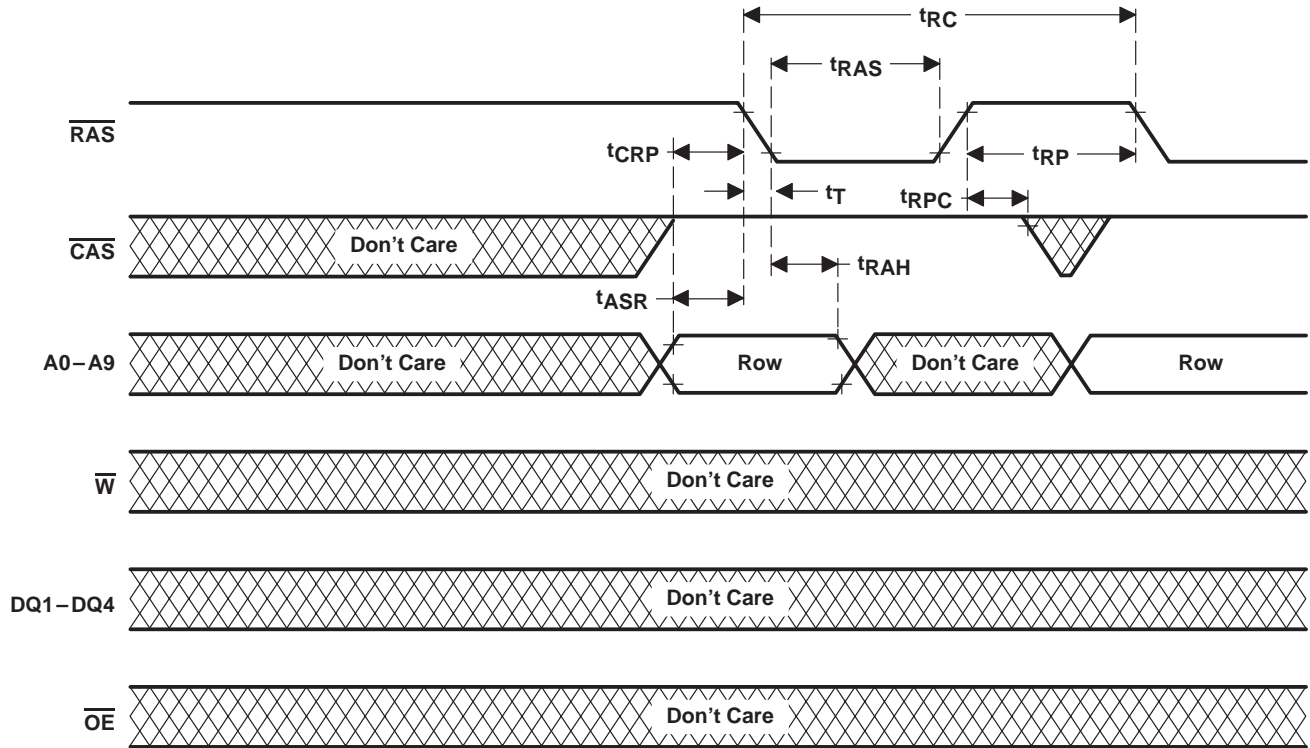


Figure 11.  $\overline{\text{RAS}}$ -Only Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

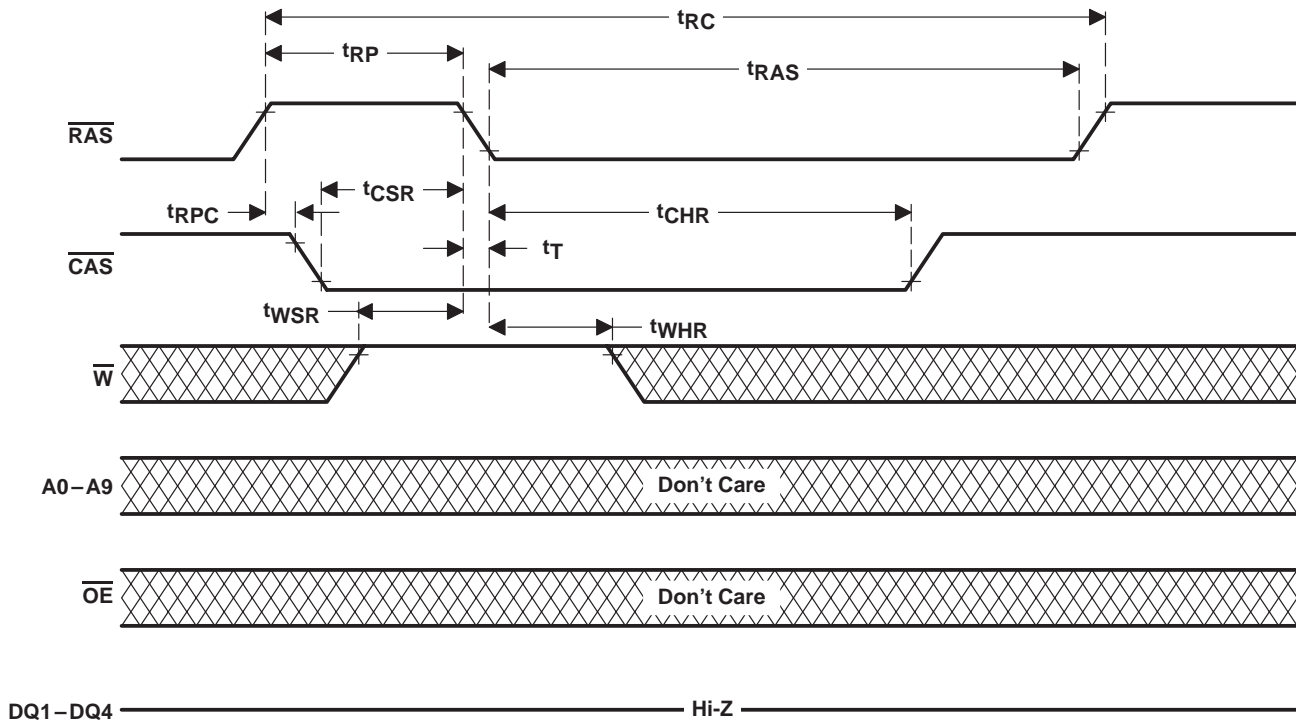


Figure 12. Automatic-CBR-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

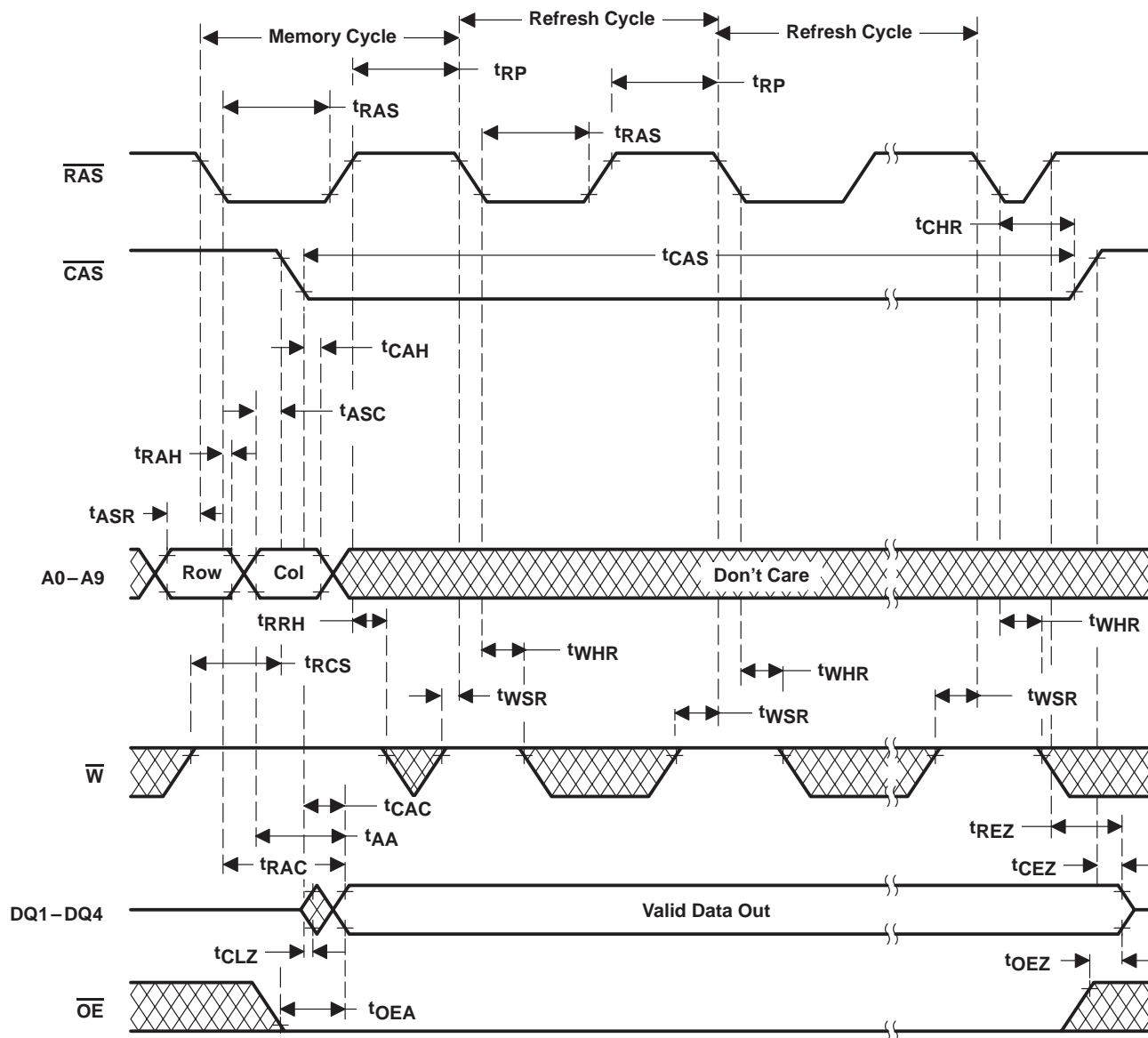


Figure 13. Hidden-Refresh Cycle (Read)

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PARAMETER MEASUREMENT INFORMATION

ADVANCE INFORMATION

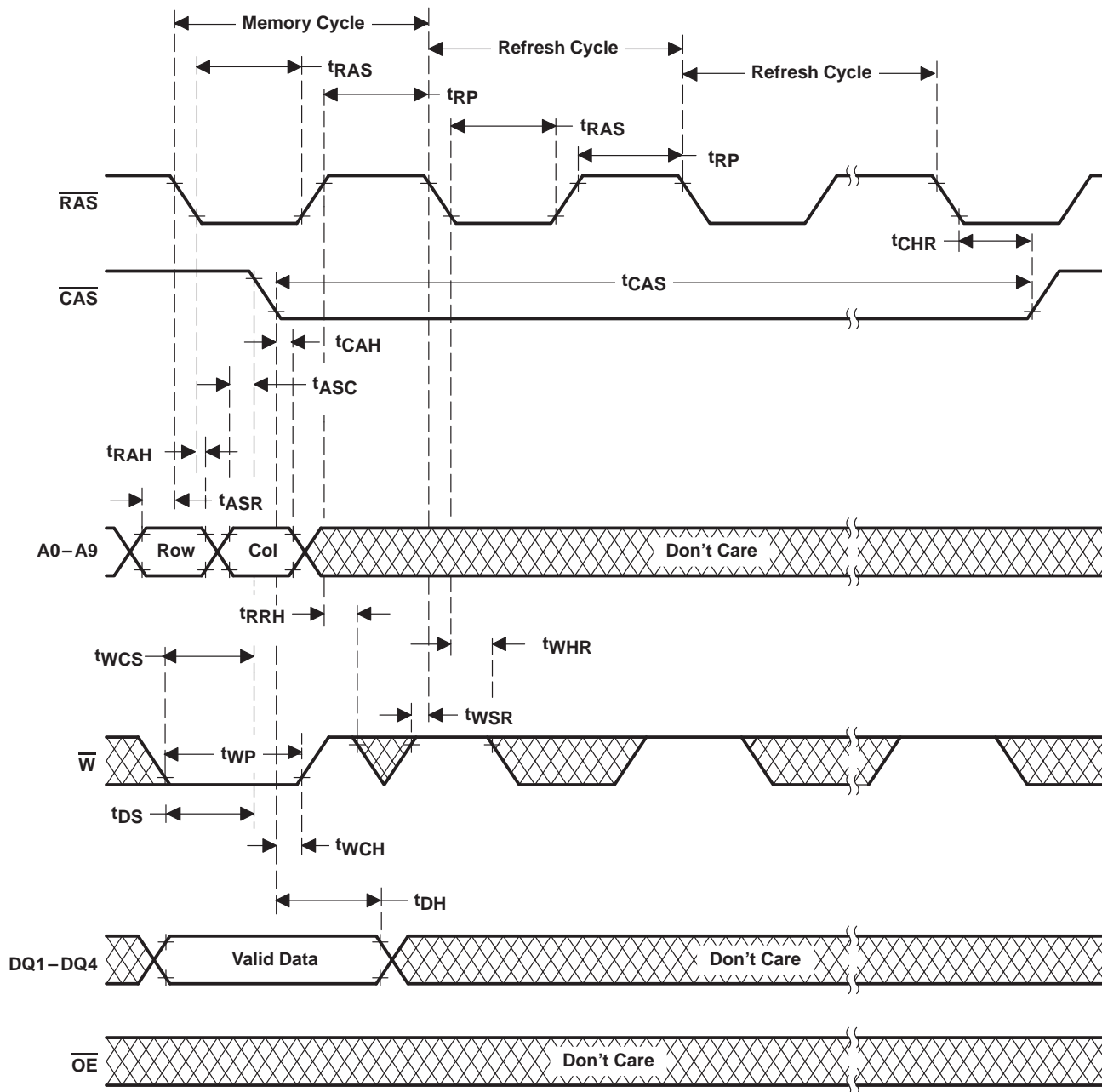


Figure 14. Hidden-Refresh Cycle (Write)

PARAMETER MEASUREMENT INFORMATION

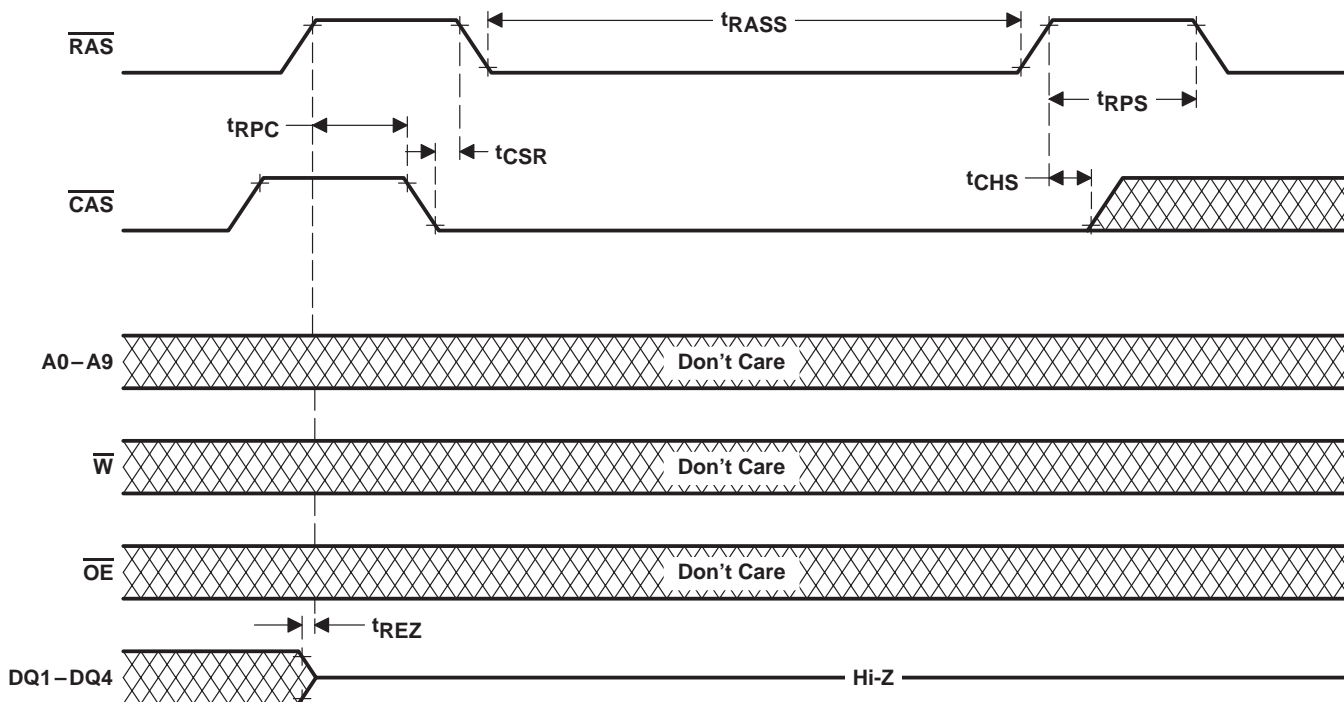


Figure 15. Self Refresh Timing

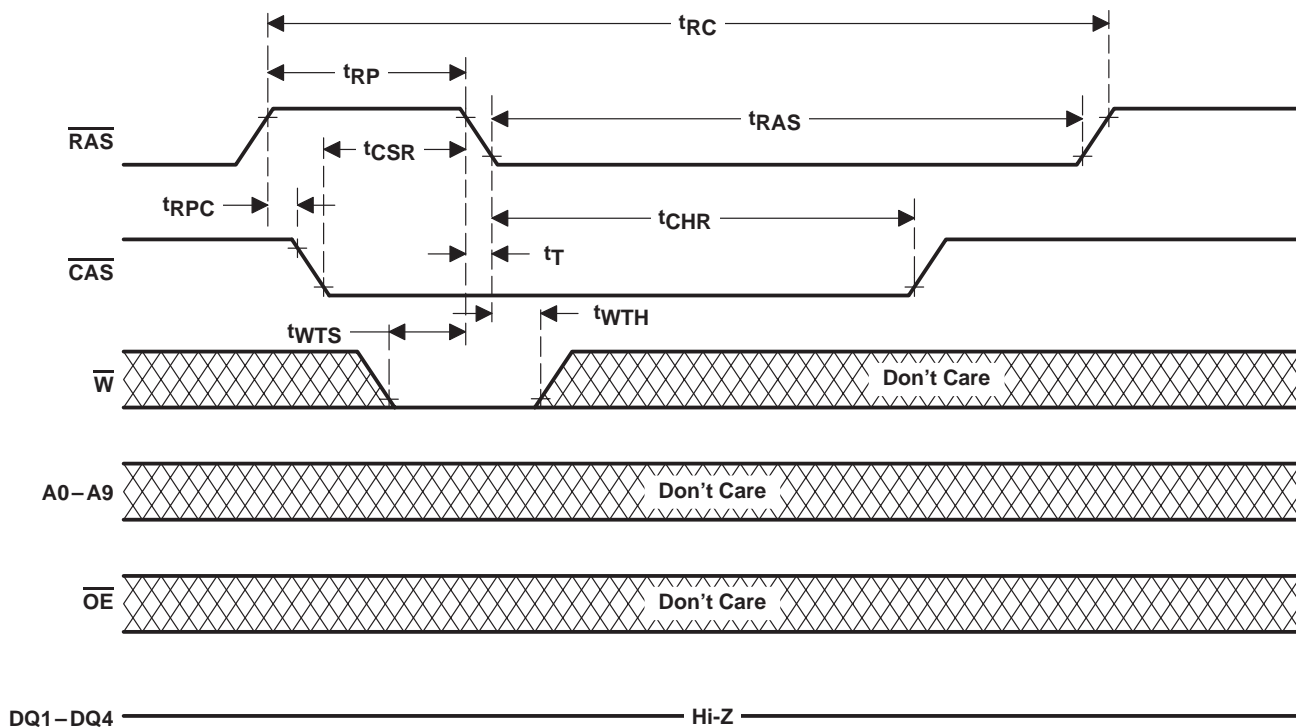


Figure 16. Test-Mode Entry Cycle

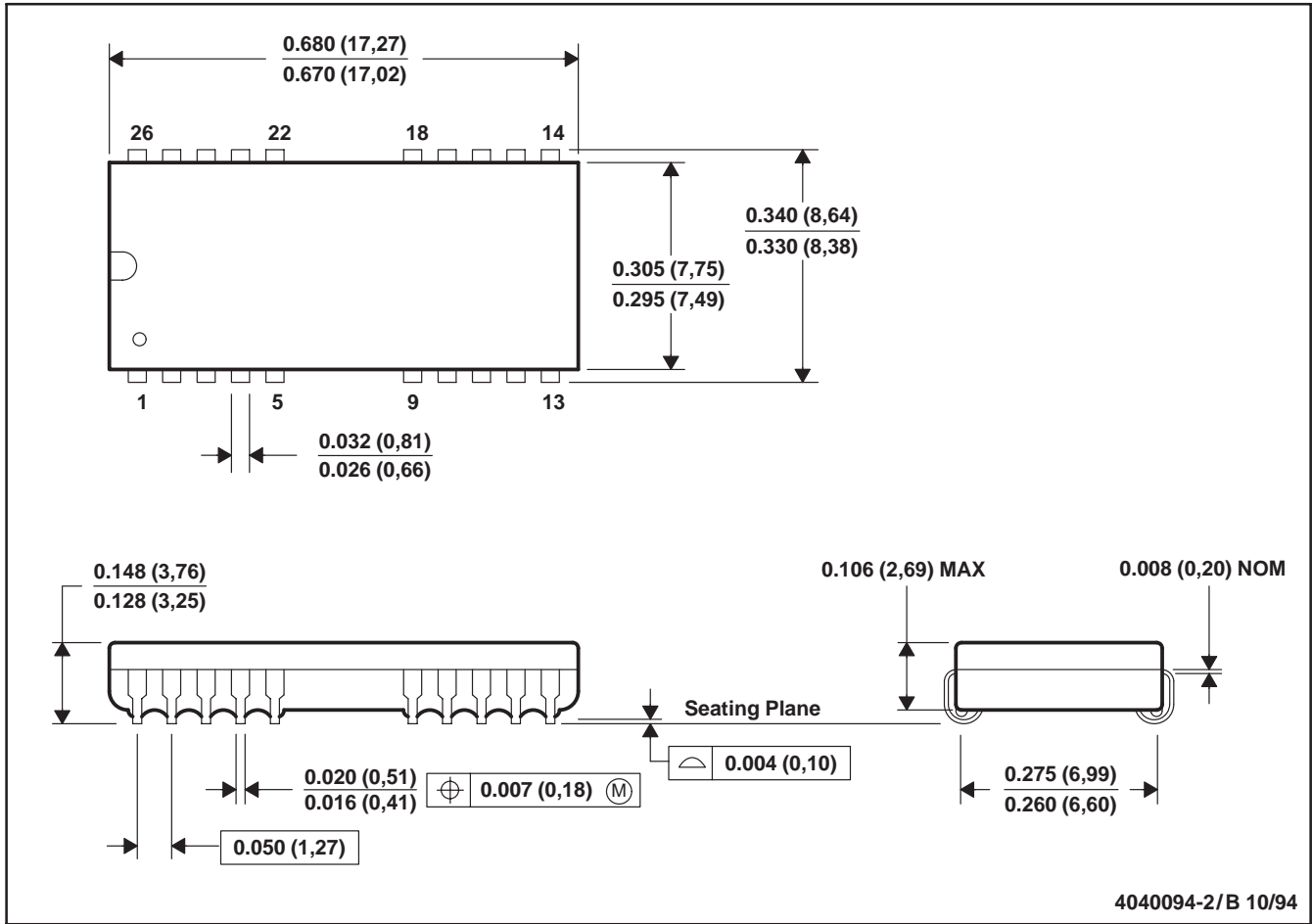
ADVANCE INFORMATION

MECHANICAL DATA

DJ (R-PDSO-J20/26)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE

ADVANCE INFORMATION



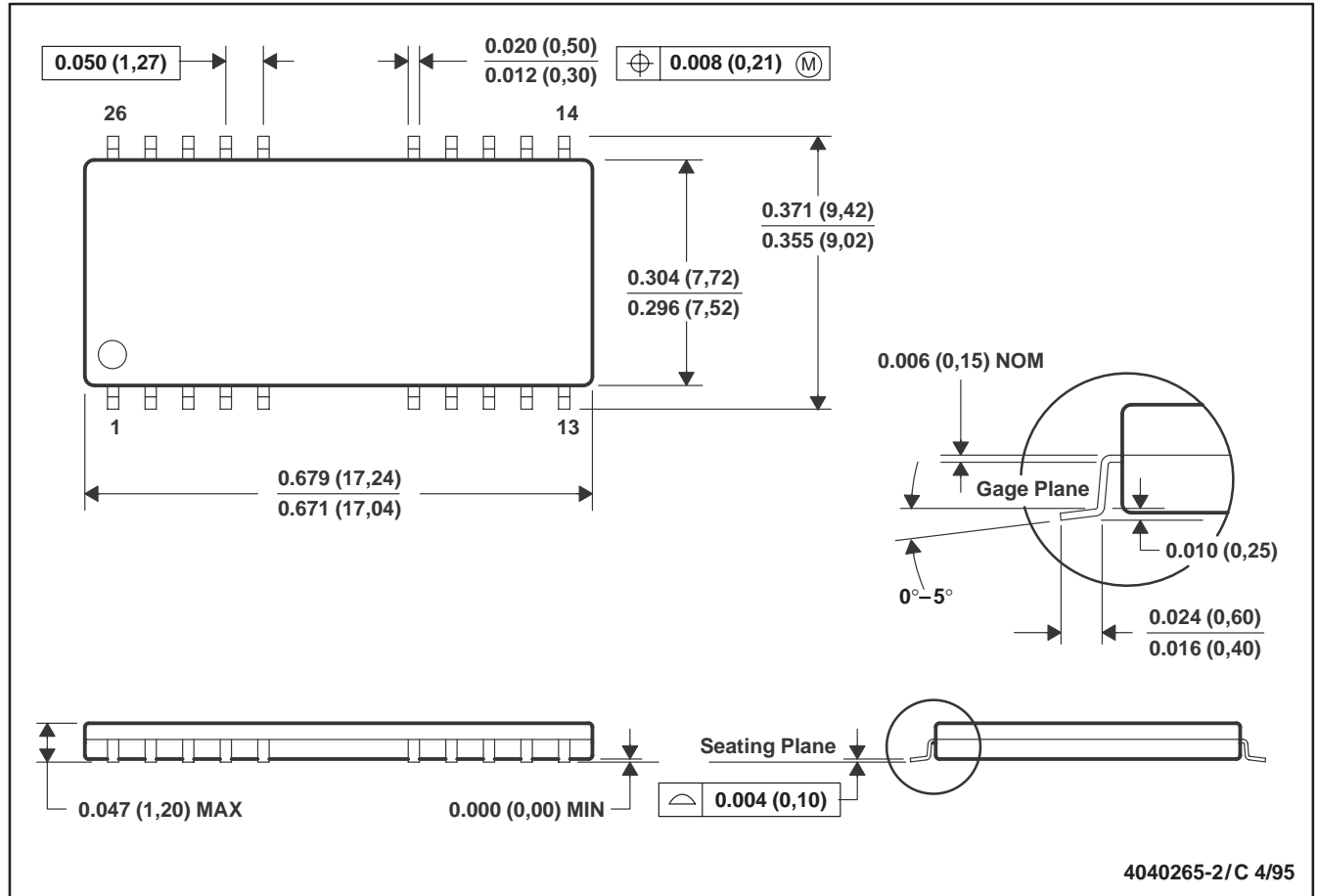
4040094-2/B 10/94

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

MECHANICAL DATA

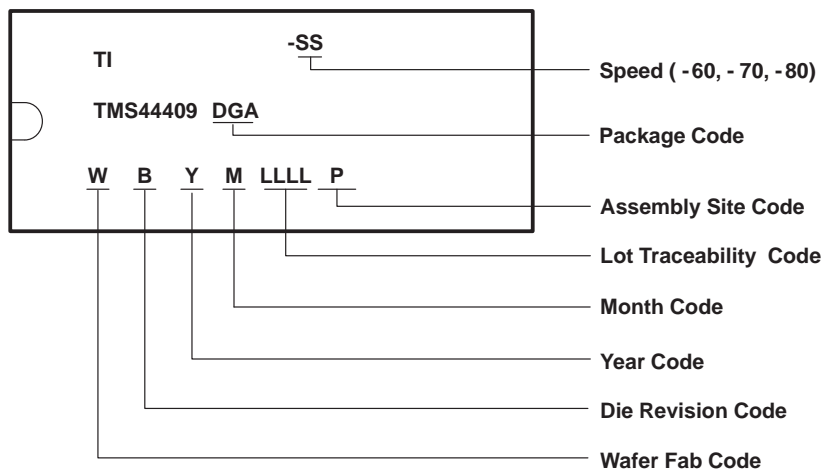
DGA (R-PDSO-G20/26)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.

device symbolization (TMS44409 illustrated)



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