

T-46-23-15

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information
4M x 1 CMOS Dynamic RAM
Fast Page Mode

3

The MCM54100A is a 0.7 μ CMOS high-speed dynamic random access memory. It is organized as 4,194,304 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

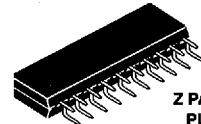
The MCM54100A requires only 11 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil J lead small outline package, 100 mil zig-zag in-line package (ZIP), and a 300 mil thin small outline package (TSOP).

- Three-State Data Output
- Fast Page Mode
- Test Mode
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$ -Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: MCM54100A = 16 ms
- Fast Access Time (t_{RAC}):
 - MCM54100A-60 and MCM5L4100A-60 = 60 ns (Max)
 - MCM54100A-70 and MCM5L4100A-70 = 70 ns (Max)
 - MCM54100A-80 and MCM5L4100A-80 = 80 ns (Max)
- Low Active Power:
 - MCM54100A-60 and MCM5L4100A-60 = 660 mW (Max)
 - MCM54100A-80 and MCM5L4100A-80 = 550 mW (Max)
 - MCM54100A-80 and MCM5L4100A-80 = 468 mW (Max)
- Low Standby Power Dissipation:
 - MCM54100A and MCM5L400A = 11 mW (Max, TTL Levels)
 - MCM54100A = 5.5 mW (Max, CMOS Levels)
 - MCM5L4100A = 1.1 mW (Max, CMOS Levels)

MCM54100A
MCM5L4100A



N PACKAGE
300 MIL SOJ
CASE 822-03



Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836-02



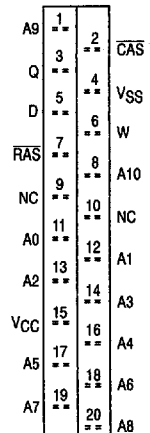
T PACKAGE
300 MIL TSOP
CASE 892-01

PIN NAMES

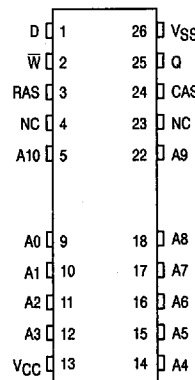
A0 - A10	Address Input
D	Data Input
Q	Data Output
W	Read/Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
VCC	Power Supply (+ 5 V)
VSS	Ground
NC	No Connection

PIN ASSIGNMENTS

100 MIL ZIP

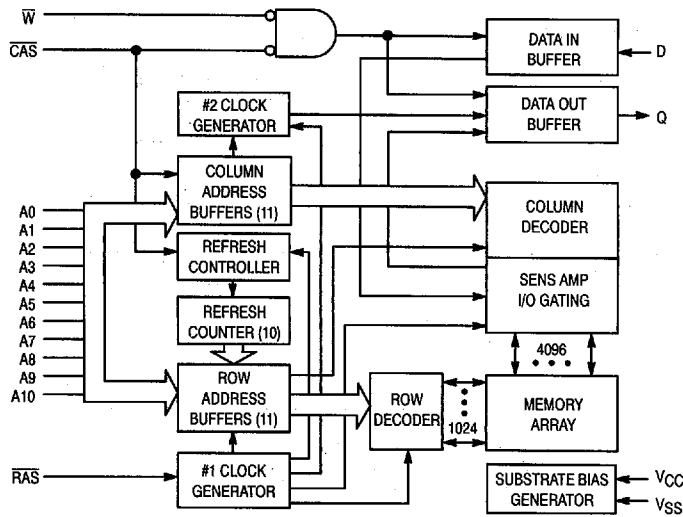


300 MIL SOJ/TSOP



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	- 1 to + 7	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	- 1 to + 7	V
Data Output Current	I _{out}	50	mA
Power Dissipation	P _D	700	mW
Operating Temperature Range	T _A	0 to + 70	°C
Storage Temperature Range	T _{stg}	- 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	
Logic High Voltage, All Inputs	V _{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V _{IL}	-1.0	—	0.8	V

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V _{CC} Power Supply Current MCM54100A-60 and MCM5L4100A-60, t _{RC} = 110 ns MCM54100A-70 and MCM5L4100A-70, t _{RC} = 130 ns MCM54100A-80 and MCM5L4100A-80, t _{RC} = 150 ns	I _{CC1}	—	120	mA	1, 2
		—	100		
		—	85		
		—	—		
V _{CC} Power Supply Current (Standby) (R _{AS} = C _{AS} = V _{IH})	I _{CC2}	—	2.0	mA	
V _{CC} Power Supply Current During R _{AS} Only Refresh Cycles (C _{AS} = V _{IH}) MCM54100A-60 and MCM5L4100A-60, t _{RC} = 110 ns MCM54100A-70 and MCM5L4100A-70, t _{RC} = 130 ns MCM54100A-80 and MCM5L4100A-80, t _{RC} = 150 ns	I _{CC3}	—	120	mA	1, 2
		—	100		
		—	85		
		—	—		
V _{CC} Power Supply Current During Fast Page Mode Cycle (R _{AS} = V _{IL}) MCM54100A-60 and MCM5L4100A-60, t _{PC} = 45 ns MCM54100A-70 and MCM5L4100A-70, t _{PC} = 45 ns MCM54100A-80 and MCM5L4100A-80, t _{PC} = 50 ns	I _{CC4}	—	60	mA	1, 2
		—	70		
		—	60		
		—	—		
V _{CC} Power Supply Current (Standby) (R _{AS} = C _{AS} = V _{IH} - 0.2 V) MCM54100A MCM5L4100A	I _{CC5}	—	1.0	mA	
		—	200		
V _{CC} Power Supply Current During C _{AS} Before R _{AS} Refresh Cycle MCM54100A-60 and MCM5L4100A-60, t _{RC} = 110 ns MCM54100A-70 and MCM5L4100A-70, t _{RC} = 130 ns MCM54100A-80 and MCM5L4100A-80, t _{RC} = 150 ns	I _{CC6}	—	120	mA	1
		—	100		
		—	85		
		—	—		
V _{CC} Power Supply Current, Battery Backup Mode — MCM5L4100A Only (t _{RC} = 125 μs; C _{AS} = C _{AS} Before R _{AS} Cycling or 0.2 V; W = V _{CC} - 0.2 V; D _{in} = V _{CC} - 0.2 V or 0.2 V or OPEN; A0 - A10 = V _{CC} - 0.2 V or 0.2 V) t _{RAS} = 300 ns to 1 μs t _{RAS} = Min to 300 ns	I _{CC7}	—	400	μA	1, 3
		—	300		
		—	—		
Input Leakage Current (0 V ≤ V _{in} ≤ 6.5 V)	I _{kg(I)}	-10	10	μA	
Output Leakage Current (C _{AS} = V _{IH} , 0 V ≤ V _{out} ≤ 5.5 V)	I _{kg(O)}	-10	10	μA	
Output High Voltage (I _{OH} = - 5 mA)	V _{OH}	2.4	—	V	
Output Low Voltage (I _{OL} = 4.2 mA)	V _{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Column address can be changed once or less while R_{AS} = V_{IL} and C_{AS} = V_{IH}.
3. t_{RAS} (max) = 1 μs is only applied to refresh of battery-back up. t_{RAS} (max) = 10 μs is applied to functional operating

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance A0 - A10, D R _{AS} , C _{AS} , W	C _{in}	5	pF
		7	
I/O Capacitance (C _{AS} = V _{IH} to Disable Output)	Q C _{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS
 (V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	110	—	130	—	150	—	ns	5
Read-Write Cycle Time	t _{RELREL}	t _{RWC}	140	—	155	—	175	—	ns	5
Fast Page Mode Cycle Time	t _{CELCEL}	t _{PC}	45	—	45	—	50	—	ns	
Fast Page Mode Read-Write Cycle Time	t _{CELCEL}	t _{PRWC}	65	—	70	—	75	—	ns	
Access Time from RAS	t _{RELQV}	t _{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from CAS	t _{CELQV}	t _{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t _{AVQV}	t _{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge CAS	t _{CEHQV}	t _{CPA}	—	40	—	40	—	45	ns	6
CAS to Output in Low-Z	t _{CELQX}	t _{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t _{CEHQZ}	t _{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t _T	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{REHREL}	t _{RP}	45	—	50	—	60	—	ns	
RAS Pulse Width	t _{RELREH}	t _{RAS}	60	10 k	70	10 k	80	10 k	ns	
RAS Pulse Width (Fast Page Mode)	t _{RELREH}	t _{RASP}	60	200 k	70	200 k	80	200 k	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	20	—	20	—	20	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	60	—	70	—	80	—	ns	
CAS Precharge to RAS Hold Time	t _{CEHREH}	t _{RHCP}	40	—	40	—	45	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	20	10 k	20	10 k	20	10 k	ns	
RAS to CAS Delay Time	t _{RELCEL}	t _{RCD}	20	40	20	50	20	60	ns	11
RAS to Column Address Delay Time	t _{RELAV}	t _{RAD}	15	30	15	35	15	40	ns	12
CAS to RAS Precharge Time	t _{CEHREL}	t _{CRP}	5	—	5	—	5	—	ns	
CAS Precharge Time	t _{CEHCEL}	t _{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t _{AVREL}	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RELAX}	t _{RAH}	10	—	10	—	10	—	ns	

3

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (-200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that t_{RCD} ≤ t_{RCD} (max).
8. Assumes that t_{RCD} ≥ t_{RCD} (max).
9. Assumes that t_{RAD} ≥ t_{RAD} (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

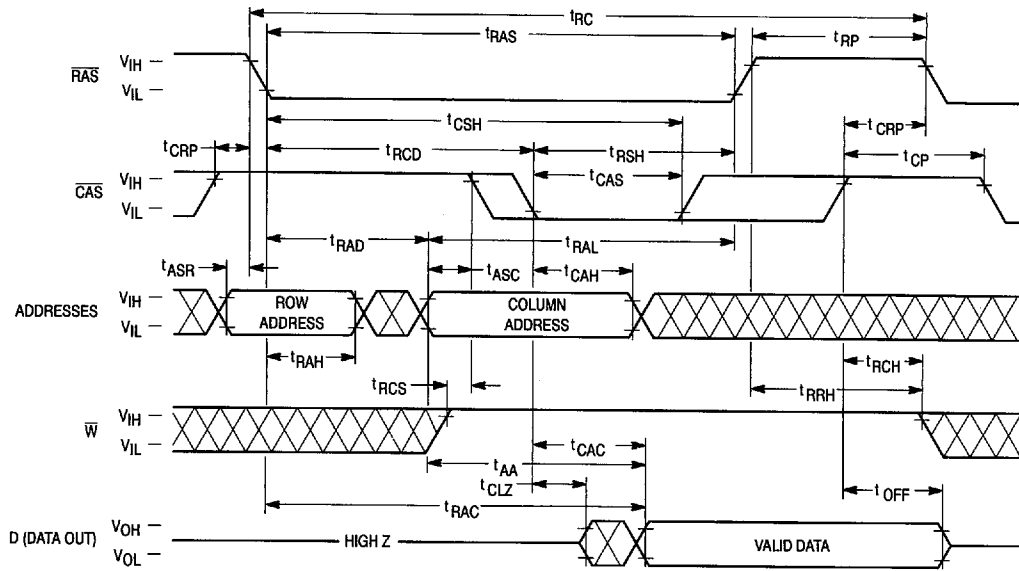
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes	
	Std	Alt	Min	Max	Min	Max	Min	Max			
Column Address Setup Time	tAVCEL	tASC	0	—	0	—	0	—	ns		
Column Address Hold Time	tCELAX	tCAH	15	—	15	—	15	—	ns		
Column Address to RAS Lead Time	tAVREH	tRAL	30	—	35	—	40	—	ns		
Read Command Setup Time	tWHCEL	tRCS	0	—	0	—	0	—	ns		
Read Command Hold Time Referenced to CAS	tCEHWX	tRCH	0	—	0	—	0	—	ns	13	
Read Command Hold Time Referenced to RAS	tREHWX	tRRH	0	—	0	—	0	—	ns	13	
Write Command Hold Time Referenced to CAS	tCELWH	tWCH	10	—	15	—	15	—	ns		
Write Command Pulse Width	tWLWH	tWP	10	—	15	—	15	—	ns		
Write Command to RAS Lead Time	tWLREH	tRWL	20	—	20	—	20	—	ns		
Write Command to CAS Lead Time	tWLCEH	tCWL	20	—	20	—	20	—	ns		
Data in Setup Time	tDVCEL	tDS	0	—	0	—	0	—	ns	14	
Data in Hold Time	tCELDX	tDH	15	—	15	—	15	—	ns	14	
Refresh Period	MCM54100A MCM5L4100A	tRVRV	tRFSH	—	16 128	—	16 128	—	16 128	ms	
Write Command Setup Time	tWLCEL	tWCS	0	—	0	—	0	—	ns	15	
CAS to Write Delay	tCELWL	tCWD	20	—	20	—	20	—	ns	15	
RAS to Write Delay	tRELWL	tRWD	60	—	70	—	80	—	ns	15	
Column Address to Write Delay Time	tAVWL	tAWD	30	—	35	—	40	—	ns	15	
CAS Precharge to Write Delay Time (Page Mode)	tCEHWL	tCPWD	40	—	40	—	40	—	ns	15	
CAS Setup Time for CAS Before RAS Refresh	tRELCEL	tCSR	5	—	5	—	5	—	ns		
CAS Hold Time for CAS Before RAS Refresh	tRELCEH	tCHR	15	—	15	—	15	—	ns		
RAS Precharge to CAS Active Time	tREHCEL	tRPC	0	—	0	—	0	—	ns		
CAS Precharge Time for CAS Before RAS Counter Time	tCEHCEL	tCPT	30	—	40	—	40	—	ns		
Write Command Setup Time (Test Mode)	tWLREL	tWTS	10	—	10	—	10	—	ns		
Write Command Hold Time (Test Mode)	tRELWH	tWTH	10	—	10	—	10	—	ns		
Write to RAS Precharge Time (CAS Before RAS Refresh)	tWHREL	tWRP	10	—	10	—	10	—	ns		
Write to RAS Hold Time (CAS Before RAS Refresh)	tRELWL	tWRH	10	—	10	—	10	—	ns		

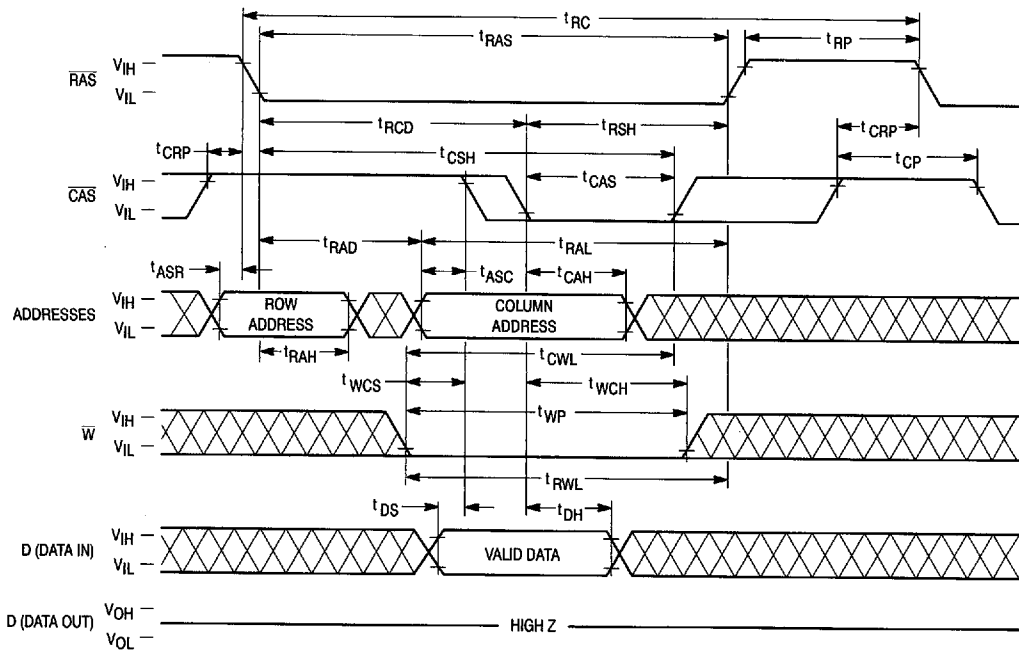
NOTES:

13. Either tRRH or tRCH must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles and to \bar{W} leading edge in read-write cycles.
15. tWCS, tRWD, tCWD, tAWD, and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if tWCS \geq tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tCWD \geq tCWD (min), tRWD \geq tRWD (min), tAWD \geq tAWD (min), and tCPWD \geq tCPWD (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



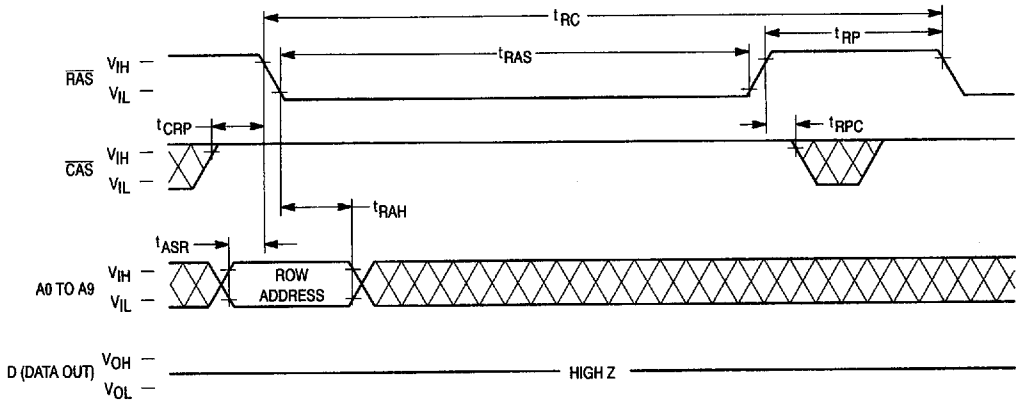
EARLY WRITE CYCLE



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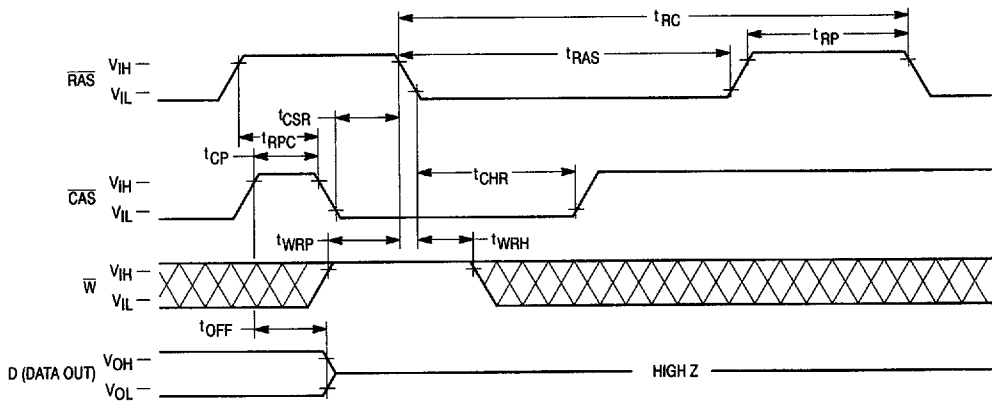
RAS ONLY REFRESH CYCLE

(\bar{W} and A10 are Don't Care)

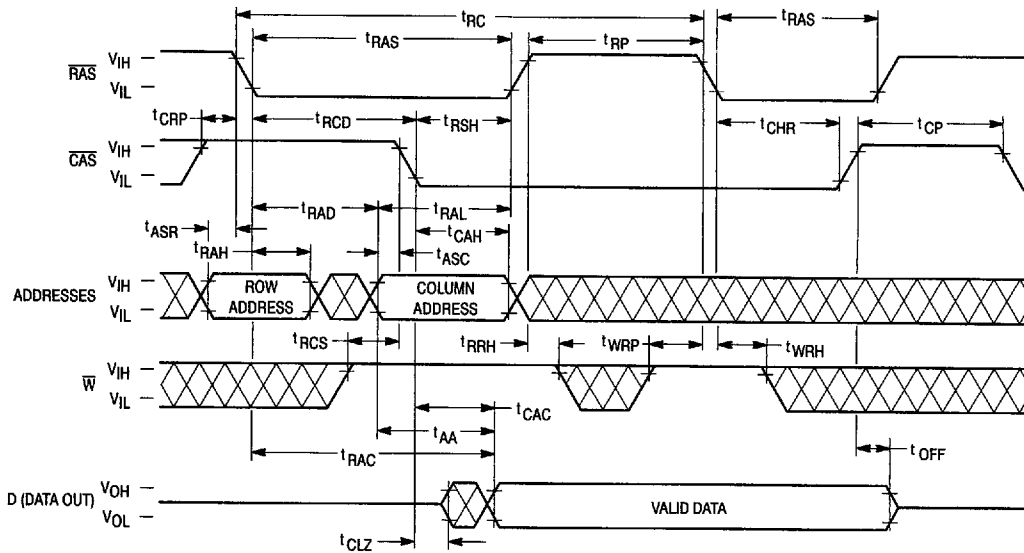


CAS BEFORE RAS REFRESH CYCLE

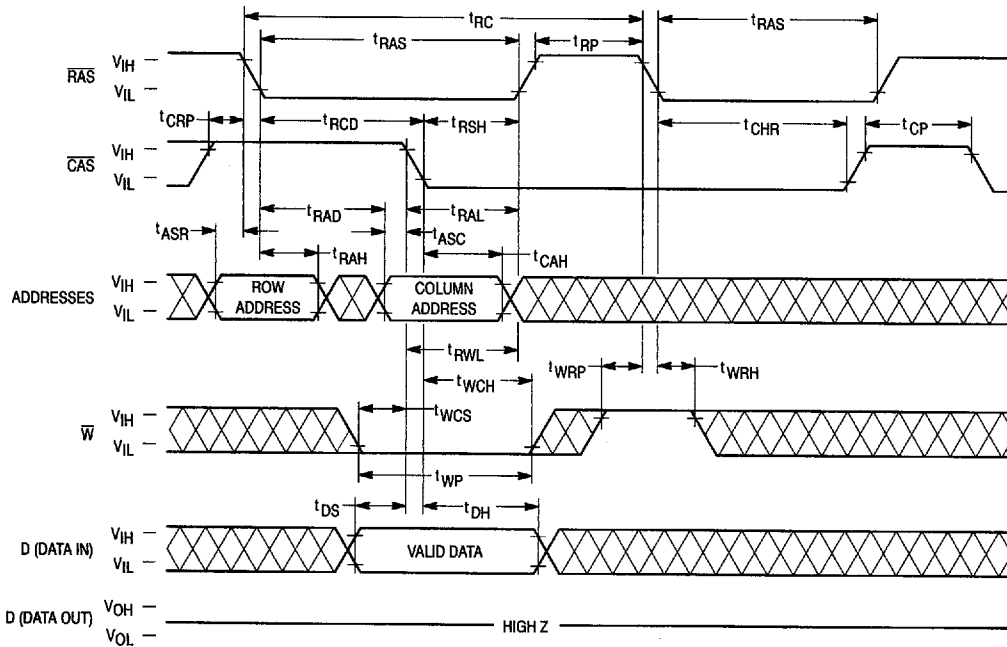
(A0 - A10 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device, with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (\overline{RAS}) and column address strobe (\overline{CAS}), into two separate 11-bit address fields. A total of twenty-two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 bit locations in the device. \overline{RAS} active transition is followed by \overline{CAS} active transition (active = V_{IL} , t_{PCD} minimum) for all read or write cycles. The delay between \overline{RAS} and \overline{CAS} active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external \overline{CAS} signal is ignored until an internal \overline{RAS} signal is available. This "gate" feature on the external \overline{CAS} clock enables the internal \overline{CAS} line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{PCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the \overline{CAS} clock.

There are three other variations in addressing the 4M RAM: **\overline{RAS} only refresh cycle, \overline{CAS} before \overline{RAS} refresh cycle, and page mode.**

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with \overline{RAS} and \overline{CAS} active transitions latching the desired bit location. The write (\overline{W}) input level must be high (V_{IH}), t_{RCS} (minimum) before the \overline{CAS} active transition, to enable read mode.

Both the \overline{RAS} and \overline{CAS} clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, \overline{CAS} must be active before or at t_{PCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from \overline{RAS} active transition). If the t_{PCD} maximum is exceeded, read access time is determined by the \overline{CAS} clock active transition (t_{CAC}).

The \overline{RAS} and \overline{CAS} clocks must remain active for a minimum time of t_{RAS} and t_{CAS} , respectively, to complete the read cycle. \overline{W} must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after \overline{RAS} or \overline{CAS} inactive transition, respectively, to maintain the data at that bit location. Once \overline{RAS} transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the \overline{CAS} clock is active.

When the \overline{CAS} clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of \overline{W} to active (V_{IL}). Early and late write modes are distinguished by the active transition of \overline{W} , with respect to \overline{CAS} . Minimum active time t_{RAS} and t_{CAS} , and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by \overline{W} active transition at minimum time t_{WJCS} before \overline{CAS} active transition. Data in (D) is referenced to \overline{CAS} in an early write cycle. \overline{RAS} and \overline{CAS} clocks must stay active for t_{RWL} and t_{CWL} , respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because \overline{W} active transition precedes or coincides with \overline{CAS} active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when \overline{W} active transition is made after \overline{CAS} active transition. \overline{W} active transition could be delayed for almost 10 microseconds after \overline{CAS} active transition, ($t_{PCD} + t_{CWD} + t_{RWL} + 2t_r$) $\leq t_{RAS}$, if other timing minimums (t_{PCD} , t_{RWL} , and t_r) are maintained. D is referenced to \overline{W} active transition in a late write cycle. Output buffers are enabled by \overline{CAS} active transition but Q may be indeterminate; see note 15 of AC Operating Conditions table. \overline{RAS} and \overline{CAS} must remain active for t_{RWL} and t_{CWL} , respectively, after \overline{W} active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except \overline{W} must remain high for t_{CWD} minimum after the \overline{CAS} active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 4M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular \overline{RAS} clock access time, t_{RAC} . Page mode operation consists of keeping \overline{RAS} active while toggling \overline{CAS} between V_{IH} and V_{IL} . The row is latched by \overline{RAS} active transition, while each \overline{CAS} active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, \overline{CAS} transitions to inactive for minimum of t_{CP} , while \overline{RAS} remains low (V_{IL}). The second \overline{CAS} active transition while \overline{RAS} is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by

t_{RASP} . Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54100A require refresh every 16 milliseconds, while refresh time for the MCM5L4100A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54100A, and 124.8 microseconds for the MCM5L4100A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54100A and 128 milliseconds on the MCM5L4100A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$ -only refresh**, **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{\text{RAS}}$ -Only Refresh

$\overline{\text{RAS}}$ -only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive

for time t_{WPP} before and time t_{WPH} after $\overline{\text{RAS}}$ active transition to prevent switching the device into **test mode**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle timing diagram**.

The test can be performed after a minimum of 8 **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

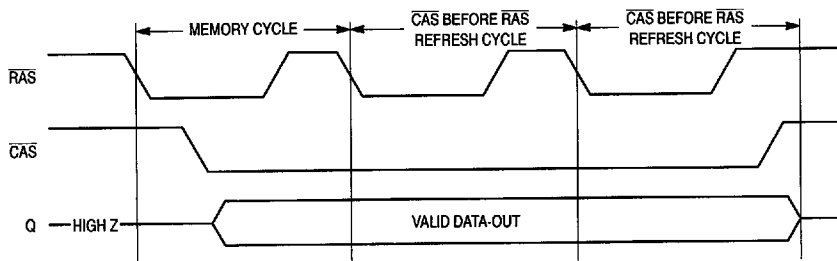


Figure 1. Hidden Refresh Cycle

TEST MODE

The internal organization of this device (512K x 8) allows it to be tested as if it were a 512K x 1 DRAM. Nineteen of the twenty-two addresses are used when operating the device in test mode. Row address A0, and column addresses A0 and A10 are ignored by the device in test mode. A test mode cycle reads and/or writes data to a bit in each of eight 512K blocks (B0 - B7) in parallel. External data out is determined by the

internal test mode logic of the device. See the following truth table and test mode block diagram.

\bar{W} , CAS before RAS timing puts the device in "Test Mode" as shown in the test mode timing diagram. A $\bar{C}AS$ before RAS or a RAS only refresh cycle puts the device back into normal mode. Refresh is performed in test mode by using a \bar{W} , CAS before RAS refresh cycle which uses internal refresh address counter.

TEST MODE TRUTH TABLE

D	B0	B1	B2	B3	B4	B5	B6	B7	Q
0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
—	Any Other								0

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TEST MODE

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

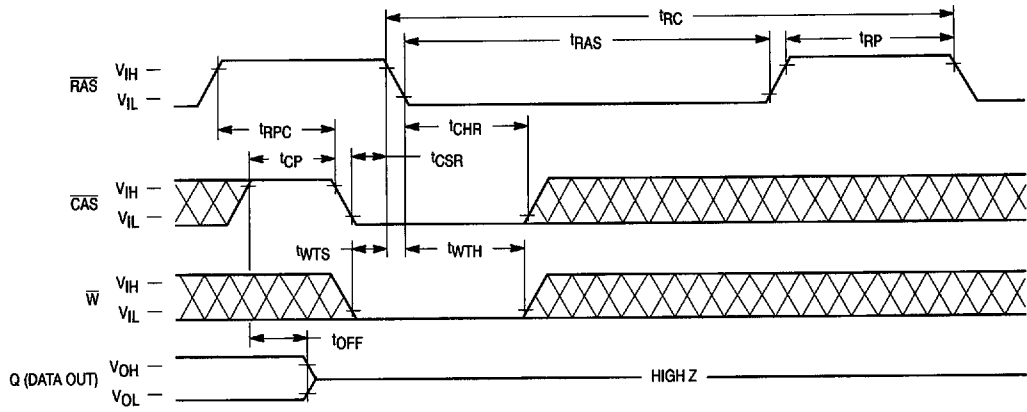
READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54100A-60 MCM5L4100A-60		MCM54100A-70 MCM5L4100A-70		MCM54100A-80 MCM5L4100A-80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	115	—	135	—	155	—	ns	5
Fast Page Mode Cycle Time	t _{CELCEL}	t _{PC}	50	—	50	—	55	—	ns	
Access Time from RAS	t _{RELQV}	t _{RAC}	—	65	—	75	—	85	ns	6, 7
Access Time from CAS	t _{CELQV}	t _{CAC}	—	25	—	25	—	25	ns	6, 8
Access Time from Column Address	t _{AVQV}	t _{AA}	—	35	—	40	—	45	ns	6, 9
Access Time from Precharge CAS	t _{CEHQV}	t _{CPA}	—	45	—	45	—	50	ns	6
RAS Pulse Width	t _{RELREH}	t _{RAS}	65	10 k	75	10 k	85	10 k	ns	
RAS Pulse Width (Fast Page Mode)	t _{RELREH}	t _{RASP}	65	200 k	75	200 k	85	200 k	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	25	—	25	—	25	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	65	—	75	—	85	—	ns	
CAS Precharge to RAS Hold Time	t _{CEHREH}	t _{RHCP}	45	—	45	—	50	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	25	10 k	25	10 k	25	10 k	ns	
Column Address to RAS Lead Time	t _{AVREH}	t _{RAL}	35	—	40	—	45	—	ns	

NOTES:

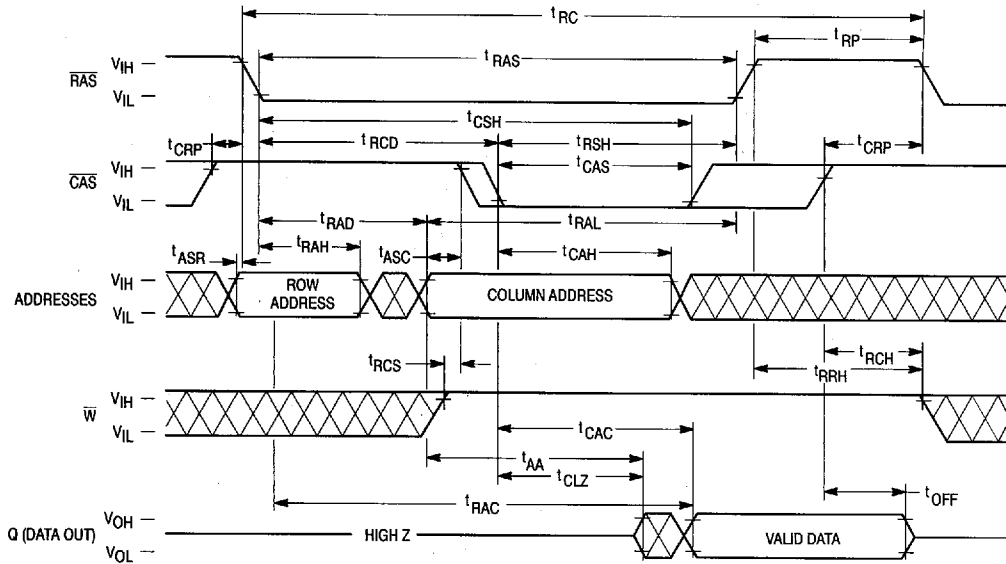
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (-200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that t_{RCD} ≤ t_{RCD} (max).
8. Assumes that t_{RCD} ≥ t_{RCD} (max).
9. Assumes that t_{RAD} ≥ t_{RAD} (max).

WRITE, CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)
 (D and A0 - A10 are Don't Care)

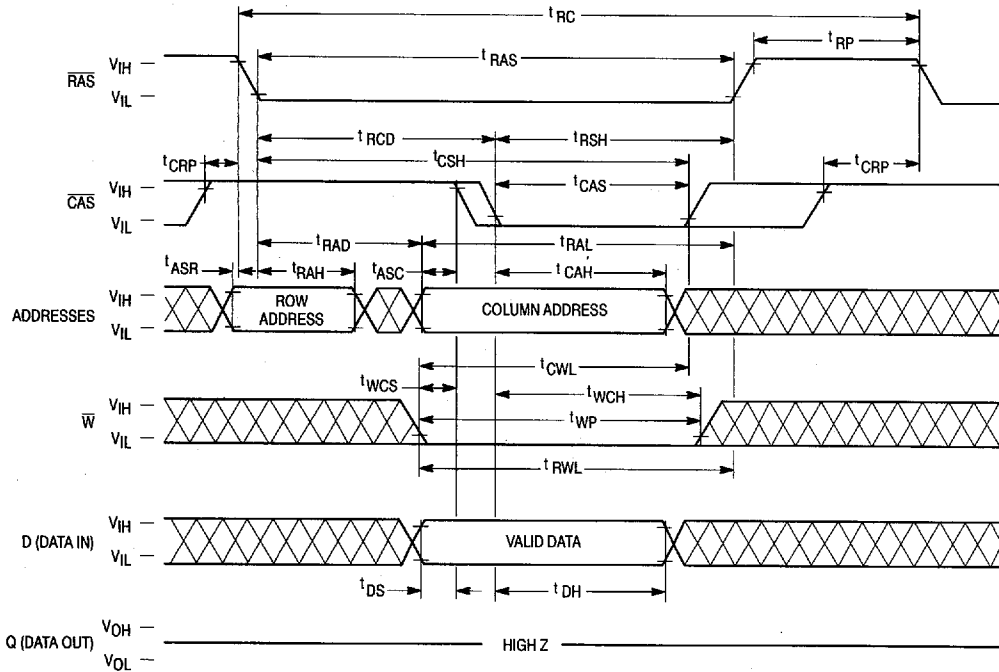


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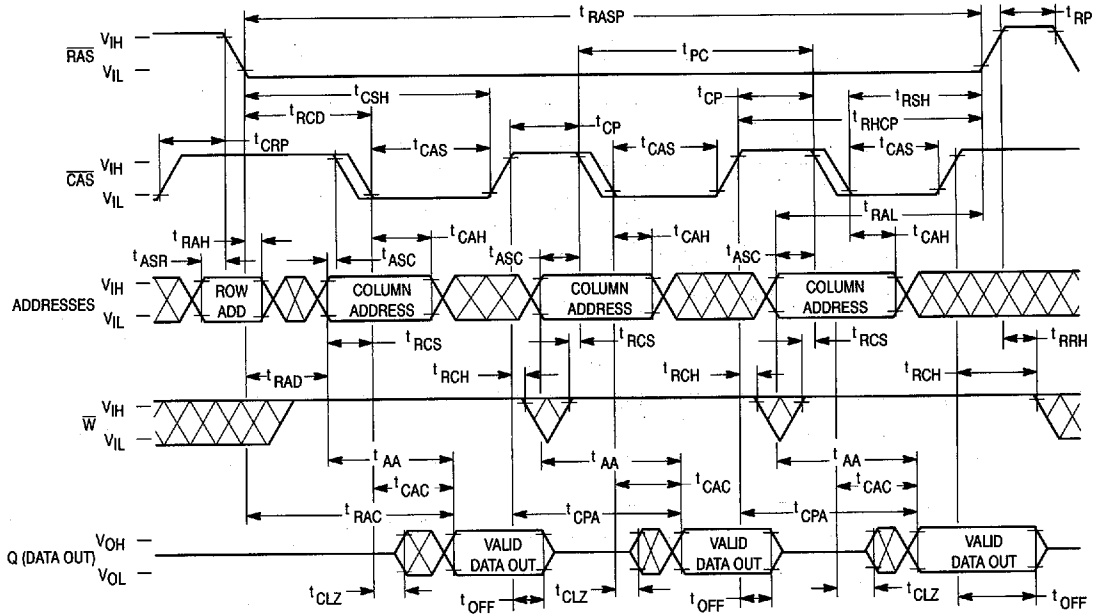
TEST MODE — READ CYCLE



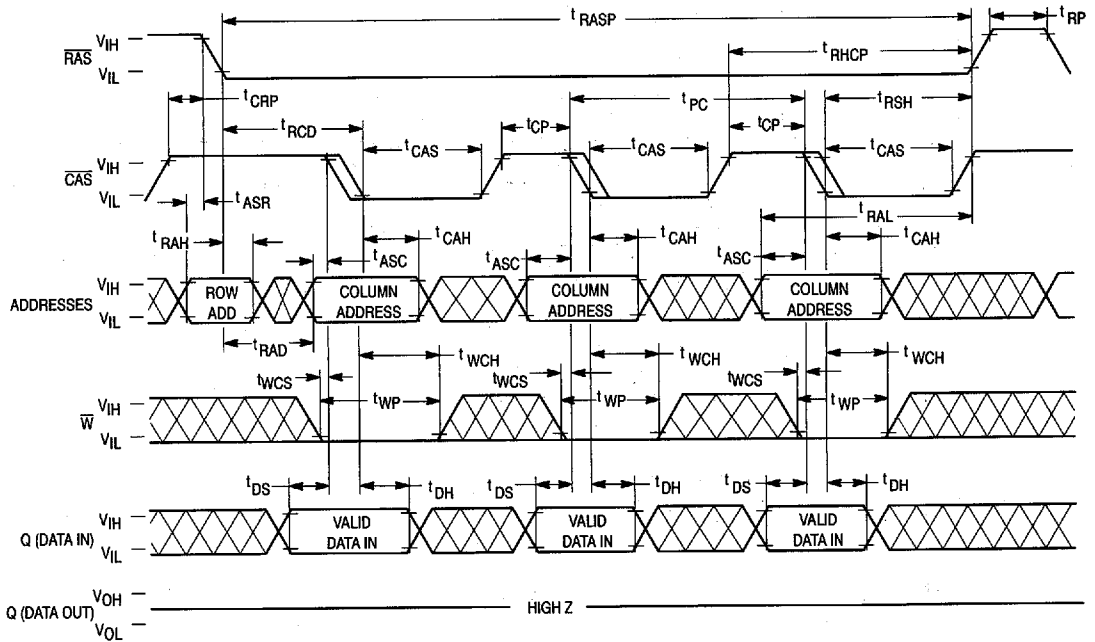
TEST MODE — EARLY WRITE CYCLE



TEST MODE — FAST PAGE MODE READ CYCLE

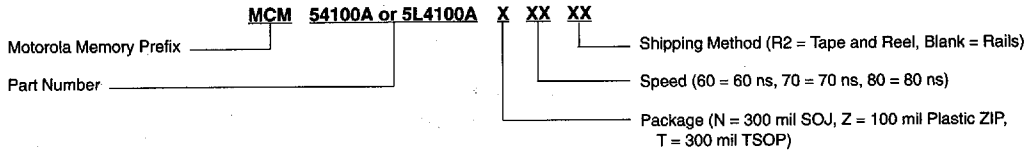


TEST MODE — FAST PAGE MODE EARLY WRITE CYCLE



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ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM54100AN60	MCM54100AN60R2	MCM54100AZ60	MCM54100AT60	MCM54100AT60R2
	MCM54100AN70	MCM54100AN70R2	MCM54100AZ70	MCM54100AT70	MCM54100AT70R2
	MCM54100AN80	MCM54100AN80R2	MCM54100AZ80	MCM54100AT80	MCM54100AT80R2
	MCM5L4100AN60	MCM5L4100AN60R2	MCM5L4100AZ60	MCM5L4100AT60	MCM5L4100AT60R2
	MCM5L4100AN70	MCM5L4100AN70R2	MCM5L4100AZ70	MCM5L4100AT70	MCM5L4100AT70R2
	MCM5L4100AN80	MCM5L4100AN80R2	MCM5L4100AZ80	MCM5L4100AT80	MCM5L4100AT80R2

NOTE: For mechanical data, please see Chapter 10.

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