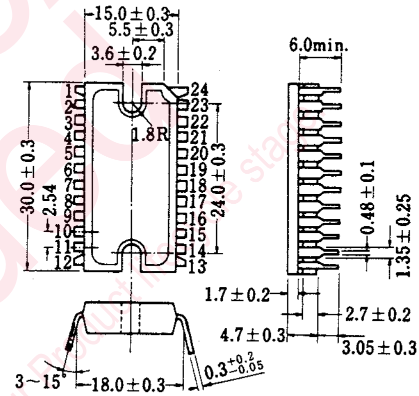
AN6387

VTR Cylinder Motor Drive Circuit

■ Outline

The AN6387 is an integrated circuit designed for VCR cylinder DD motor drive.

Unit : mm

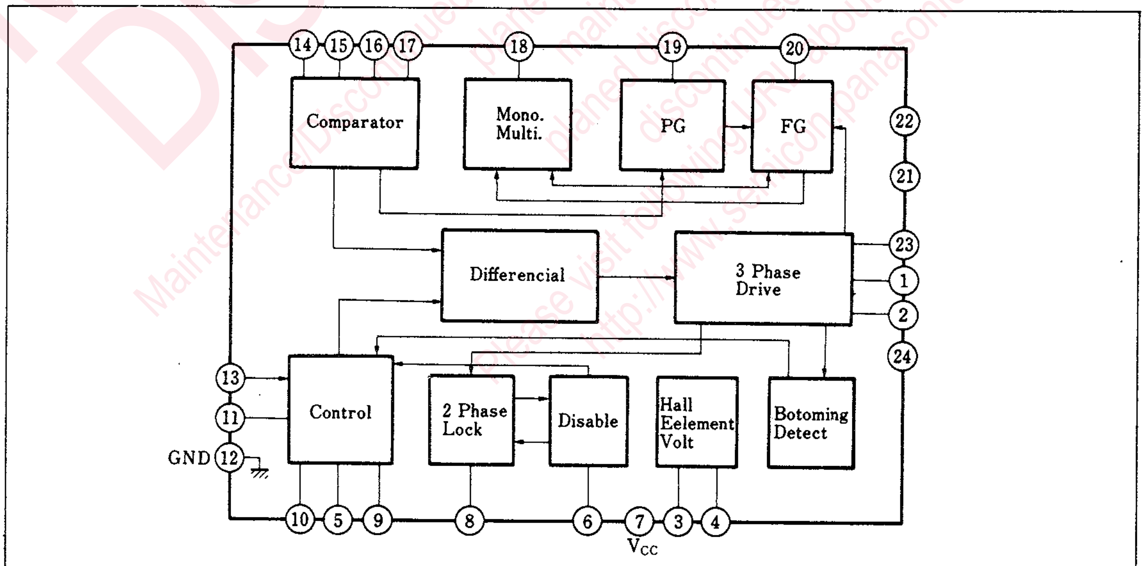


24-Lead DIL Plastic Package (Power Type)

■ Features

- The functions consist of :
  - 3-Phase motor drive circuit
  - 2 Phase-Hall element input circuit
  - PG, FG, generator circuit
  - Motor lock detector
- Supply voltage either 9V or 12V

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Drive Output (2)	13	Torque Direct Voltage
2	Drive Output (3)	14	Hall Element Voltage Input (1)
3	Hall Element Ref. Voltage	15	Hall Element Voltage Input (2)
4	Hall Element Voltage	16	Hall Element Voltage Input (3)
5	Motor Current Detect	17	Hall Element Voltage Input (4)
6	Disable	18	MM Output
7	V_{CC}	19	PG Output
8	Lock Detect	20	FG Output
9	Phase Compensation	21	V_M
10	Phase Compensation	22	NC
11	Servo Ref. Voltage	23	Drive Output(1)
12	GND	24	Total Current Output

■ Absolute Maximum Ratings (Ta=25℃)

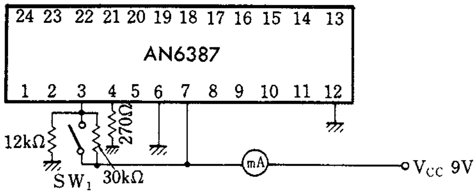
Item	Symbol	Rating		Unit	Note
Supply voltage	V_{CC}	14.4		V	
Circuit voltage	V_{n-12}	0	40	V	n=1, 2, 23
Circuit voltage	V_{21-12}	0	24	V	
Circuit current	I_n	0	1500	mA	n=1, 2, 23
Power dissipation	P_D	10		W	
Operating ambient temperature	T_{opr}	−20~+70		℃	
Storage temperature	T_{stg}	−40~+150		℃	

■ Electrical Characteristics (Ta=25℃±2℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total circuit current	I_{tot}	1	V_{CC}=9V disable	4.0		20	mA
ET-ATC transfer gain	$G_{(IO)}$	2	V_{CC}=9V	0.86		1.06	
ATC limit voltage	$V_{(lim)}$	2	V_{CC}=9V when a full torque specified	0.44		0.50	V
Saturation detection gain	$G_{(S)}$	3	V_{CC}=9V, R_d=0.47Ω	0.5		1.5	
Saturation detection start voltage	$V_{(Det\ 1)}$	3	V_{CC}=9V, R_d=0.47Ω	1.0		1.8	V
Saturation detection end voltage	$V_{(Det\ 2)}$	3	V_{CC}=9V, R_d=0.47Ω	0.5		1.0	V
HV output voltage	V_{HV}	1	V_{CC}=9V, V_{SV}=2.6V, R_{HV}=270	2.1			V
HV protective voltage	$V_{(Protect)}$	1	V_{CC}=9V, V_{SV}=V_{CC}	3.5		4.3	V
$\overline{DS}$ level voltage	$V_{\overline{DS}}$	2	V_{CC}=9V			1.2	V
ETR voltage	V_{ETR}	2	V_{CC}=9V	4.3		4.7	V
HEM, $\overline{HEM}$, HES, $\overline{HES}$ bias current	I_{Bias}	2	V_{CC}=9V	−6			μA
Hes-$\overline{HES}$ comparator offset voltage	$V_{I(offset)S}$	2	V_{CC}=9V	−6		6	mV
HEM-$\overline{HEM}$ comparator offset voltage	$V_{I(offset)\cdot M}$	2	V_{CC}=9V	−6		6	mV
PG minimum voltage	V_{OL19}	2	V_{CC}=9V, 47kΩ to Pin⑲→5V			0.5	V
FG minimum voltage	V_{OL20}	4	V_{CC}=9V, 47kΩ to Pin⑳→5V			0.5	V
BEG take-out voltage	V_{BFG}	4	V_{CC}=V_M=9V	0.6		1.0	V

Note) Operating supply voltage range $V_{CC(opr)}$= 8~13V (V_{7-12})

Test Circuit 1 (I_{tot}, V_{HV}, $V_{(Protect)}$)

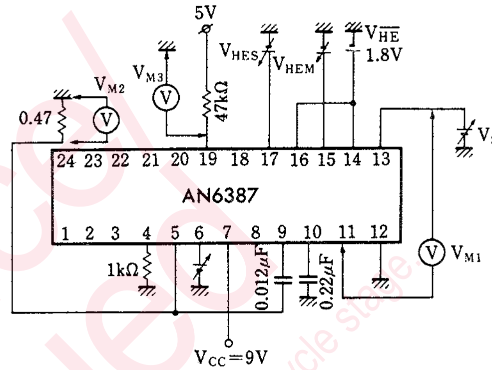


SW₁ : Open, Current value I_{CC}

SW₁ : Open, Pin③ voltage 2.6V··· Pin-④ V_{HV}

SW₁ : Short, Pin④ voltage···$V_{(Protect)}$

Test Circuit 2 ($G_{(IO)}$, $V_{(lim)}$, $V_{\overline{DS}}$, V_{ETR}, I_{Bias}, $V_{I(offset)S}$, $V_{I(offset)M}$, V_{OL19})



Set $V_{HES}=V_{HEM}=2V$, $V_{\overline{DS}}=2V$, and V_S to 0−6V, and read V_{M1} V_{M2}.

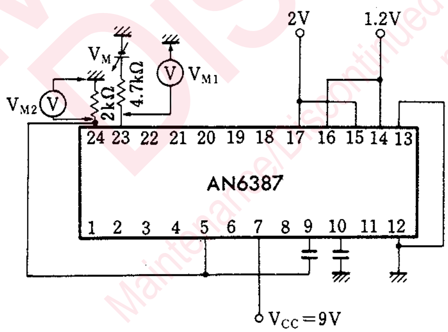
G_{IO}, $V_{(lim)}$

(V_{HES}, V_{HEM} ,and $V_{\overline{HE}}$ current···I_{Bias})

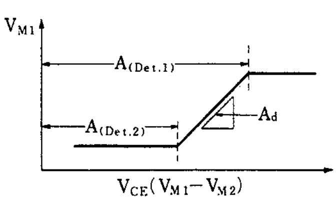
V_{M1} reading when V_S=0V···−V_{ETR}

$V_{HES}=V_{HEM}=2V$, $V_{DS}=2V$
voltage of $V_{MES}-V_{FE}$ when a V_{M3} voltage is lower in lowering V_{HES} continuously from 2V : $V_{I(offset)S}$ Next, voltage of $V_{HEM}-V_{\overline{HE}}$ when a V_{M3} voltage is increased in lowering V_{HEM} continuously from 2V : $V_{I(offset)M}$ V_{M3} minimum voltage···V_{OL19}

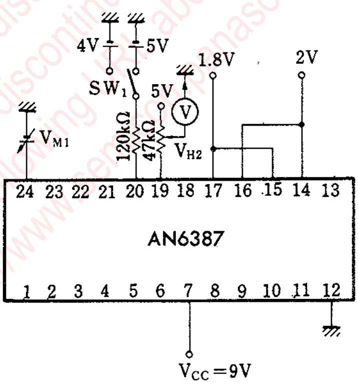
Test Circuit 3 ($G_{(S)}$, $V_{(Det.1)}$, $V_{(Det.2)}$)



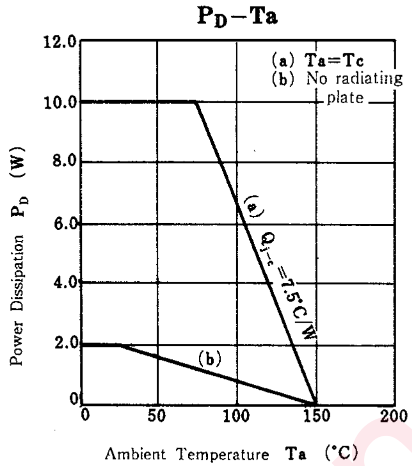
Set V_M to 2V. Increase it continuously to obtain the figure below.



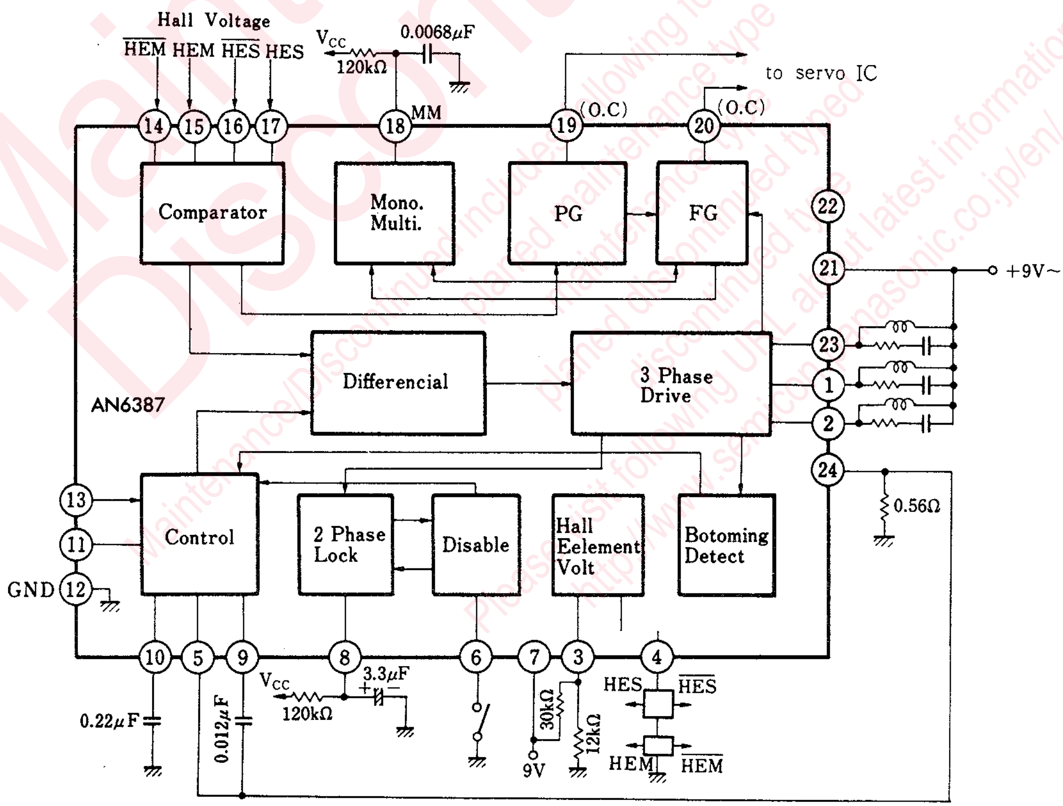
Test Circuit 4 (V_{OL20}, V_{BFG})



When S_1=5V and V_{M1}=9V, V_{M2}···High voltage When S_1 =%V and V_{M1}=9V, V_{M2}···Low voltage···V_{OL20} At this time, increase V_{M1} continuously up to 10V. Next set S_1= 5V, lower V_{M1} continuously, and V_{M1} voltage when V_{M2} becomes a High voltage···V_{BFG}



■ Application Circuit



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