DRAM

16 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 3mW standby; 330mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's ***Military Data Book.***

• Operating Temperature, T_A	
Commercial (0°C to +70°C)	None

- Part Number Example: MT4C16M1D1DJ-6

PIN ASSIGNMENT (Top View)

24-Pin SOJ
(Q-3)

Vcc	1	28	Vss
D	2	27	Q
NC	3	26	NC
WE	4	25	CAS
RAS	5	24	NC
A11	6	23	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

GENERAL DESCRIPTION

The MT4C16M1D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. RAS is used to latch the first 12 bits and CAS the latter 12 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires CAS to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN refresh) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.