

6 Output Telecom Oscillator

- Common multiple telecom frequencies 1 package
- Reduced EMI
- Differential PECL Output

Applications

- SDH / SONET
- Digital Switching
- Test Equipment
- Cellular Telephony
- Land Mobile Radio
- Communications

Series **CCE6ET**



Part Numbering Example: CCE6ET 1A

CCE6ET	1A
SERIES	PACKAGE STYLE
1A	= 14 pin dip
9	= 9.6 x 11.4

Specifications:	Min	Typ	Max	Unit
Frequency Range:				
* Output PECL +		155.52		MHz
* Output PECL -		155.52		MHz
Output A CMOS		19.44		MHz
Output B CMOS		38.88		MHz
Output C CMOS		77.76		MHz
Output R Fixed		12.00		MHz
Available Stability Options:	-50		50	ppm
Supply Voltage:	3.135	3.3	3.465	V
Operating Temperature Range Options:	-40		85	°C
Storage Temperature:	-55		125	°C
Duty Cycle:	40 45		60 55	% %
Start-Up Time:		3	10	ms
Aging (PPM/1st Year): Ta=25C, Vdd=3.3V			±5	
Static Discharge Voltage Mil-Std 883, method 3015	2000			V
Output Load:			15	pF
Output Level:	PECL/CMOS			
Packaging:	25 / Tube Tape & Reel			14 pin SMD

Notes: Recommended .01 µF bypass capacitor from Vcc to GND. Capacitor should be as close to oscillator as possible.
* LV PECL outputs require an external termination network



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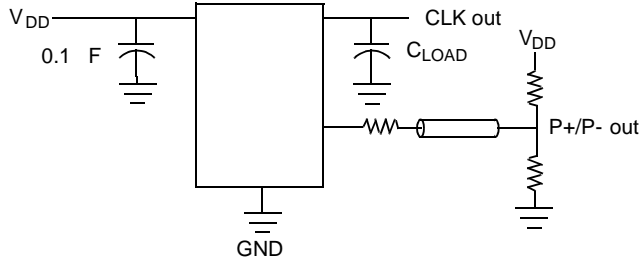
Series **CCE6ET****Electrical Characteristics**

DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
Ioh	Output High Current	Voh = Vdd - 0.5, Vdd = 3.3 V	12	24		mA
Iol	Output Low Current	Vol = .5, Vdd = 3.3 V	12	24		mA
Vih	High Level Input Voltage	CMOS levels, % of Vdd	70			%Vdd
Vil	Low-Level Input Voltage	CMOS levels, % of Vdd			30	%Vdd
Iih	Input High Current	Vin = Vdd - 0.3 V		<1	10	μA
Iil	Input Low Current	Vin = + 0.3 V		<1	10	μA
Ioz	Output Leakage Current	Tri-state outputs			10	μA
Idd	Total Power Supply Current	All outputs active and connected to a load		75		mA
Idds	Shutdown Power Supply Curr	Shutdown active		5	20	μA
OE	Output Enable	Connect to Vdd to enable and Gnd to disable				
SO	Suspend	Connect to Gnd for normal operation				

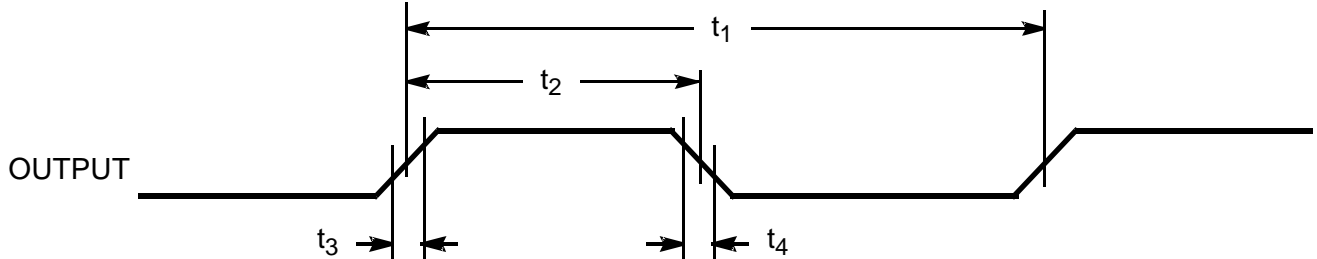
Output Clock Switching Characteristics

DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
1/t1	Output Frequency	See page 1 for outputs				
t3	Rising Edge Slew Rate	Output clock rise time, 20% – 80% Vdd	0.75	1.4		V/ns
t4	Falling Edge Slew Rate	Output clock fall time, 20% – 80% Vdd	0.75	1.4		V/ns
t5	Output Tri-state timing after SD/OE switches	Time for output to enter/leave Tri-state mode		150	300	ns
t6	Clock Jitter measured at Vdd/2	Peak-to-Peak period jitter, CLK outputs		200		ps
v7	P+/P- Crossing Point	Crossing point ref. to Vdd/2 Balanced Resistor Network	-0.2	0	0.2	V

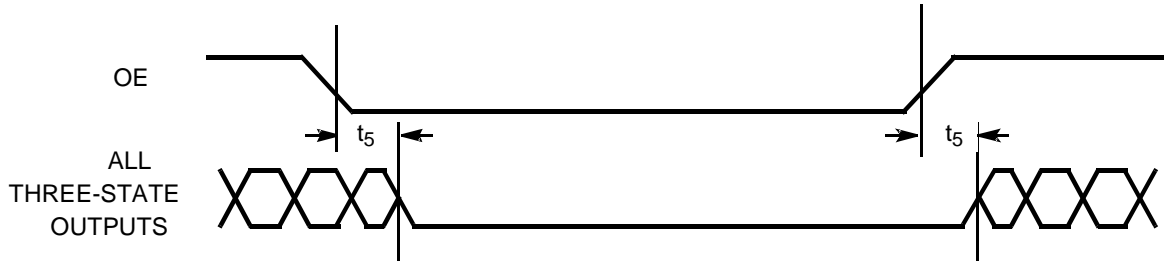
TEST CIRCUIT



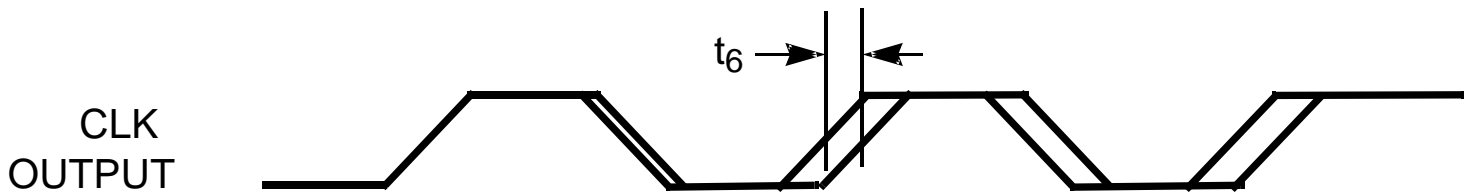
ALL OUTPUTS, DUTY CYCLE, RISE/FALL TIME



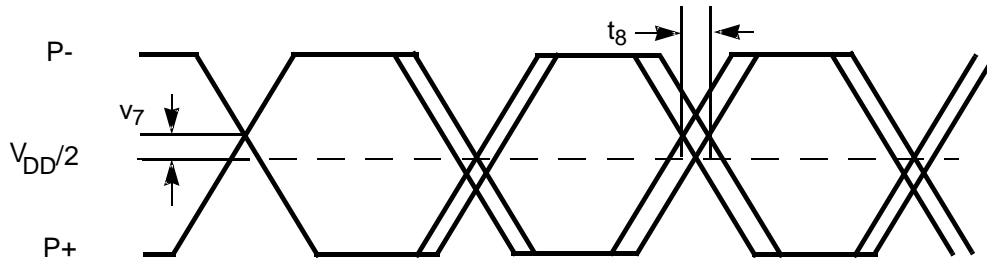
OUTPUT 3-STATE TIMING



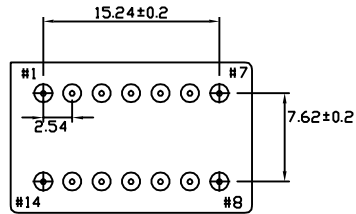
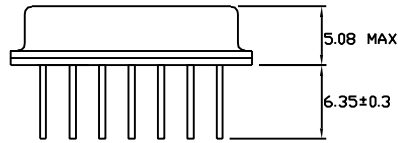
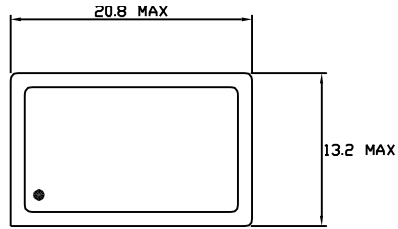
CLK OUTPUT JITTER



P+/P- CROSSING POINT AND JITTER



DIP

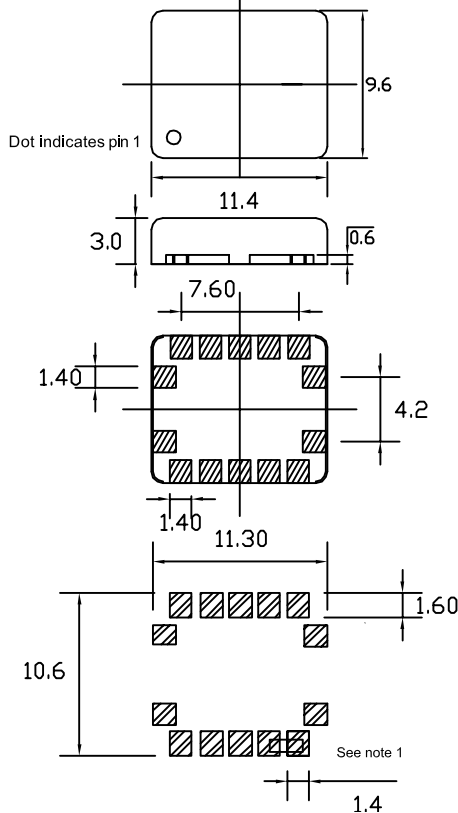


Dimensions are in mm

PIN FUNCTION

- PIN 1 OE
- PIN 2 SUSPEND (CONNECT TO GND)
- PIN 3 VDD
- PIN 4 77.76 MHz CMOS OUTPUT
- PIN 5 CONNECT TO PIN 6
- PIN 6 CONNECT TO PIN 5
- PIN 7 GND
- PIN 8 12 MHz REF CLOCK OUTPUT
- PIN 9 155.52 MHz PECL - OUTPUT
- PIN10 155.52 MHz PECL + OUTPUT
- PIN 11 FACTORY USE (MAKE NO CONNECTION)
- PIN 12 FACTORY USE (MAKE NO CONNECTION)
- PIN 13 19.44 MHz COMS OUTPUT
- PIN 14 38.88 MHz COMS OUTPUT

SMD



PIN FUNCTION

- PIN 1 FACTORY USE (MAKE NO CONNECTION)
- PIN 2 OE
- PIN 3 VDD
- PIN 4 77.76 MHz CMOS OUTPUT
- PIN 5 CONNECT TO PIN 6
- PIN 6 CONNECT TO PIN 5
- PIN 7 GND
- PIN 8 12 MHz REF CLOCK OUTPUT
- PIN 9 155.52 MHz PECL - OUTPUT
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- PIN 11 FACTORY USE (MAKE NO CONNECTION)
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Dimensions in mm
Recommended solder pad layout

Note1:
For proper operation pin 5 must be connected to pin 6

