

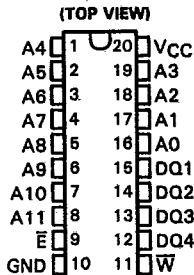
SM64C16, SMJ64C16
4096-WORD BY 4-BIT STATIC RAMS

TEXAS INSTR (ASIC/MEMORY) 25E D

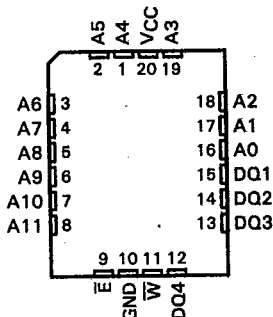
MARCH 1987—REVISED NOVEMBER 1987

- 4096 x 4 Organization
- Common I/O
- Military Temperature Range . . . -55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
 - '64C16-25 . . . 25 ns
 - '64C16-35 . . . 35 ns
 - '64C16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Automatic Power Down when Deselected
 - 125 µA MAX Standby Current at CMOS Levels
- Low Power Dissipation (VCC = 5.5 V)
 - Active . . . 660 mW
 - Standby . . . 55 mW MAX (TTL Levels)
 - Standby . . . 0.68 mW MAX (CMOS Levels)
- Standard and Class B Processing
 - SM Prefix . . . Standard Processing
 - SMJ Prefix . . . Class B Processing
- Packaging Options:
 - 20-Pin Ceramic 300-mil DIP
 - 20-Pad Leadless Ceramic Chip Carrier

JD PACKAGE T-46-23-08



FG PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Addresses
DQ1-DQ4	Data In/Data Out
E	Chip Enable/Power Down
GND	Ground
VCC	5-V Supply
W	Write Enable

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description

The '64C16 is a common I/O, 16,384-bit static random-access memory organized as 4096 words by 4 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six-transistor cell) memory array. The six-transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and extremely low standby power compared to the four-transistor/two-poly load cell, making it ideal for military applications.

The '64C16's static design and control signals (\bar{E} and \bar{W}) remove the need for refresh circuitry and simplify timing requirements. The chip enable pin provides for easy memory expansion and for an automatic powerdown feature. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns.

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operation

addresses (A0-A11)

The 12 address inputs select one of the 4096 4-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down (\bar{E})

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

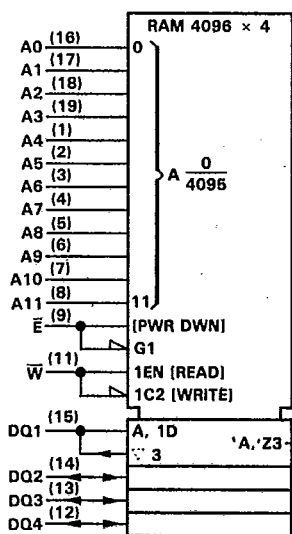
write enable (\bar{W})

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. \bar{W} or \bar{E} must be high when changing addresses to prevent erroneously writing data into a memory location. The \bar{W} input can be driven directly from standard TTL circuits.

data in/data out (DQ1-DQ4)

Data can be written into a selected device when the write-enable input is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fanout of two Series 54 TTL gates, one Series 54S TTL gate, or eight Series 54LS TTL gates. The DQ terminals are in the high-impedance state when chip enable (\bar{E}) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

logic symbol†



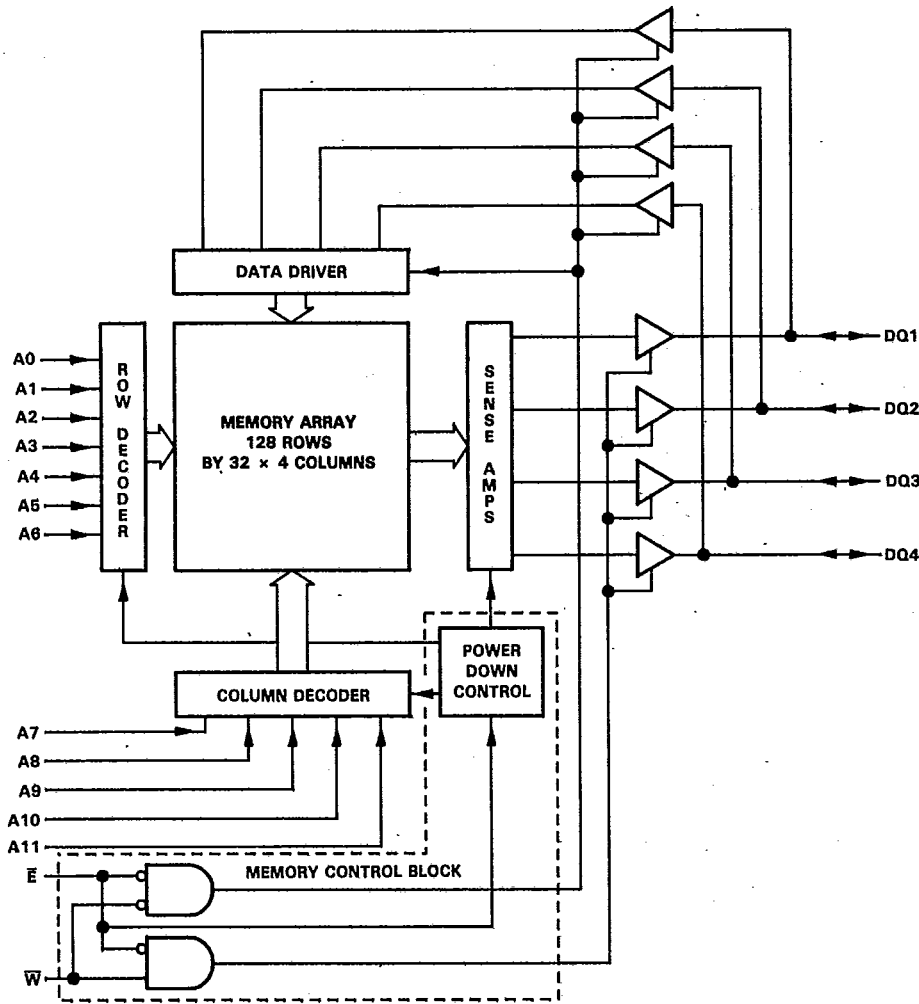
FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
\bar{E}	\bar{W}	DQ1-DQ4		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the JD package.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1)	-0.5 V to 7 V
Input voltage range (see Note 2)	-1 V to 7 V
Output voltage range in high-impedance state	-0.5 V to 7 V
Output current	20 mA
Minimum operating free-air temperature	-55°C
Maximum operating case-temperature	125°C
Storage temperature range	-65°C to 150°C
Latch-up current	200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.

2. V_{IL} (min) of -3 V for short pulse durations. Prolonged operation at V_{IL} levels below -1 V will result in excessive currents that may damage the part.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2		$V_{CC} + 1$	V
V_{IL} Low-level input voltage (see Note 2)	-1		0.8	V
T_C Operating case temperature			125	°C
T_A Operating free-air temperature	-55			°C

NOTE 2: V_{IL} (min) of -3 for short pulse durations. Prolonged operation at V_{IL} levels below -1 V will result in excessive currents that may damage the part.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'64C16-25			'64C16-35			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH} High-level output voltage	$V_{CC} = 4.5 V, I_{OH} = -4 mA$	2.4			2.4			V
V_{OL} Low-level output voltage	$V_{CC} = 4.5 V, I_{OL} = 8 mA$			0.4			0.4	V
I_I Input current (load)	$0 V \leq V_I \leq V_{CC}$	-10		10	-10		10	μA
I_O Output current (leakage)	$0 V \leq V_O \leq V_{CC}$, Output disabled	-50		50	-50		50	μA
I_{OS} Short circuit output current (see Note 3)	$V_{CC} = 5.5 V, V_O = GND$			-350			-350	mA
I_{CC} V_{CC} operating supply current	$V_{CC} = 5.5 V, I_O = 0 mA$			120			120	mA
I_{CCI} V_{CC} supply current (standby)	TTL-level inputs			20			20	mA
	CMOS-level inputs			125			125	μA

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'64C16-46			UNIT
		MIN	TYP	MAX	
V _{OH} High-level output voltage	V _{CC} = 4.5 V, I _{OH} = -4 mA	2.4			V
V _{OL} Low-level output voltage	V _{CC} = 4.5 V, I _{OL} = 8 mA		0.4		V
I _I Input current (load)	0 V ≤ V _I ≤ V _{CC}	-10	10		μA
I _O Output current (leakage)	0 V ≤ V _O ≤ V _{CC} , Output disabled	-60	60		μA
I _{OS} Short circuit output current (see Note 3)	V _{CC} = 5.5 V, V _O = GND		-360		mA
I _{CC} V _{CC} operating supply current	V _{CC} = 5.5 V, I _O = 0 mA		120		mA
I _{CCI} V _{CC} supply current (standby)	TTL-level inputs		20		mA
	CMOS-level inputs	Inputs = V _{CC} ± 0.3, V _{CC} = 5.5 V	125		μA

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

data retention characteristics

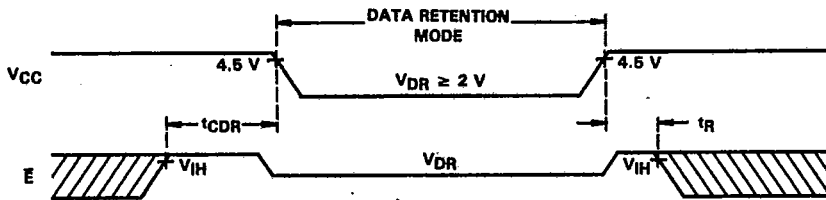
PARAMETER	TEST CONDITION	MIN	TYP†		MAX		UNIT
			V _{CC} @ 2.0 V	V _{CC} @ 3.0 V	V _{CC} @ 2.0 V	V _{CC} @ 3.0 V	
V _D V _{CC} for data retention	E ≥ V _{CC} - 0.3 V, V _{IN} ≥ V _{CC} - 0.3 V or ≤ GND + 0.3 V	2.0	-	-	-	-	V
I _{CCDR} Data retention current			3	6	60	75	μA
t _{CDR} Chip deselect to data retention time		0	-	-	-	-	ns
t _R Operation recovery time		t _{c(RD)} ‡	-	-	-	-	ns
I _I § Input leakage current			-	-	1	-	μA

†TYP values listed are typical values at 25°C.

‡t_{c(RD)} = read cycle time.

§This parameter is guaranteed but not tested.

data retention waveform



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capacitance, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$ †

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$			4	pF
C_o Output capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$			7	pF

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'64C16-25			'64C16-35			'64C16-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	20			30			35			ns
$t_{su(W)rd}$	Write enable high to chip enable low (read command setup)	0			0			0			ns
t_{ELWH}	Chip-enable low to end of write	25			30			35			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			15			ns
$t_{h(W)rd}$	Write enable low from chip enable high (read command hold)	0			0			0			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			3			ns
t_{ELIH}	Delay time, chip-enable low to power up‡	5			5			5			ns
t_{EHIL}	Delay time, chip-enable high to power down‡			35			35			35	ns
t_{AVWH}	Address setup to write end	20			30			35			ns

‡This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER	TEST CONDITIONS	'64C16-25		'64C16-35		'64C16-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_a(A)$	Access time from address	25		35		45		ns
$t_a(E)$	Access time from chip enable low	25		35		45		ns
$t_v(A)$	Output data valid after address change	0		0		0		ns
$t_{en(W)}$	Output enable time from write enable high†	6		6		6		ns
$t_{en(E)}$	Output enable time from chip enable low	5		5		5		ns
$t_{dis(E)}$	Output disable time from chip enable high‡	15		20		25		ns
$t_{dis(W)}$	Output disable time from write enable low‡	10		15		20		ns

†Transition is measured $\pm 500\text{ mV}$ from steady state voltage. This parameter is guaranteed but not tested.

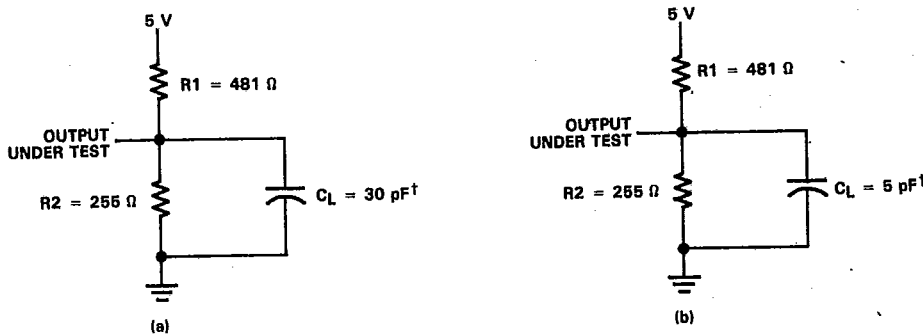
‡This parameter is guaranteed but not tested.

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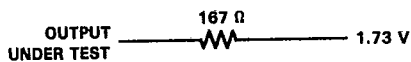
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PARAMETER MEASUREMENT INFORMATION

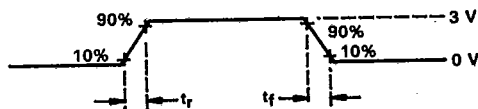


THEVENIN EQUIVALENT OF (a) OR (b)



[†]C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT



NOTE 4: t_r and t_f ≤ 6 ns.

FIGURE 2. TRANSITION TIMES

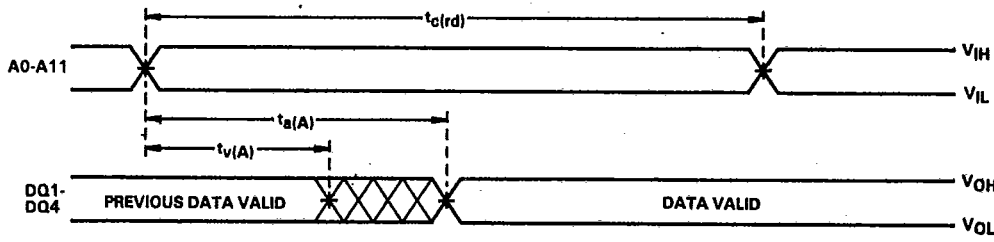
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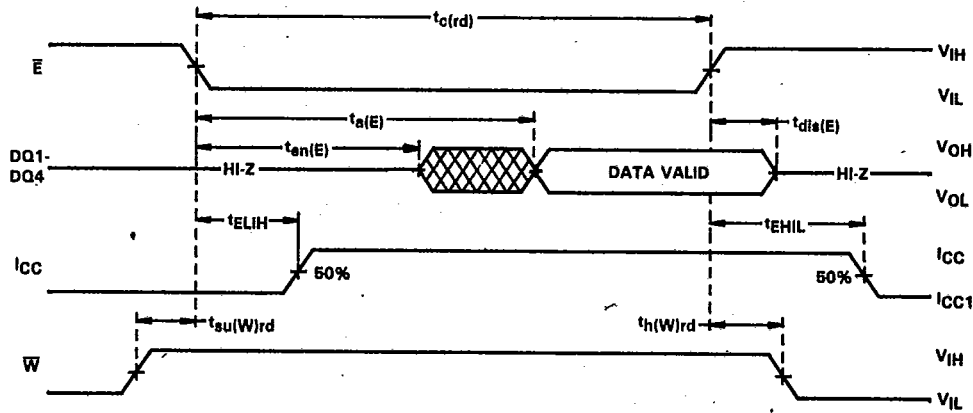
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read cycle timing from address†



†W is high, and \bar{E} is low.

read cycle timing from chip enable‡



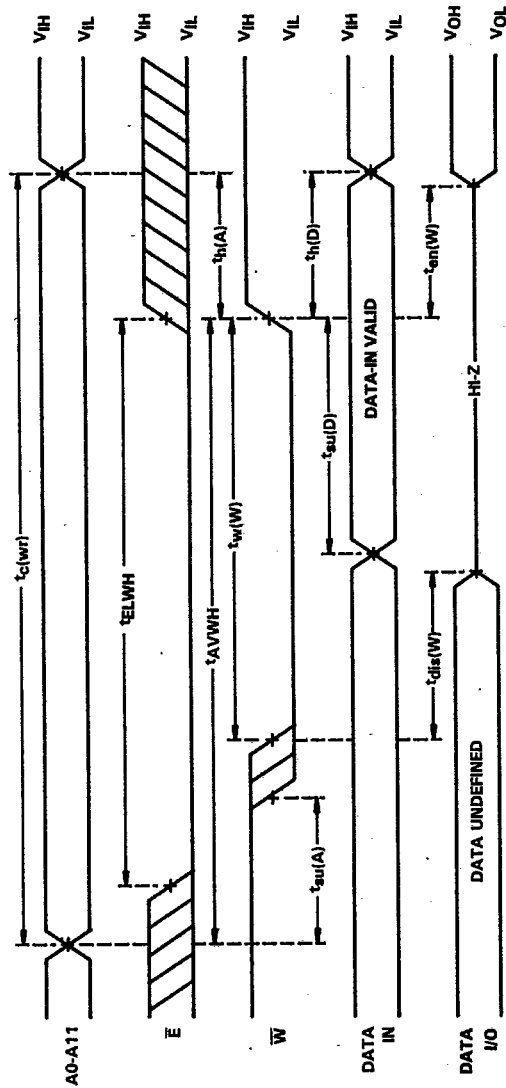
‡W is high, address is valid prior to or simultaneously with the high-to-low transition of \bar{E} .

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write cycle timing controlled by write enable†



†E or W must be high during address transitions.

NOTE: For both WE-controlled and CE-controlled write operations, the internal write time of the memory is defined by the overlap of E low and W high. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge which terminates the write.

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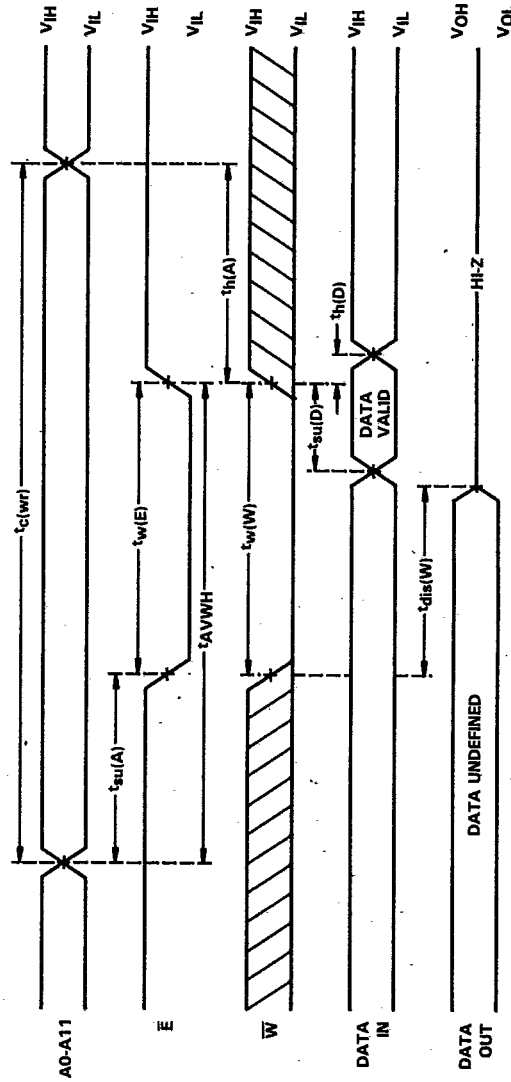
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write cycle timing controlled by chip enable†

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†E or W must be high during address transitions.