

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μ PD160061 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 65 MHz when driving at 2.7 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 384 outputs
- Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- Logic power supply voltage (V_{DD1}): 2.3 to 3.6 V
- Driver power supply voltage (V_{DD2}): 7.5 to 9.5 V
- High-speed data transfer: $f_{CLK} = 65$ MHz MAX. (internal data transfer speed when operating at $V_{DD1} = 2.7$ V)
40 MHz MAX. (internal data transfer speed when operating at $V_{DD1} = 2.3$ V)
- Output dynamic range: $V_{SS2} + 0.2$ V to $V_{DD2} - 0.2$ V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Input data inversion function (capable of controlling by each input port) (POL21, POL22)
- Apply for heavy load, light load
- Semi slim-chip shaped

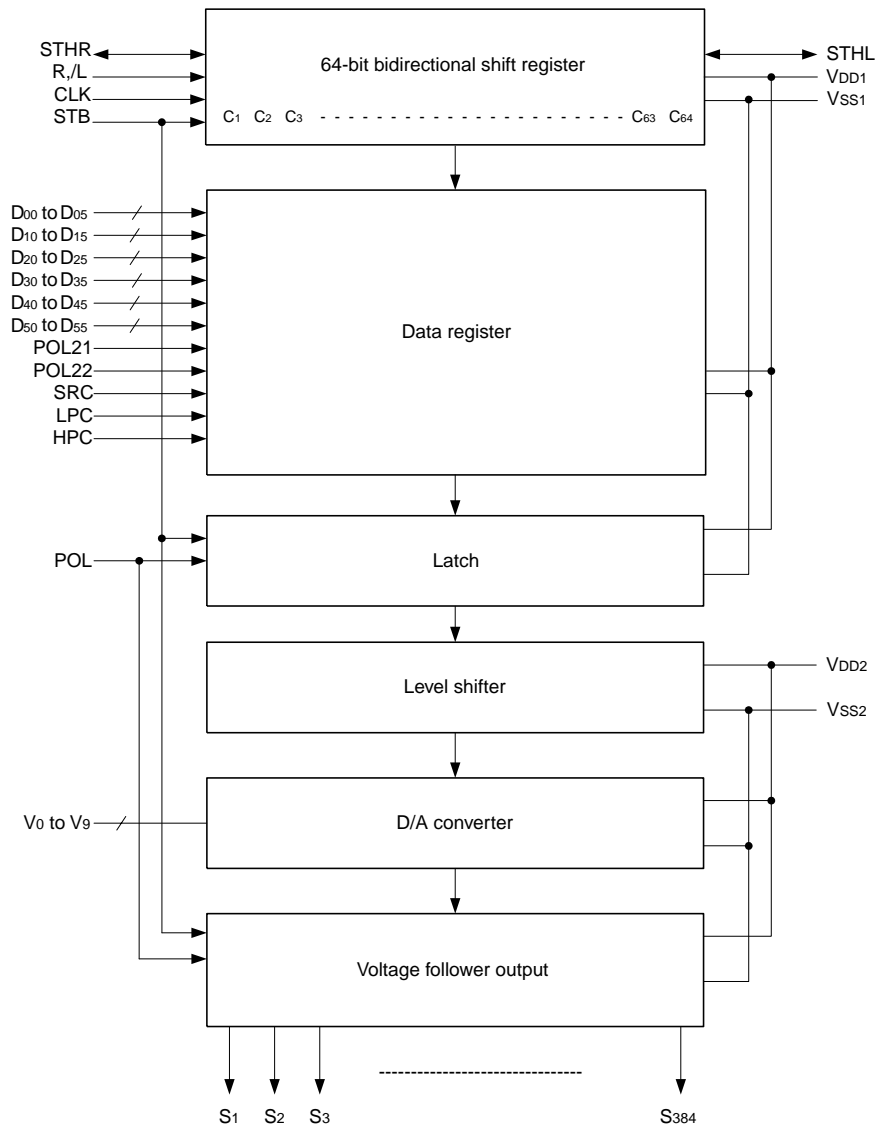
ORDERING INFORMATION

Part Number	Package
μ PD160061N-xxx	TCP (TAB package)
μ PD160061NL-xxx	COF (COF package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

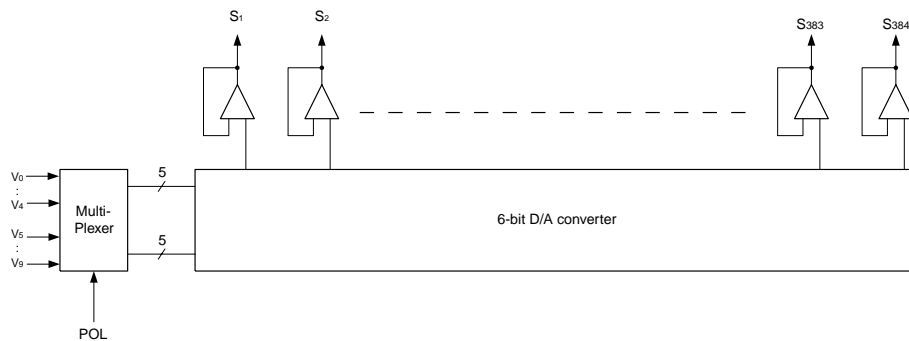
The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM

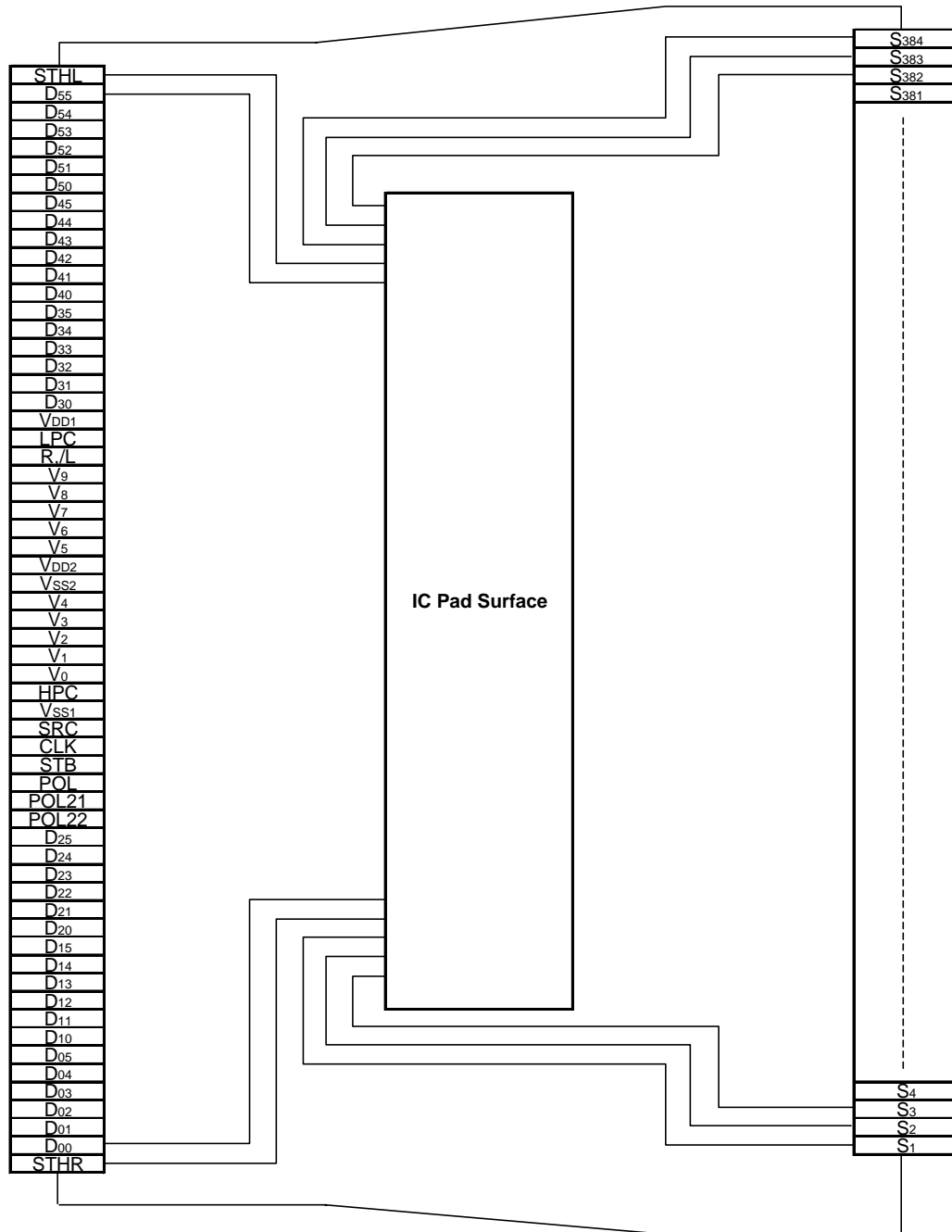


Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (Copper foil surface: Face-up)
 (μPD160061N-xxx: TCP (TAB package) / μPD160061NL-xxx: COF (COF package))



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S ₁ to S ₃₈₄	Driver output	Output	The D/A converted 64-gray-scale analog voltage is output.
D ₀₀ to D ₀₅	Display data input	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D _{X0} : LSB, D _{X5} : MSB
D ₁₀ to D ₁₅			
D ₂₀ to D ₂₅			
D ₃₀ to D ₃₅			
D ₄₀ to D ₄₅			
D ₅₀ to D ₅₅			
R,/L	Shift direction control	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR input, S ₁ →S ₃₈₄ , STHL output R,/L = L (left shift): STHL input, S ₃₈₄ →S ₁ , STHR output
STHR	Right shift start pulse input/output	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Fetching of display data starts when H is read at the rising edge of CLK. When right shift: STHR input, STHL output When left shift: STHL input, STHR output A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is valid.
STHL	Left shift start pulse input/output		
CLK	Shift clock input	Input	Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 66th clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch input	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge of the STB, the gray scale voltage is supplied to the driver. When STB = H period, driver output level is Hi-Z (High impedance). It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	Input	POL = L: The S _{2n-1} output uses V ₀ to V ₄ as the reference supply. The S _{2n} output uses V ₅ to V ₉ as the reference supply. POL = H: The S _{2n-1} output uses V ₅ to V ₉ as the reference supply. The S _{2n} output uses V ₀ to V ₄ as the reference supply. S _{2n-1} indicates the odd output, and S _{2n} indicates the even output. Input of the POL signal is allowed the setup time (t _{POL-STB}) with respect to STB's rising edge.
POL21, POL22	Data inversion input	Input	Data inversion can invert when display data is loaded. POL21: D ₀₀ to D ₀₅ , D ₁₀ to D ₁₅ , D ₂₀ to D ₂₅ , data inversion can invert display data POL22: D ₃₀ to D ₃₅ , D ₄₀ to D ₄₅ , D ₅₀ to D ₅₅ , data inversion can invert display data POL21, POL22 = H: Data inversion loads display data after inverting it. POL21, POL22 = L: Data inversion does not invert input data.
LPC, HPC	Bias current control input	Input	Please refer to panel loads and driver power supply voltage (V _{DD2}), when set up these pins. Refer to 10. BIAS CURRENT CONTROL BY LPC AND HPC . LPC pin is pulled down to the V _{SS1} inside the IC, HPC pin is pulled up to the V _{DD1} inside the IC.

(2/2)

Pin Symbol	Pin Name	I/O	Description
SRC	High driving time control	Input	This pin is set up to high drive time of the output amplifier. Please decide the pin setting refer to panel loads and one horizontal period. SRC pin is pulled up to the V _{DD1} inside the IC. SRC = H or open: High drive time 64 CLK (Normally period mode) SRC = L: High drive time 128 CLK (Long time mode) Refer to 9. SRC AND HIGH DRIVE TIME.
V ₀ to V ₉	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. V _{DD2} – 0.2 V ≥ V ₀ > V ₁ > V ₂ > V ₃ > V ₄ ≥ 0.5 V _{DD2} V _{DD2} – 0.3 V ≥ V ₅ > V ₆ > V ₇ > V ₈ > V ₉ ≥ V _{SS2} + 0.2 V
V _{DD1}	Logic power supply	–	2.3 to 3.6 V
V _{DD2}	Driver power supply	–	7.5 to 9.5 V
V _{SS1}	Logic ground	–	Grounding
V _{SS2}	Driver ground	–	Grounding

- Cautions**
1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V₀ to V₉ in that order. Reverse this sequence to shut down.
 2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1} to V_{SS1} and V_{DD2} to V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V₀, V₁, V₂,....., V₉) and V_{SS}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD160061 incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel γ-compensated voltages to V_{0'} to V_{63'} and V_{0''} to V_{63''} is almost equivalent, resistor ratio is shown in Figure 5-2. For the 2 sets of five γ-compensated power supplies, V₀ to V₄ and V₅ to V₉, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the γ-compensated power supplies V₁ to V₃ and V₆ to V₈.

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2} and V_{SS2}, common electrode potential V_{COM}, and γ-corrected voltages V₀ to V₉ and the input data. Be sure to maintain the voltage relationships of below.

$$V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5 V_{DD2}$$

$$0.5 V_{DD2} - 0.3 V \geq V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.2 V$$

Figures 5-3 indicates the relationship between the input data and output voltage.

Figure 5-1. Relationship between Input Data and γ-corrected Power Supplies

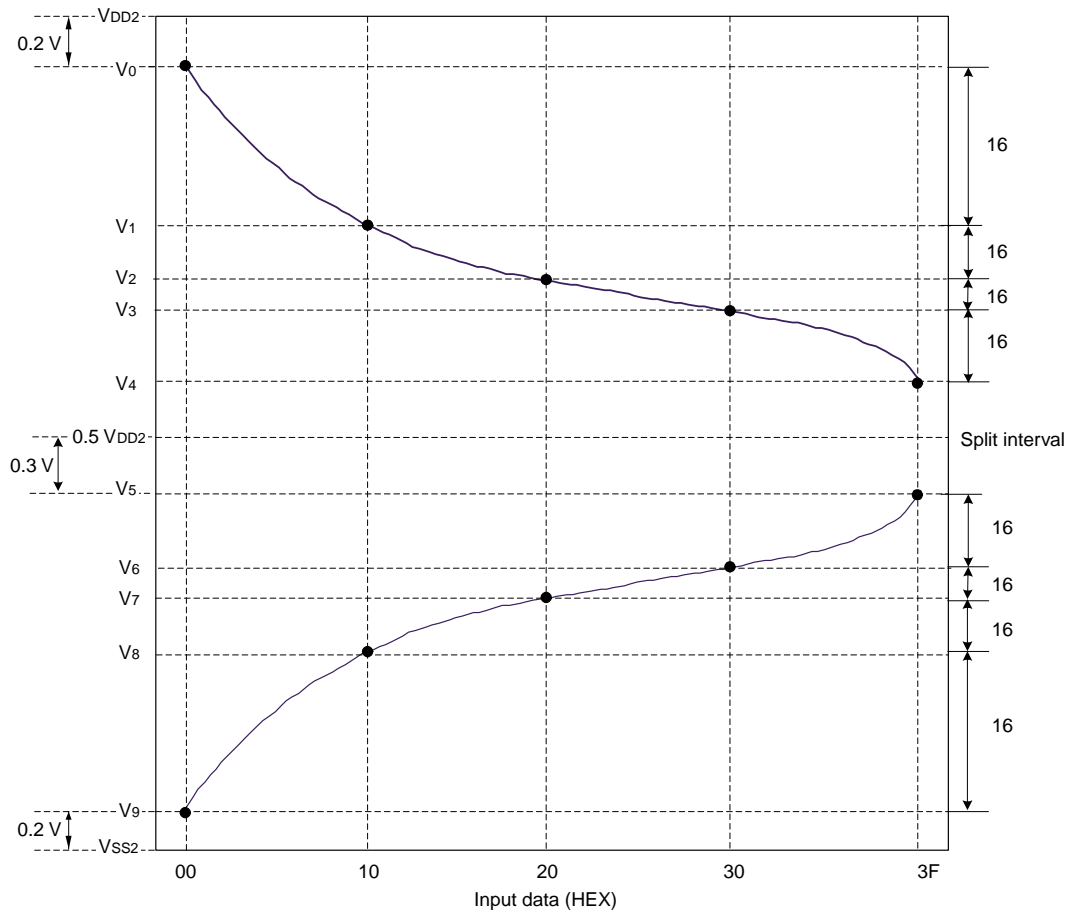
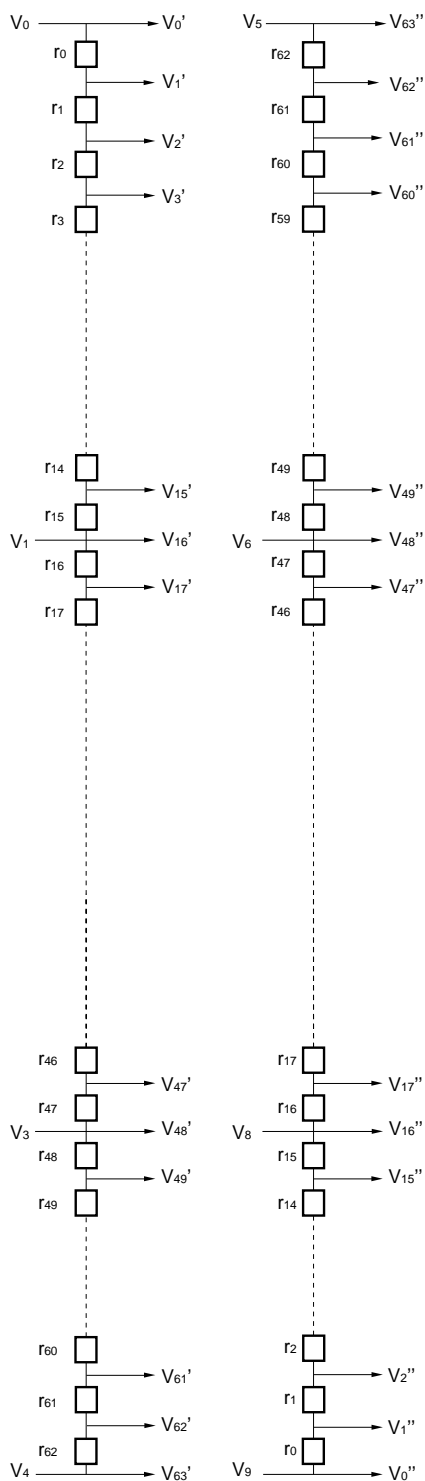


Figure 5-2. γ -corrected Voltages and Ladder Resistors Ratio



m	Ratio	Value (TYP.)
r0	8.5	800
r1	7.5	750
r2	7.0	700
r3	6.5	650
r4	6.0	600
r5	5.5	550
r6	5.5	550
r7	5.0	500
r8	5.0	500
r9	4.0	400
r10	4.0	400
r11	3.5	350
r12	3.5	350
r13	3.5	350
r14	3.0	300
r15	3.0	300
r16	3.0	300
r17	2.5	250
r18	2.5	250
r19	2.5	250
r20	2.0	200
r21	2.0	200
r22	2.0	200
r23	1.5	150
r24	1.5	150
r25	1.5	150
r26	1.5	150
r27	1.0	100
r28	1.0	100
r29	1.0	100
r30	1.0	100
r31	1.0	100
r32	1.0	100
r33	1.0	100
r34	1.0	100
r35	1.0	100
r36	1.0	100
r37	1.0	100
r38	1.0	100
r39	1.0	100
r40	1.0	100
r41	1.0	100
r42	1.0	100
r43	1.0	100
r44	1.0	100
r45	1.0	100
r46	1.0	100
r47	1.0	100
r48	1.0	100
r49	1.0	100
r50	1.0	100
r51	1.0	100
r52	1.0	100
r53	1.5	150
r54	1.5	150
r55	1.5	150
r56	2.0	200
r57	2.0	200
r58	2.5	250
r59	2.5	250
r60	3.0	300
r61	5.0	500
r62	8.0	800

Caution There is no connection between V4 and V5 terminal in the IC.

Figure 5-3. Relationship between Input Data and Output Voltage (POL21, POL22 = L)

Output Voltage 1: $V_{DD2} - 0.2 V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5 V_{DD2}$

Output Voltage 2: $0.5 V_{DD2} - 0.3 V \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.2 V$

Input Data	Output Voltage 1			Output Voltage 2		
00H	V_0	V_0		V_0	V_9	
01H	V_1	$V_1+(V_0-V_1) \times$	7250 / 8050	V_1	$V_9+(V_8-V_9) \times$	800 / 8050
02H	V_2	$V_1+(V_0-V_1) \times$	6500 / 8050	V_2	$V_9+(V_8-V_9) \times$	1550 / 8050
03H	V_3	$V_1+(V_0-V_1) \times$	5800 / 8050	V_3	$V_9+(V_8-V_9) \times$	2250 / 8050
04H	V_4	$V_1+(V_0-V_1) \times$	5150 / 8050	V_4	$V_9+(V_8-V_9) \times$	2900 / 8050
05H	V_5	$V_1+(V_0-V_1) \times$	4550 / 8050	V_5	$V_9+(V_8-V_9) \times$	3500 / 8050
06H	V_6	$V_1+(V_0-V_1) \times$	4000 / 8050	V_6	$V_9+(V_8-V_9) \times$	4050 / 8050
07H	V_7	$V_1+(V_0-V_1) \times$	3450 / 8050	V_7	$V_9+(V_8-V_9) \times$	4600 / 8050
08H	V_8	$V_1+(V_0-V_1) \times$	2950 / 8050	V_8	$V_9+(V_8-V_9) \times$	5100 / 8050
09H	V_9	$V_1+(V_0-V_1) \times$	2450 / 8050	V_9	$V_9+(V_8-V_9) \times$	5600 / 8050
0AH	V_{10}	$V_1+(V_0-V_1) \times$	2050 / 8050	V_{10}	$V_9+(V_8-V_9) \times$	6000 / 8050
0BH	V_{11}	$V_1+(V_0-V_1) \times$	1650 / 8050	V_{11}	$V_9+(V_8-V_9) \times$	6400 / 8050
0CH	V_{12}	$V_1+(V_0-V_1) \times$	1300 / 8050	V_{12}	$V_9+(V_8-V_9) \times$	6750 / 8050
0DH	V_{13}	$V_1+(V_0-V_1) \times$	950 / 8050	V_{13}	$V_9+(V_8-V_9) \times$	7100 / 8050
0EH	V_{14}	$V_1+(V_0-V_1) \times$	600 / 8050	V_{14}	$V_9+(V_8-V_9) \times$	7450 / 8050
0FH	V_{15}	$V_1+(V_0-V_1) \times$	300 / 8050	V_{15}	$V_9+(V_8-V_9) \times$	7750 / 8050
10H	V_{16}	V_1		V_{16}	V_8	
11H	V_{17}	$V_2+(V_1-V_2) \times$	2450 / 2750	V_{17}	$V_8+(V_7-V_8) \times$	300 / 2750
12H	V_{18}	$V_2+(V_1-V_2) \times$	2200 / 2750	V_{18}	$V_8+(V_7-V_8) \times$	550 / 2750
13H	V_{19}	$V_2+(V_1-V_2) \times$	1950 / 2750	V_{19}	$V_8+(V_7-V_8) \times$	800 / 2750
14H	V_{20}	$V_2+(V_1-V_2) \times$	1700 / 2750	V_{20}	$V_8+(V_7-V_8) \times$	1050 / 2750
15H	V_{21}	$V_2+(V_1-V_2) \times$	1500 / 2750	V_{21}	$V_8+(V_7-V_8) \times$	1250 / 2750
16H	V_{22}	$V_2+(V_1-V_2) \times$	1300 / 2750	V_{22}	$V_8+(V_7-V_8) \times$	1450 / 2750
17H	V_{23}	$V_2+(V_1-V_2) \times$	1100 / 2750	V_{23}	$V_8+(V_7-V_8) \times$	1650 / 2750
18H	V_{24}	$V_2+(V_1-V_2) \times$	950 / 2750	V_{24}	$V_8+(V_7-V_8) \times$	1800 / 2750
19H	V_{25}	$V_2+(V_1-V_2) \times$	800 / 2750	V_{25}	$V_8+(V_7-V_8) \times$	1950 / 2750
1AH	V_{26}	$V_2+(V_1-V_2) \times$	650 / 2750	V_{26}	$V_8+(V_7-V_8) \times$	2100 / 2750
1BH	V_{27}	$V_2+(V_1-V_2) \times$	500 / 2750	V_{27}	$V_8+(V_7-V_8) \times$	2250 / 2750
1CH	V_{28}	$V_2+(V_1-V_2) \times$	400 / 2750	V_{28}	$V_8+(V_7-V_8) \times$	2350 / 2750
1DH	V_{29}	$V_2+(V_1-V_2) \times$	300 / 2750	V_{29}	$V_8+(V_7-V_8) \times$	2450 / 2750
1EH	V_{30}	$V_2+(V_1-V_2) \times$	200 / 2750	V_{30}	$V_8+(V_7-V_8) \times$	2550 / 2750
1FH	V_{31}	$V_2+(V_1-V_2) \times$	100 / 2750	V_{31}	$V_8+(V_7-V_8) \times$	2650 / 2750
20H	V_{32}	V_2		V_{32}	V_7	
21H	V_{33}	$V_3+(V_2-V_3) \times$	1500 / 1600	V_{33}	$V_7+(V_6-V_7) \times$	100 / 1600
22H	V_{34}	$V_3+(V_2-V_3) \times$	1400 / 1600	V_{34}	$V_7+(V_6-V_7) \times$	200 / 1600
23H	V_{35}	$V_3+(V_2-V_3) \times$	1300 / 1600	V_{35}	$V_7+(V_6-V_7) \times$	300 / 1600
24H	V_{36}	$V_3+(V_2-V_3) \times$	1200 / 1600	V_{36}	$V_7+(V_6-V_7) \times$	400 / 1600
25H	V_{37}	$V_3+(V_2-V_3) \times$	1100 / 1600	V_{37}	$V_7+(V_6-V_7) \times$	500 / 1600
26H	V_{38}	$V_3+(V_2-V_3) \times$	1000 / 1600	V_{38}	$V_7+(V_6-V_7) \times$	600 / 1600
27H	V_{39}	$V_3+(V_2-V_3) \times$	900 / 1600	V_{39}	$V_7+(V_6-V_7) \times$	700 / 1600
28H	V_{40}	$V_3+(V_2-V_3) \times$	800 / 1600	V_{40}	$V_7+(V_6-V_7) \times$	800 / 1600
29H	V_{41}	$V_3+(V_2-V_3) \times$	700 / 1600	V_{41}	$V_7+(V_6-V_7) \times$	900 / 1600
2AH	V_{42}	$V_3+(V_2-V_3) \times$	600 / 1600	V_{42}	$V_7+(V_6-V_7) \times$	1000 / 1600
2BH	V_{43}	$V_3+(V_2-V_3) \times$	500 / 1600	V_{43}	$V_7+(V_6-V_7) \times$	1100 / 1600
2CH	V_{44}	$V_3+(V_2-V_3) \times$	400 / 1600	V_{44}	$V_7+(V_6-V_7) \times$	1200 / 1600
2DH	V_{45}	$V_3+(V_2-V_3) \times$	300 / 1600	V_{45}	$V_7+(V_6-V_7) \times$	1300 / 1600
2EH	V_{46}	$V_3+(V_2-V_3) \times$	200 / 1600	V_{46}	$V_7+(V_6-V_7) \times$	1400 / 1600
2FH	V_{47}	$V_3+(V_2-V_3) \times$	100 / 1600	V_{47}	$V_7+(V_6-V_7) \times$	1500 / 1600
30H	V_{48}	V_3		V_{48}	V_6	
31H	V_{49}	$V_4+(V_3-V_4) \times$	3350 / 3450	V_{49}	$V_6+(V_5-V_6) \times$	100 / 3450
32H	V_{50}	$V_4+(V_3-V_4) \times$	3250 / 3450	V_{50}	$V_6+(V_5-V_6) \times$	200 / 3450
33H	V_{51}	$V_4+(V_3-V_4) \times$	3150 / 3450	V_{51}	$V_6+(V_5-V_6) \times$	300 / 3450
34H	V_{52}	$V_4+(V_3-V_4) \times$	3050 / 3450	V_{52}	$V_6+(V_5-V_6) \times$	400 / 3450
35H	V_{53}	$V_4+(V_3-V_4) \times$	2950 / 3450	V_{53}	$V_6+(V_5-V_6) \times$	500 / 3450
36H	V_{54}	$V_4+(V_3-V_4) \times$	2800 / 3450	V_{54}	$V_6+(V_5-V_6) \times$	650 / 3450
37H	V_{55}	$V_4+(V_3-V_4) \times$	2650 / 3450	V_{55}	$V_6+(V_5-V_6) \times$	800 / 3450
38H	V_{56}	$V_4+(V_3-V_4) \times$	2500 / 3450	V_{56}	$V_6+(V_5-V_6) \times$	950 / 3450
39H	V_{57}	$V_4+(V_3-V_4) \times$	2300 / 3450	V_{57}	$V_6+(V_5-V_6) \times$	1150 / 3450
3AH	V_{58}	$V_4+(V_3-V_4) \times$	2100 / 3450	V_{58}	$V_6+(V_5-V_6) \times$	1350 / 3450
3BH	V_{59}	$V_4+(V_3-V_4) \times$	1850 / 3450	V_{59}	$V_6+(V_5-V_6) \times$	1600 / 3450
3CH	V_{60}	$V_4+(V_3-V_4) \times$	1600 / 3450	V_{60}	$V_6+(V_5-V_6) \times$	1850 / 3450
3DH	V_{61}	$V_4+(V_3-V_4) \times$	1300 / 3450	V_{61}	$V_6+(V_5-V_6) \times$	2150 / 3450
3EH	V_{62}	$V_4+(V_3-V_4) \times$	800 / 3450	V_{62}	$V_6+(V_5-V_6) \times$	2650 / 3450
3FH	V_{63}	V_4		V_{63}	V_5	

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₅₂₇	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

(2) R,/L = L (Left shift)

Output	S ₁	S ₂	S ₃	S ₄	...	S ₅₂₇	S ₃₈₄
Data	D ₀₀ to D ₀₅	D ₁₀ to D ₁₅	D ₂₀ to D ₂₅	D ₃₀ to D ₃₅	...	D ₄₀ to D ₄₅	D ₅₀ to D ₅₅

POL	S _{2n-1} Note	S _{2n} Note
L	V ₀ to V ₄	V ₅ to V ₉
H	V ₅ to V ₉	V ₀ to V ₄

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB CLK AND OUTPUT WAVEFORM

Figure 7-1. Input Circuit Block Diagram

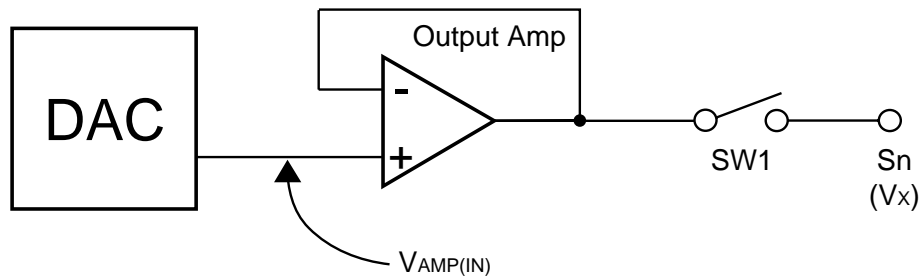
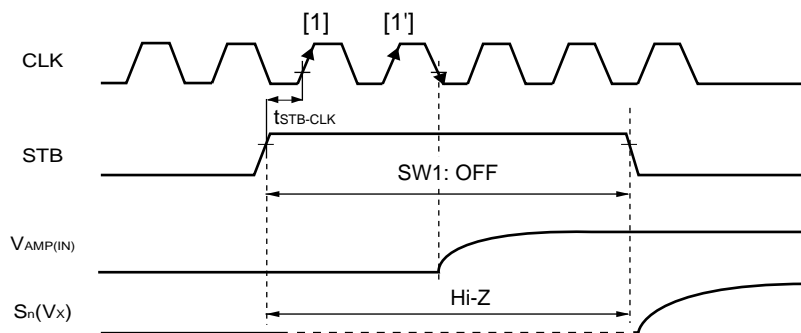


Figure 7-2. Output Circuit Timing Waveform

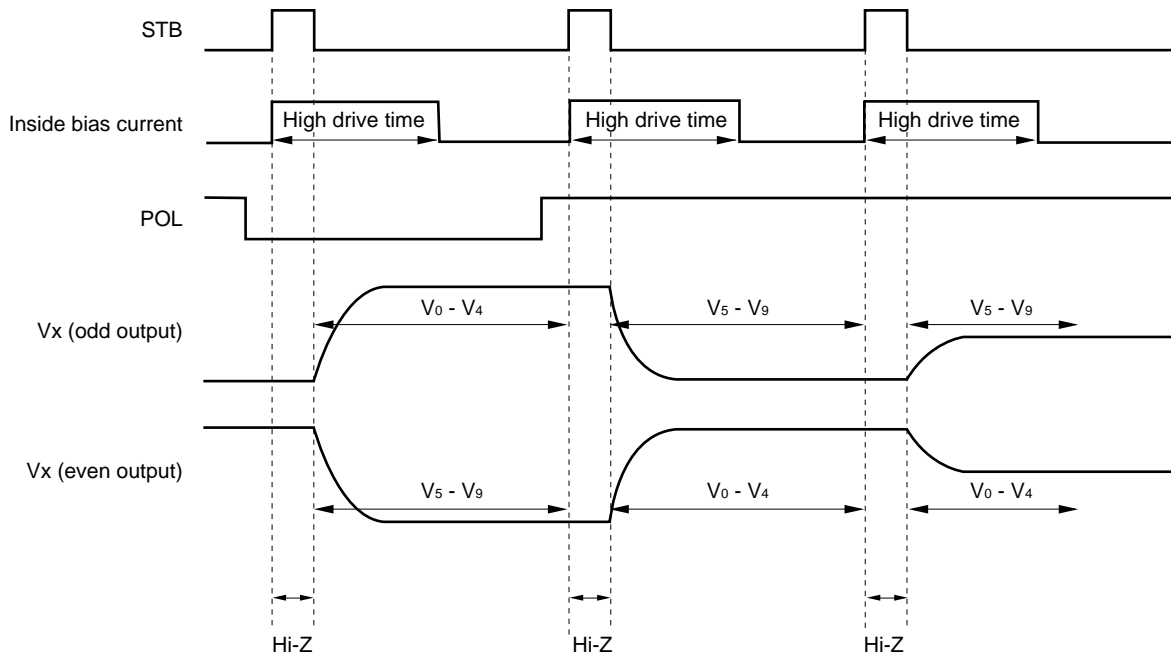


STB = H is loaded with the rising edge of CLK[1]. However, when not satisfying the specification of $t_{STB-CLK}$, STB = H is loaded with the rising edge of the next CLK[1']. Latch operation of display data is completed with the falling edge of the next CLK which loaded STB = H. Therefore, in order to complete latch operation of display data, it is necessary to input at least 2 CLK in STB = H period.

8. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

When the STB is high level, all outputs became Hi-Z and the gray-scale voltage is output to the LCD in synchronization with the falling edge of STB.

Therefore, high drive time of the output amplifier as below is determined by the CLK number of the required SRC pin setting. Be sure to avoid using such as extremely changing the CLK frequency (ex. CLK stop).

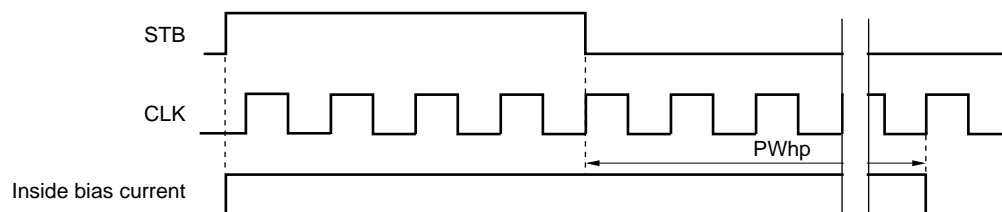


9. SRC AND HIGH DRIVE TIME

The μPD160061 can control high drive time of the output amplifier by SRC pin logic (refer to below figure).

SRC = H or open (high drive time: standard mode): High drive time (PW_{hp}) of the output amplifier is in 64 CLK period from falling edge of the STB.

SRC = L (high drive time: long-term mode): High drive time (PW_{hp}) of the output amplifier is in 128 CLK period from falling edge of the STB.



We recommend a thorough simulation of the output amplifier in advance when set the SRC pin.

10. BIAS CURRENT CONTROL BY LPC AND HPC

The μPD160061 can control the bias current of the output amplifier in high drive period and low drive period.

Bias Current	LPC	HPC
High	H	L
Middle	H or open	L
Normal	L or open	H or open
Low	H	H or open

Panel Load
Heavy
↑ ↓
Light

We recommend a thorough simulation of the output amplifier in advance, when set the LPC and HPC pins.

Refer to the table below for the example of the combination of setting level and panel load, with driver part supply voltage.

	Example of Condition	LPC	HPC	SRC
Example 1	Load: $R_L = 5\text{ k}\Omega$, $C_L = 75\text{ pF}$ Driver part supply voltage: $V_{DD2} = 7.5\text{ V}$	L or open	L	H or open
		Bias current mode: Middle		
Example 2	Load: $R_L = 5\text{ k}\Omega$, $C_L = 75\text{ pF}$ Driver part supply voltage: $V_{DD2} = 9.0\text{ V}$	L or open	H or open	H or open
		Bias current mode: Normal		
Example 3	Load: $R_L = 40\text{ k}\Omega$, $C_L = 80\text{ pF}$ Driver part supply voltage: $V_{DD2} = 9.0\text{ V}$	H	L	L
		Bias current mode: High		

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V _{DD1}	-0.5 to +4.0	V
Driver Part Supply Voltage	V _{DD2}	-0.5 to +10.0	V
Logic Part Input Voltage	V _{I1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Input Voltage	V _{I2}	-0.5 to V _{DD2} + 0.5	V
Logic Part Output Voltage	V _{O1}	-0.5 to V _{DD1} + 0.5	V
Driver Part Output Voltage	V _{O2}	-0.5 to V _{DD2} + 0.5	V
Operating Ambient Temperature	T _A	-10 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V _{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V _{DD2}		7.5	8.5	9.5	V
High-Level Input Voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low-Level Input Voltage	V _{IL}		0		0.3 V _{DD1}	V
γ-Corrected Voltage	V ₀ to V ₄ V ₅ to V ₉	7.5 V ≤ V _{DD1} ≤ 9.5 V	0.5 V _{DD2}		V _{DD2} - 0.2	V
		7.5 V ≤ V _{DD1} < 8.5 V	0.2		0.5 V _{DD2} - 0.3	V
		8.5 V ≤ V _{DD1} ≤ 9.5 V	0.2		0.5 V _{DD2}	V
Driver Part Output Voltage	V _O		0.2		V _{DD2} - 0.2	V
Clock Frequency	f _{CLK}	2.3 V ≤ V _{DD1} < 2.7 V			40	MHz
		2.7 V ≤ V _{DD1} ≤ 3.6 V			65	MHz

Electrical Characteristics (T_A = -10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 7.5 to 9.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Input Leak Current	I _{IL}	Except LPC, HPC, SRC			±1.0	μA
		LPC, HPC, SRC	T.B.D.		T.B.D.	μA
High-Level Output Voltage	V _{OH}	STHR (STHL), I _{OH} = 0 mA	V _{DD1} - 0.1			V
Low-Level Output Voltage	V _{OL}	STHR (STHL), I _{OL} = 0 mA			0.1	V
γ-Corrected Resistance	R _γ	V ₀ to V ₄ = V ₅ to V ₉ = 4.0 V, V _{DD2} = 8.5 V	T.B.D.	15.8	T.B.D.	kΩ
Driver Output Current	I _{VOH}	V _{DD2} = 8.0 V, V _X = 7.0 V, V _{OUT} = 6.5 V ^{Note1}			T.B.D.	μA
	I _{VOL}	V _{DD2} = 8.0 V, V _X = 1.0 V, V _{OUT} = 1.5 V ^{Note1}	T.B.D.			μA
Output Voltage Deviation	ΔV _O	T _A = 25°C,		±7	±20	mV
Output Swing Difference Deviation	ΔV _{P-P}	V _{DD1} = 3.3 V, V _{DD2} = 8.5 V, V _{OUT} = 2.0 V, 4.25 V, 6.5 V		±2	±15	mV
Logic Part Dynamic Current Consumption ^{Note2, 3, 4}	I _{DD1}	V _{DD1}	T.B.D.		T.B.D.	mA
Driver Part Dynamic Current Consumption ^{Note2, 4}	I _{DD22}	V _{DD2} , with no load	T.B.D.		T.B.D.	mA

Remark T.B.D. (To be determined.)

Notes1. V_X refers to the output voltage of analog output pins S₁ to S₃₈₄. V_{OUT} refers to the voltage applied to analog output pins S₁ to S₃₈₄.

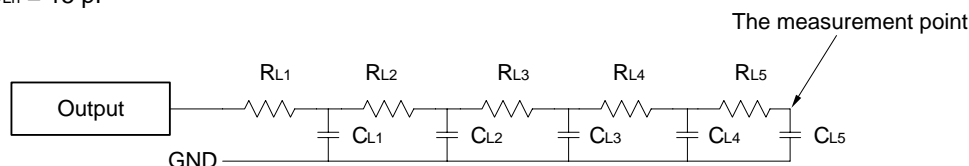
2. Specified at f_{STB} = 65 kHz and f_{CLK} = 54 MHz.
3. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
4. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = -10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 7.5 to 9.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t _{PLH1}	C _L = 15 pF, 2.3 V ≤ V _{DD1} < 2.7 V			20	ns
		C _L = 10 pF, 2.7 V ≤ V _{DD1} ≤ 3.6 V			10.5	ns
	t _{PLH1}	C _L = 10 pF, 2.3 V ≤ V _{DD1} < 2.7 V			20	ns
		C _L = 10 pF, 2.7 V ≤ V _{DD1} ≤ 3.6 V			10.5	ns
Driver Output Delay Time	t _{PLH2}	C _L = 75 pF, R _L = 5 kΩ,			5	μs
	t _{PLH3}	LPC = H or open,			8	μs
	t _{PHL2}	HPC = H or open,			5	μs
	t _{PHL3}	SRC = H or open			8	μs
Input Capacitance	C _{i1}	Logic input of exclude STHR (STHL), T _A = 25°C			10	pF
	C _{i2}	STHR (STHL), T _A = 25°C			5	pF

<Measurement condition>

R_{L1} = 1 kΩ, C_{L1} = 15 pF



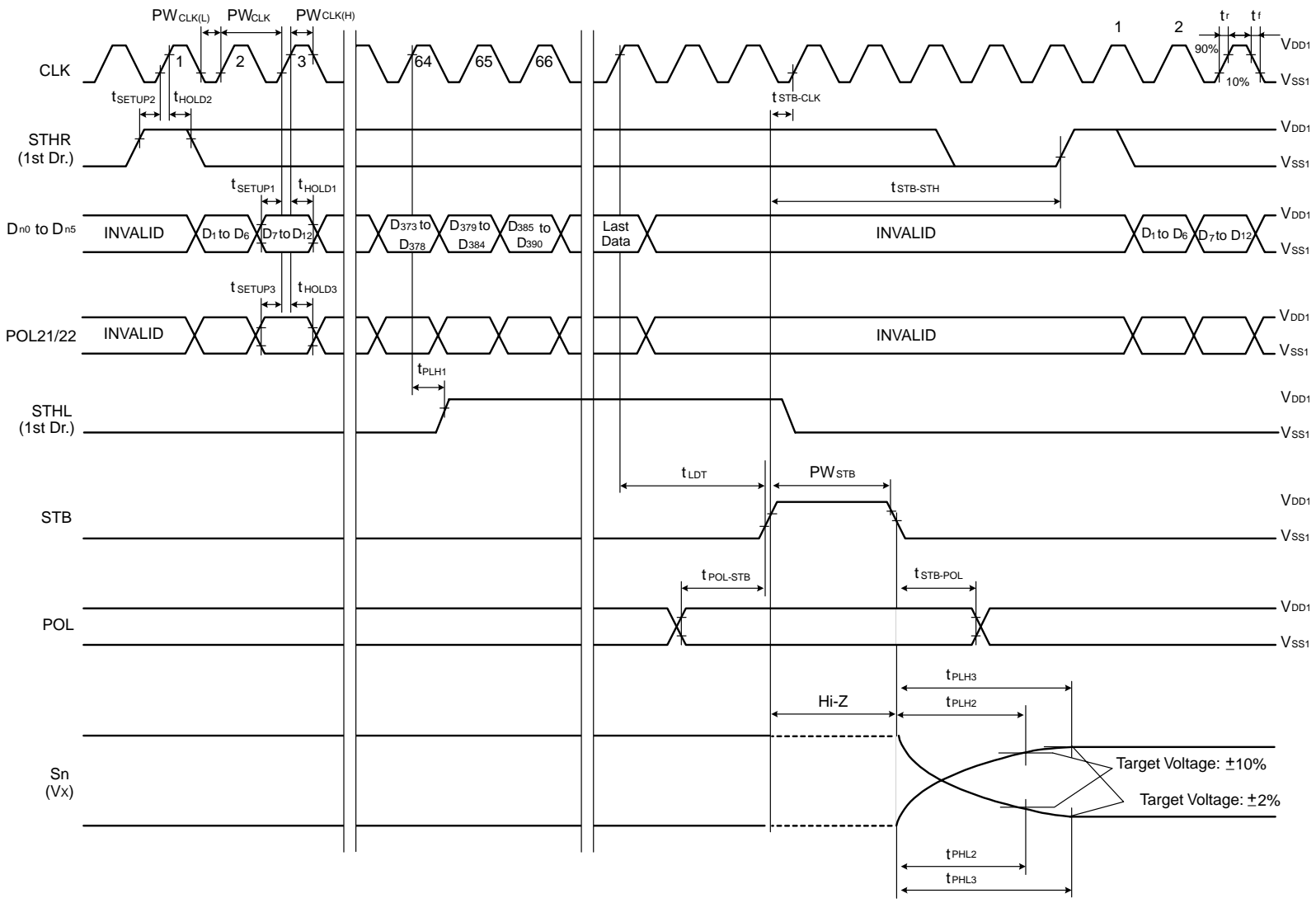
Timing Requirements ($T_A = -10$ to $+75^\circ\text{C}$, $V_{DD1} = 2.3$ to 3.6 V, $V_{SS1} = 0$ V, $t_r = t_f = 5.0$ ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW _{CLK}	$2.3\text{ V} \leq V_{DD1} < 2.7\text{ V}$	25			ns
		$2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$	15			ns
Clock Pulse High Period	PW _{CLK(H)}	$2.3\text{ V} \leq V_{DD1} < 2.7\text{ V}$	6			ns
		$2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$	4			ns
Clock Pulse Low Period	PW _{CLK(L)}	$2.3\text{ V} \leq V_{DD1} < 2.7\text{ V}$	6			ns
		$2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$	4			ns
Data Setup Time	t _{SETUP1}		4			ns
Data Hold Time	t _{HOLD1}		0			ns
Start Pulse Setup Time	t _{SETUP2}		4			ns
Start Pulse Hold Time	t _{HOLD2}		0			ns
POL21, POL22 Setup Time	t _{SETUP3}		4			ns
POL21, POL22 Hold Time	t _{HOLD3}		0			ns
STB Pulse Width	PW _{STB}		2			CLK
Last Data Timing	t _{LDT}		2			CLK
STB-CLK Time	t _{STB-CLK}	STB \uparrow \rightarrow CLK \uparrow	9			ns
Time Between STB and Start Pulse	t _{STB-STH}	STB \uparrow \rightarrow STHR(STHL) \uparrow	2			CLK
POL-STB Time	t _{POL-STB}	POL \uparrow or \downarrow \rightarrow STB \uparrow	-5			ns
STB-POL Time	t _{STB-POL}	STB \downarrow \rightarrow POL \downarrow or \uparrow	6			ns

Remark Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.

★ SWITCHING CHARACTERISTICS WAVEFORM (R./L= H)

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7 V_{DD1}$, $V_{IL} = 0.3 V_{DD1}$.



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades On NEC Semiconductor Devices (C11531E)**

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