This product is not released and the specifications herein are subject to change

AMCC®

SONET/SDH/ATM OC-48 8:1 TRANSMITTER S3041

FEATURES

- Micro-power Bipolar technology
- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports 2.4 GHz (OC-48)
- Reference frequency of 155.52 MHz
- Interface to both PECL and TTL logic
- 8-bit PECL data path
- Compact 64 PQFP package
- Diagnostic loopback mode
- Line loopback
- Lock detect
- Low jitter PECL interface
- Single 3.3V supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexors
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3041 SONET/SDH Mux chip is a fully integrated serialization SONET OC-48 (2.4 GHz) interface device. The chip performs all necessary parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

On-chip clock synthesis PLL components are contained in the S3041 Mux chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3041 is packaged in a 64 PQFP, offering designers a small package outline.

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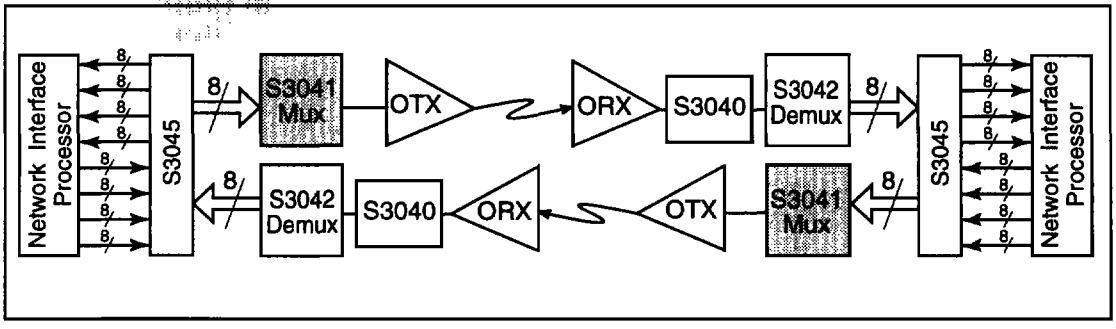
Figure 1. System Block Diagram



S3041 OVERVIEW

The S3041 Mux implements SONET/SDH serialization and transmission functions. The block diagram in Figure 2 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial conversion and system timing. The system timing circuitry consists of a high-speed phase detector, clock dividers, and clock distribution throughout the front end.

The sequence of operations is as follows:

Transmitter Operations:

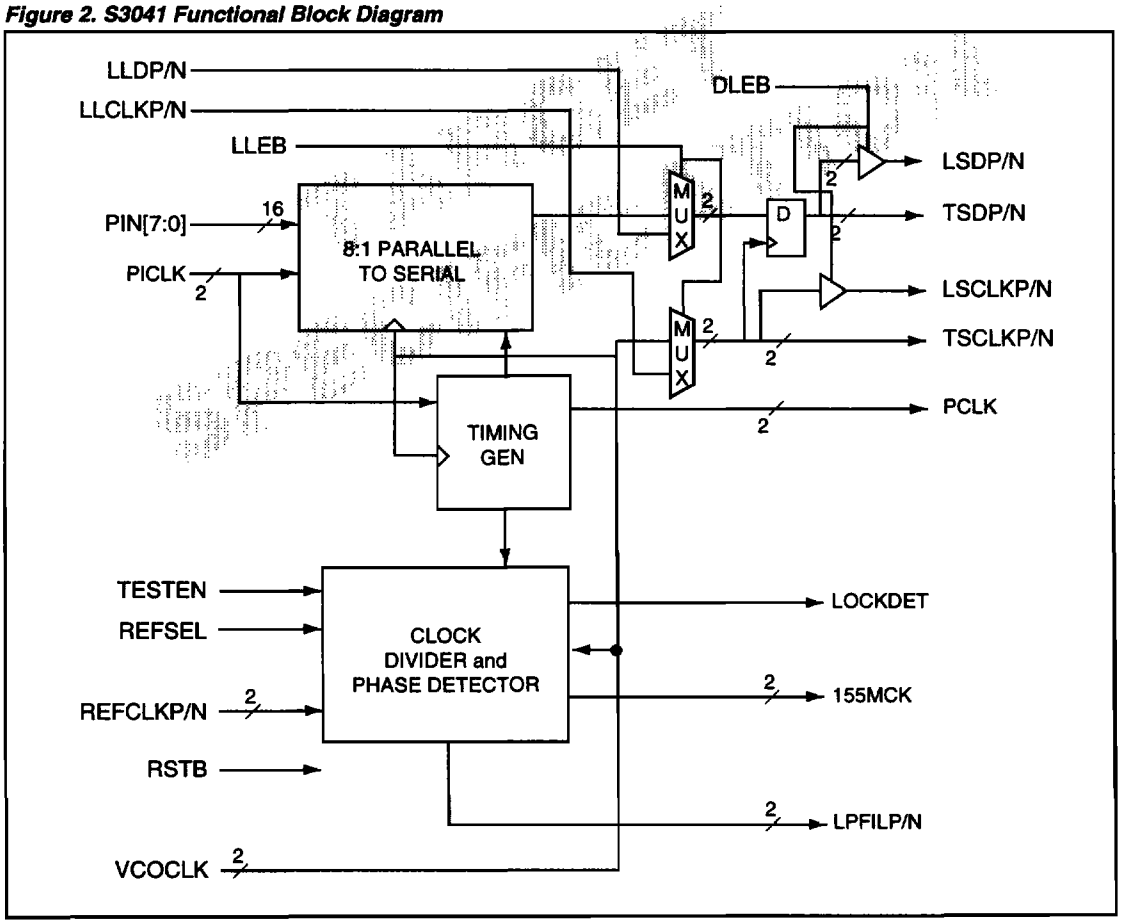
1. 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Internal clocking and control functions are transparent to the user.

Suggested Interface Devices

AMCC	S3040	OC-48 Clock Recovery Device
AMCC	S3045	OC-48 to OC-12 Demux
AMCC	S3042	OC-48 Demux

Figure 2. S3041 Functional Block Diagram



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