Gould AMI was the first company to recognize the need for custom integrated circuits in the mid-1960's, and to pioneer the development of application-specific integrated circuits (ASICs). With more than twenty years' dedication to providing ASIC system solutions, Gould AMI has more experience than any other vendor of ASICs.

The company now offers a continuum of ASIC products, ranging from CMOS programmable logic devices to complex cell-based custom ICs. This spectrum of offerings provides customers with a full range of ASIC choices, so that the optimum solution for an application can be selected.

Gould AMI's ASIC technology allows system designers to tailor their systems and reduce the number of parts in their products by combining multiple memory and processing functions on a single device, instead of mixing and matching several standard parts. The result: smaller board sizes, lower final product cost and higher reliability. ASIC users also benefit by greater product differentiation due to custom tailoring and higher security ensured by an ASIC's resistance to duplication.

CMOS EEPLDs

User-programmable digital devices ideal for small and medium-scale integration

Electrically erasable programmable logic devices are ideal for small and medium-scale integration system design in low-volume production. Our lowest development cost ASICs, these devices deliver plenty of performance and offer a surprising measure of versatility and customer-control.

Built using our unique PEEL™ (Programmable Electrically Erasable Logic) technology, these PLDs are user-programmable, so there's no pre-production customer design and development risk. You may use PC-based or industry-standard PLD programmers to configure the macrocells and, if necessary, to repeatedly erase and reconfigure them.

The table below can help you select the right PLD for you. See the PLD section later in this catalog for detailed data sheets.

For a low-cost, low-risk avenue for conversions of EEPLDs to gate arrays, see PALTRANs Flow in ASIC Software Services section.

Gould AMI's CMOS PLD Family

Part No.	Architecture	Complexity	Speed	Replaces
18CV8	20 pin E²PLD	74 product terms x 36 input array	10/15/25ns Tpd	Bipolar PLDs
20CG10	24 pin E²PLD	92 product terms x 44 input arrays	15/25ns Tpd	20V8, 20G10
22CV10Z	24 pin E²PLD	132 product terms x 44 inputs	15/25ns Tpd	Bipolar PLDs Zero power mode
22CV10	24 pin E²PLD	132 product terms x 44 inputs	15/25ns Tpd	Bipolar PLDs
PEEL153	20 pin E²PLD	42 product terms x 36 inputs 10 sum terms x 32 product terms	30ns Tpd	Bipolar PLS153
PEEL173	24 pin E²PLD	42 product terms x 44 inputs 10 sum terms x 32 product terms	15/30ns Tpd	Bipolar PLS173
PEEL253	20 pin E²PLD	42 product terms x 36 inputs 20 sum terms x 42 product terms	30ns Tpd	Bipolar PLS153 PEEL153
PEEL273	24 pin E²PLD	42 product terms x 44 inputs 20 sum terms x 42 product terms	15/30ns Tpd	Bipolar PLS173 PEEL173
PA7024	24 pin E²PMD	Over 80 sum of product terms	13/20ns Tpd	MULTI-PLDs
PA7040	40 pin E²PMD	Over 120 sum of product terms	13/20ns Tpd	MULTI-PLDs

Gate Arrays

Semi-finished digital chips provide high performance for medium volume production with quick development

- 1-micron triple or double metal and 1.25-micron double metal CMOS processes.
- Basic Logic, interface, MSI, and 7400 functions.
- Compatible with Gould AMI's megacell library.
- Custom RAMs available in both 1-micron and 1.25-micron processes.
- Artificial Intelligence Software Services available for netlist translation, gate reduction, clock-tree insertion, netlist analysis, and NETSCAN technology.

Gate arrays provide solutions for a variety of high performance digital applications--at a low development cost and quick design time. If you need fast turn production runs, gate arrays may be the right ASIC for you.

Gate arrays are semi-finished digital circuits that contain patterns of uncommitted transistors pre-fabricated on silicon base wafers. Using any major CAE workstation at your own facility, you can use Gould AMI libraries to customize your design as a network of logic functions. NETRANS is also available for conversion of any ASIC supplier's netlist to Gould AMI's bolt netlist format. With only the metal layers to fabricate, gate array development time is fast—typically four weeks.

Gould AMI's arrays are fabricated in a double (or triple) metal, single poly, twin-tub CMOS process. They offer the CMOS advantages of low power dissipation, broad power supply voltage range (2.5 to 5.5 Volts), and high noise immunity.

Over 600 macros in the process families include:

Basic functions: Sequential and combinational logic.

Interface functions: TTL and CMOS level inputs, TTL and CMOS Schmitt trigger inputs, pull-ups and pull-downs, TTL and CMOS output drivers, and output drivers with a controlled slew rate for lower noise operation.

MSI functions: Counters, multiplexers, decoders, adders.

7400 functions: Over 160 TTL compatible functions.

Digital megacells: Megacells and compilers include 82xx, 29xx, core processors, RAM, FIFOs, DSP megacells, and many more.

1-micron Gate Arrays

Array	Useable Gates		Programmable Pads		Power Pins
	Triple-metal	Double-metal	TAB	Wire-bond	
GD200K	150,000	100,000	492	360	12
GD100K	75,000	50,000	348	252	12
GD 70K	49,000	35,000	288	208	12
GD 50K	35,000	25,000	256	184	12
GD 35K	24,500	17,500	208	152	12
GD 25K	17,500	12,500	180	128	12
GD 20K	14,000	10,000	156	112	12
GD 16K	11,200	8,000	140	100	12
GD 12K	8,400	6,000	120	84	12
GD 9K	6,300	4,500	100	72	12
GD 7K	4,900	3,500	92	64	12
GD 5K	3,500	2,500	76	52	12
GD 3K	2,100	1,500	56	40	12

1.25-micron Gate Arrays

Array	Useable Gates	Programmable			Power Pins
		TAB	Fine Pitch	Standard Pitch	
GC100K	51,320	436	330	260	12
GC 50K	26,266	312	232	184	12
GC 40K	17,496	260	194	154	12
GC 30K	16,280	246	182	142	12
GC 25K	13,122	220	166	134	12
GC 20K	10,714	196	144	116	12
GC 15K	7,560	168	128	100	12
GC 10K	5,264	136	104	84	12
GC 7K	3,526	116	86	68	12
GC 5K	2,692	98	72	56	12
GC 3K	1,286	72	52	40	12

Standard Cell Circuits

Analog and digital building blocks offer higher density and smaller size for medium to high volume needs

- 1.0 and 1.25-micron Double Metal CMOS Families.
- 3-micron and 2-micron Double Poly, Double Metal CMOS Families
- Cells Created by Expert-based Cell Generator
- Basic Logic, Interface, MSI, 7400 and Megacell Functions
- 2-micron Process includes Analog Functions
- Tailor-made RAMs, ROMs and PLAs Available
- Artificial Intelligence Software Services Available for Digital Netlist Translation and Gate Reduction

Chips designed with these cells, offered in analog and digital formats, surpass gate array density and approach that of cell-based custom designs at half the development cost and development time. They're cost effective for medium to high-volume production.

Standard cells are pre-designed circuit building blocks whose functional, timing and performance parameters exist in Gould AMI's libraries. As with a gate array, you design a standard cell circuit by choosing logic functions from a library installed on a CAE workstation. But while a gate array design specifies only the final metal layers of a pre-fabricated silicon base, all of a standard cell's base and metal layers are custom fabricated from pre-characterized cells. This feature gives standard cells greater design flexibility, but requires an eight week development time.

A standard cell circuit also uses only the number of cells required for a design, whereas gate arrays seldom utilize all of the available cells. This means a smaller die size and lower cost to you for a given circuit function.

Gould AMI offers over 850 cells in its four standard cell families:

- 1.0-micron digital CMOS (CYX Family).
- 1.25-micron digital CMOS (CAB Family).
- 3-micron analog and digital CMOS (CCI Family).
- 2-micron analog and digital CMOS (ABX Family).

Digital Standard Cells

Both the CAB and CYX families use a double metal, single poly, twin tub CMOS process. They are intended primarily for 5 Volt operation but will operate down to 2.5 Volts.

Cells in these libraries include:

Basic functions:	simple gates, clock drivers, flip/flops. latches
Interface functions:	TTL, CMOS, Schmitt trigger, slew rate buffers, TTL with hysteresis
MSI functions:	counters, multiplexers, decoders, adders
7400 functions:	over 160 TTL compatible functions
Digital megacells:	barrel shifter, funnel shifter, RAM, ROM and PLA

Digital Megacell List

MG53C80	SCSI Interface Controller
MG80C85	8-Bit CMOS Microprocessor
MG82C12	8-Bit Input/Output Port
MG82C37A	Programmable DMA Controller
MC82C50A	Asynchronous Comm. Element
MG82C52	Serial Controller Interface
MG82C54	Programmable Interval Timer
MG82C55A	Programmable Peripheral Interface
MG82C59A	Programmable Interrupt Controller
MG82C84A	Clock Generator and Driver
MG82C88	Microprocessor Bus Controller
MG85C30	Serial Communications Controller
MGM1616A	16x16 Fast Multiplier
MGA1616A	16x16 Fast Adder/Subtractor

Analog/Digital Standard Cells

The CCI family uses a 3-micron double metal, double poly, p-well CMOS process. It is intended primarily for analog and/or digital applications running at 10 Volts analog with 5 Volts digital operation.

Gould AMI's new ABX process is a 2-micron double poly, double metal process. This is Gould AMI's most flexible process, built on N or P-type starting material, with a range of 13 to 17 process layers. Ideal for mixed signal analog and digital applications, it can operate from 5 to 12 volts. Functions include electrically erasable ROMs, implant programmable ROMs and NPN and PNP bipolar transistors on board.

Cells in the CCI and ABX libraries include:

Basic functions:	simple gates, clock drivers, flip/flops, latches
Interface functions:	TTL, CMOS, Schmitt trigger
MSI functions:	counters, multiplexers, decoders, adders
7400 functions:	over 160 TTL compatible functions
Analog functions:	Op amps, A/D, D/A, comparators, switches, voltage references, input buffer and output buffer

Cell-based Custom

Most tailored ASIC solution--best for high performance, mixed signal or high volume needs

Cell-based custom chips use a combination of Gould's megacells, custom cells and standard cells to provide you with the ultimate in design tailoring and performance. This approach is ideal when you have a requirement for high speed, special interfaces, mixed analog/digital, or very high volume production runs.

Though their development costs and time are longer than with standard cells, cell-based custom circuits pack the most functions into the smallest area. Fewer custom chips need be used in a given design, thus saving board space. Custom devices also provide greater security because they are nearly impossible to copy.

Over twenty years' experience in custom design have given Gould AMI's design team the kind of engineering expertise that complex solutions demand. Particular areas of expertise are analog, mixed signal, high voltage and E2 applications. The following illustrate some examples of Gould AMI's answers to our customers' technical challenges.

Case History #1

A consumer products manufacturer is developing an instrumentation device that measures pressure, room dimensions and weight. The technical challenge? To reduce the number of discrete logic parts and consolidate into one device, which requires analog and digital functions on a single ASIC.

Gould AMI's Solution: A cell-based custom chip which incorporates LCD drivers, a comparator, a/d converters, gain stages and voltage references on a single chip, thus making the measuring device perform more reliably and reducing the number of components required. This saves the customer money in component costs, as well as assembly and inventory costs.

Case History #2

Problem: An automotive company needs a drop-in replacement for a device that nearest fuel, oil and temperature and displays the results on a car dashboard. The technical challenge? This smart device needs to be fast and super-accurate, with numerous features on a single densely packed chip. The customer also requires fault coverage to be 99%.

Gould AMI's solution: To integrate analog and digital blocks on a single custom chip. The analog portion of the circuit allows sampling of a greater number of bits, thus resulting in a faster, more accurate display. The integrated solution enables Gould AMI to meet the size, power, speed and accuracy requirements so that the device will drop right in to the customer's board.

Silicon Foundry Approach

Gould AMI is proud of the leadership position it occupies in today's fast-paced world of process and technology. Our Silicon Foundry services and capabilities are truly world class. We provide consulting services to our customers in the design, fabrication, packaging and testing of state-of-the-art digital, analog, and mixed-signal integrated circuits. All AMI manufacturing is performed under one of the most highly advanced real-time SPC environments in the semiconductor industry today.

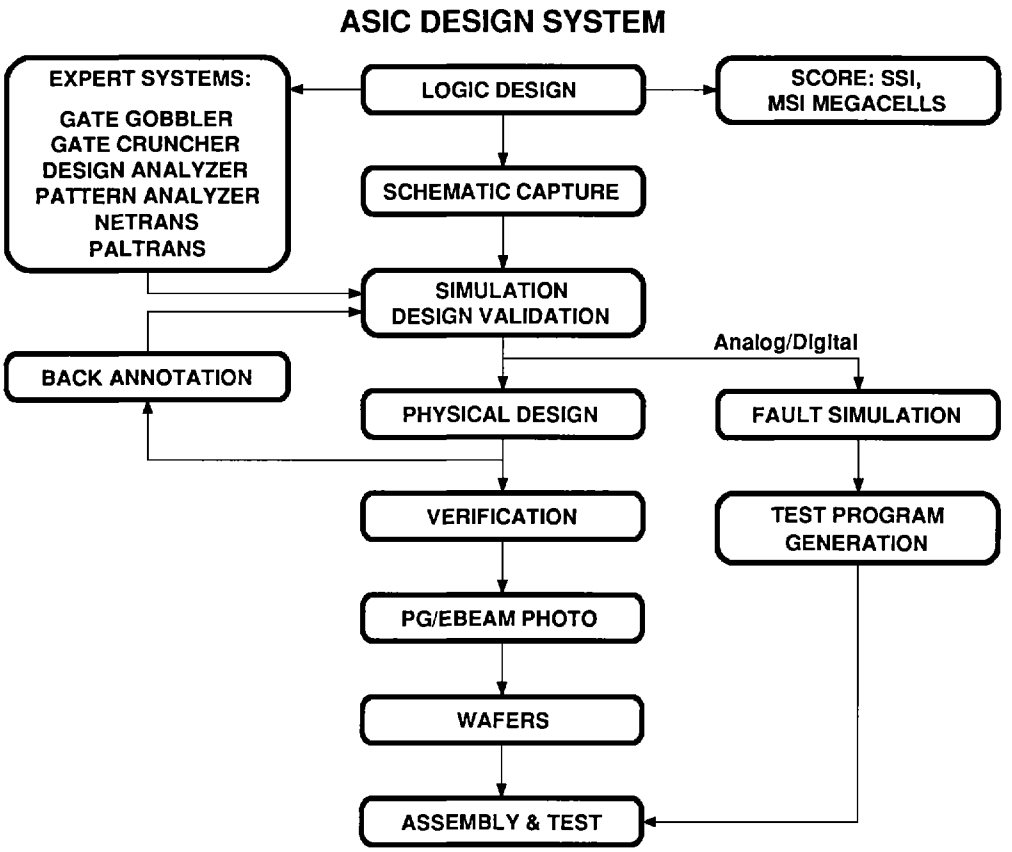
Gould AMI's approach to Silicon Foundry services is your road to success. Whether you are a highly sophisticated circuit designer with your own design resources and facilities, utilize outside third-party design resources, or are simply seeking a second source to manufacture your already existing circuit, Gould AMI can provide you with cost-effective and timely semiconductor solutions. Gould AMI is a complete VLSI integrated circuit manufacturing facility with the capability to help you develop, produce and deliver CMOS and NMOS circuits.

At Gould AMI you will receive the very best in service, product quality, and cost-effective manufacturing available in the industry today. It is as simple as providing Gould AMI with a data base tape of your circuit in standard GDSII format. Digital, analog, or mixed-signal designs can be made to match any of the wide variety of Gould AMI's CMOS processes presently in use or under development. Our company-wide drive for improvement encourages continuous advances in processing technology and development. With over two decades of experience in custom and semi-custom integrated circuit manufacturing, Gould AMI provides a highly flexible and responsive team capable of meeting the rapidly changing needs of our customers in a world class manufacturing environment.

GOULD AMI CMOS PROCESS FAMILY

Process Family	Geometry	Maximum Voltage	Characteristics
CMOS	1.0	5.5 Volts	Digital
CMOS	1.25	5.5 Volts	Digital
CMOS	1.5	5.0 to 12.0 Volts	Mixed Signal
CMOS	2.0	5.5 Volts	Digital
CMOS	3.0	5.0 to 10.0 Volts	Analog and Digital
CMOS	1.2	5.5 Volts	Digital
CMOS	5.0	5.5 to 12.0 Volts	Digital
CMOS	7.0	5.5 Volts	Analog and Digital
NMOS	3.0	5.5 Volts	Digital
NMOS	4.0	5.5 Volts	Digital
NMOS	5.0	5.5 Volts	Digital

Typical ASIC Development Flow



ASIC Software Services

Optional design services give you the power of choice and ease your designs

Unlike many ASIC vendors that accept only completed designs or finished netlists, Gould AMI is able to pick up an ASIC design at any stage, whether customers submit a partially finished design, a foundry-ready database tape, or a simple set of specifications. In order to ease logic design for its customers, Gould AMI has installed its analog and digital cell libraries on popular engineering workstations including Mentor Graphics, Daisy Systems, Intergraph, VALID Logic Systems, FutureNet and Viewlogic.

Gould AMI uses several advanced expert systems in-house, each of which taps the combined experience of Gould AMI's engineers to accelerate device layout and design optimization.

ASIC Netlist Translation Services:

If a client has already designed a digital chip using another vendor's or their own proprietary tools, Gould AMI's NETRANS™ expert system will "translate" the netlist into Gould AMI-compatible form in just a few hours. This automated design transfer works independently of workstation libraries or processes, and can save customers thousands of dollars and weeks of precious time. For turning programmable logic device into gate arrays or standard cells, PALTRANS™ is the answer. PALTRANS converts standard programmable array logic (PAL), programmable electrically erasable logic (PEEL) and field programmable gate arrays (FPGAs) into netlists used to design gate array or standard cell ASICs. You can use an off-the-shelf PLD as a prototype for programming, debugging, and beta-testing logic designs, instead of first requiring the production of an ASIC. Engineers then use PALTRANS to convert the data into a netlist. In about eight hours, mask production can begin and an ASIC design is produced in two to three weeks.

Tools Speed Layout and Optimization

The SCORE™ cell compiler generates and tailors cells to a client's specific requirements in one-tenth the time required for hand-built cells.

Gate Gobbler, Gate Cruncher, Design Analyzer and Pattern Analyzer are artificial intelligence (AI) tools that assist with the conversion of conventional standard devices to CMOS ASICs.

Gould AMI offers an Automatic Test Generation tool, NETSCAN, that generates test vectors in a matter of hours, relieving designers of the task and saving at least six weeks for manual test generation. This tool automatically partitions a circuit into a set of combinatorial functions and inserts a scan path. Each function, seen as a distinct circuit, can be quickly and easily tested with an automatic test program generator employing the D-Algorithm.

Transitioning from standard TTL parts to ASICs can be fraught with difficulty, and when ASIC prototypes don't work, design re-work through traditional analysis and optimization techniques can take weeks or months. Gould AMI's AI tools minimize the delays caused by having to re-work a design through traditional analysis and optimization techniques. The tools incorporate a continually expanding knowledge base, applying Gould AMI's hundreds of engineering man-years to every job.