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- **Central Arbitration Mechanism Is Fully Compliant to Futurebus+ Standard (IEEE Std 896.1–1991)**
- **Supports Up to 14 Modules**
- **Provides Fully Programmable Priority (0 to 255) for Each Module Interface for Optimal Real-Time Performance**
- **Contains a TFB2012 for Distributed Arbitration and Programming Central Arbitration for Use With Redundant Arbitration Methods**
- **Supports a Fairness Protocol Within Each Arbitration Priority Level**
- **Fully Supports Arbitrated Messages**
- **Fully Supports Preemption**
- **Timeout Registers Provided On Chip**
- **Provides a JTAG Test Port**

description

The TFB2011 Programmable Central-Bus Arbiter is a member of the Texas Instruments Futurebus+ chip set. This chip set provides an integrated approach to the Futurebus+ interface that reduces new-product design time, allows more functionality per circuit board, improves overall interface reliability, and reduces end-user down time through built-in test capabilities. The Futurebus+ chip set is capable of supporting, in any combination, 32- or 64-bit data widths on both the Hostbus interface and Futurebus+. The address width is programmable to be 32-bits or 36-bits (with either data width).

The TFB2011 contains the necessary functions to arbitrate between 1 to 14 requesting modules each having two programmable priority levels. Each priority can be assigned a value of between 0 and 255. It will grant the bus to the module that is the first to request the bus with the highest priority level. Performance is optimized for the special case of a single requestor. Preemption of lower-priority masters is fully supported.

The TFB2011 is designed to support three different scenarios. It can be a standalone central arbiter on the backplane or on a central-resources board in the system. It can also be used in place of the TFB2010 arbitration bus controller or other distributed arbiter on all boards, thus allowing any board in the system to be plugged into the central-bus arbiter slot. Alternatively, central arbitration can be wired to each board such that any board in any slot can perform the central arbiter function. This last approach requires special wiring of the backplane and BTL transceivers for the central arbitration signals.

Since the TFB2011 contains a complete TFB2010, it can be used as an arbitrated-message controller to program another central-bus arbiter, send asynchronous interrupts, or send event messages to other modules. In addition, in the case of a failure in the central-bus arbiter or if distributed arbitration is desired, it can be used as a distributed-arbitration controller without a change in the host software.

This device monitors the bus for arbitration messages, storing these in a four-message-deep FIFO or in the targeted interrupt register for reference by the processor. Messages may be sent by writing to the send arbitrated message (SAM) register.

Initialization, interrupt handling, and control of this device are handled through the CSR registers. All registers are memory mapped into the Futurebus+ CSR space and made accessible to a module-processing element through the CSR interface. The arbitration mode is initially determined from the state of the PE signal following a system reset. This device acts as the central arbiter for the system when the central arbiter enable bit is set in the configuration register and central arbitration is enabled in the common control register.

PRODUCT PREVIEW

NOTE: To maintain consistency with the notation used in the Futurebus+ standard (IEEE Std 896.1–1991), an active-low signal is denoted herein by use of the trailing asterisk (*) on the signal name.

description (continued)

Priority numbers are independently maintained for RQ<0> and RQ<1> for each of the 14 potential modules. They may be programmed to any number from 0 to 255. The priorities of these requests default to 0x00 and 0x80, respectively, when the device is powered up or reset. These numbers may be programmed with arbitrated messages or through writing the corresponding CSR. Priority numbers are also maintained for RQ<0> and RQ<1> in this module.

Fairness is independently maintained within two different priority levels (corresponding to the priorities of RQ<0> and RQ<1>) for each of the 14 modules when operating in central arbitration mode. Fairness is the mechanism that provides potentially equal bandwidth to all bus modules.

Timeout error checkers are provided for phases 1, 2, and 4 and for phase 0 between the first and second pass of a two-pass arbitration cycle. Phases 2 and 4 are hardwired to a timeout of 1 to 2 μs. Programmable wired-OR glitch filters are provided for the handshake lines and and the RE input.

Terminal Functions

CSR bus

NAME	PIN TYPE	FROM/TO	FUNCTION
CA<11:0>	I	CSR bus	CSR bus address
CD<7:0>	I/O	CSR bus	CSR bus data
CDP	I/O	CSR bus	CSR bus data odd parity
CCE*	I	CSR bus	CSR bus chip enable
COE*	I	CSR bus	CSR bus output enable
CWE*	I	CSR bus	CSR bus write enable

protocol controller interface

NAME	PIN TYPE	FROM/TO	FUNCTION
ARB_ERR<1:0>	O	Arbiter	Arbitration error: LL No error LH AC0 and AC1 asserted during phase 3 HL Arbitration comparison error HH Arbitration timeout error (phase 2 or 4)
GR	O		Futurebus+ mastership has been granted (bus tenure may begin). This signal remains in the high-impedance state while in the central-bus arbitration mode.
PE	O		Preempt. This signal is driven low to indicate that a module with a higher priority is requesting the bus. This signal remains in the high-impedance state while in the central-bus arbitration mode.
RQ<1:0>	I		Futurebus+ mastership is requested: RQ0 asserted: use arbitration number in registers 10H and 1H RQ1 asserted: use arbitration number in registers 12H and 13H Once a request is asserted, it shall not be released until GR* has been asserted. Once GR* is asserted, RQn* may be released at any time. Both request lines must be released prior to release of GR*. Another RQn* may be asserted after GR* has been released.

PRODUCT PREVIEW

Terminal Functions (continued)

other module interfaces

NAME	PIN TYPE	PIN FROM/TO	FUNCTION
CLK	I		Clock input. This is the clock used by the CSR bus master(s).
CENTRAL_EN	I		Central arbiter enable. This device is the central arbiter upon power-up if this bit is asserted. It will act as the system central arbiter if this bit is set while RST* is asserted. After RST* is released, the enable central arbiter bit controls whether this device is the system central arbiter. If central mode is disabled in the common control register, then this device operates as a distributed arbiter.
!NT*	O (open-collector)		Host interrupt. When an enabled interrupt condition occurs, this signal is driven low. Interrupts are cleared by writing a zero to the appropriate bit in the interrupt register. The interrupt goes high during the write cycle to the interrupt register even if another interrupt is pending.
PFAIL*	O		Power-fail message received
REF_CLK	I	Module	Clock input. The recommended frequency and duty cycle are 40 MHz, 50% ± 5%; 30 MHz to 50 MHz and 50% ± 20% can be tolerated.

JTAG test port

NAME	PIN TYPE	PIN FROM/TO	FUNCTION
TCK	I	Module	JTAG test clock
TDI	I	Module	JTAG test data in
TDO	O	Module	JTAG test data out
TMS	I	Module	JTAG test mode select

reset port

NAME	PIN TYPE	PIN FROM/TO	FUNCTION
BINIT*	O	Module	Open-collector signal indicating that a bus interface reset is required.
BUSI*	O		Bus has been idle for longer than 1 μs and **re** is asserted.
RE	I		Futurebus+ reset in
REf	O		Futurebus+ reset – filtered
RST*	I	Module	Module power-up reset. Resets all logic: output signals go to their inactive states; three-state outputs and bidirectionals go to the high-impedance state.
SYS_RESET*	O	Module	Open-collector signal indicating that a system reset is required.

central arbitration interface

NAME	PIN TYPE	PIN FROM/TO	FUNCTION
GR	O		Futurebus+ mastership has been granted (bus tenure may begin after ET* is released by the present master) for the corresponding module. Only one GRi is asserted at a time.
PE	O		Preemption has occurred for the present master. The bus should be released for use by a higher-priority module. This may be configured independently for each module to preempt when a module with equal or greater priority requests the bus.
RQ<0>	I		Futurebus+ mastership is requested at level 0. Separate requests come from each of 14 modules. Any unused request signals should be tied high.
RQ<1>	I		Futurebus+ mastership is requested at level 1. Separate requests come from each of 14 modules. Any unused request signals should be tied high.

PRODUCT PREVIEW

Terminal Functions (Concluded)

Futurebus+ interface

NAME	PIN TYPE	PIN FROM/TO	FUNCTION
AC<1:0>	I		Futurebus+ arbitration condition – input
ac<1:0>	O		Futurebus+ arbitration condition – output
AP, AQ, AR	I		Futurebus+ arbitration handshake – input
ap, aq, ar	O		Futurebus+ arbitration handshake – output
AS	I		Futurebus+ address handshake – input
CENT_MODE	O		Central-mode operation is in effect
CMPT*	O		Arbitration contest logic compete indication
CN<7:0>, CNP	I/O		Futurebus+ contest number and parity
GA<4:0>*	I		Futurebus+ geographical address
LE*	O		Enable latch on competition transceiver
OEA	O		Enable TTL drivers on competition transceiver
WIN	I		Arbitration contest logic win indication

PRODUCT PREVIEW

detailed description

interface to the protocol controller

In distributed mode, the TFB2011 receives requests from a controller and performs distributed arbitration cycles to gain mastership of the bus for the host module. When mastership is acquired, the host module is granted the bus. Preemption and arbitration errors are signaled through this interface. Arbitration errors are signaled synchronously with respect to the host clock (CLK). The request, grant, and preemption handshake is identical to the Futurebus+ central-mode handshake. This mechanism is identical to that used in the TFB2010 arbitration bus controller.

arbitration messages

This device supports sending and receiving messages in both central and distributed modes. It supports four types of received messages: central arbiter priority updates, targeted interrupts, selected messages, and power fail.

Central arbiter priority updates are messages that are used to program the central arbiter. They are captured and stored in the appropriate field of the module configuration register regardless of whether or not this module is enabled as the central arbiter. This allows an easier transition between central arbiters for fault-tolerant systems.

The TFB2011 fully supports the standard targeted interrupts described in 896.2. Target interrupts cause a bit in the target interrupt set register to be set if the corresponding bit in the target interrupt mask register is set. This may cause an interrupt if target interrupts are enabled. The ID of the highest-priority target interrupt is made available for simplification of software.

The message control register is used to determine which messages are selected for receipt by the host module. Some selected messages may be sent to a particular destination, while others may be globally broadcast within the system. Two classes of selected messages are supported in the TFB2011 through the use of a four-byte register. Two bytes are associated with each message class. Each byte pair has two parts: a mask value and a mask enable. The mask value byte defines the value to be compared against; the mask enable indicates which bits to compare. For example, if the message class value byte contains the value 01101001 and the message class enable byte contains 11110000, then all messages beginning with 0110xxxx are stored in the 4-deep FIFO;

arbitration messages (continued)

any other messages are ignored. The second mask register operates in a similar fashion. In addition, all messages with the value FE or FF are stored in the FIFO. Duplicate messages are ignored if the configuration register indicates that they should be ignored.

The message FF causes the PFAIL signal to be asserted, indicating a power failure. If Profile-B power-fail encoding is specified in the configuration register, then messages 0x60 through 0xFF are interpreted as power-fail notification. Whenever a power failure is detected, the PFAIL interrupt status bit is set; if enabled, a power-failure interrupt also occurs.

JTAG interface

The TFB2011 contains a JTAG (IEEE 1149.1) test port. The device was designed with boundary scan I/O buffers and a JTAG state machine, allowing it to be tested with industry-standard JTAG test methods. Even parity is used to protect the instruction value. The instruction plus parity is an eight-bit value. It is scanned in using an instruction register (IRSCAN) JTAG sequence. While an instruction is scanned in, the previous instruction's status is scanned out. Status is 0x81 if the previous instruction had even parity; status is 0x01 if the previous instruction had odd parity. This device supports the following instructions:

1. Bypass Scan [0xff]. Default instruction after reset. Data is scanned in through TDI. TDO follows the data scanned in by one clock cycle. This is used when odd parity is detected in the instruction.
2. Sample [0x82]. A snapshot of the values on the terminals is taken. The sampled values can be scanned out using a data-scan sequence. This does not interfere with normal system operation. Data may be scanned in to prepare for some other test.
3. EXTEST [0x00]. External boundary test, test mode.
4. INTEST [0x03]. Internal boundary test, test mode.
5. READBN [0x0A]. Read boundary register, normal mode.
6. CELLTEST [0x0C]. SCOPE self-test, normal mode.
7. READBT [0x8B]. Read boundary register, test mode.

CSR bus operation

The TFB2011 functions as a CSR bus slave. Reads and writes are sent to the TFB2011 through this bus. All register locations on the TFB2011 are accessed through the CSR bus, allowing the TFB2011 to be configured by the system. The CSR interface appears like an SRAM with output enables. CSR read and write cycles are shown in the CSR bus specification. All CSR transactions are bytewise to the byte address indicated in the table that follows. For example, the address of byte 3 of the target interrupt value set register (address 80) has the byte address 83.

internal registers (see CSR register mapping section)

The TFB2011 unit-specific CSR registers have a CSR offset of 3712.

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
80	Target interrupt value set	Core CSR [1212]	Writing to a bit in this register causes a targeted interrupt to occur if the corresponding mask bit is set. Reading this register returns zeroes. The value of these interrupt bits can be seen by reading the target interrupt clear register in the unit CSRs. The ID of the highest priority targeted interrupt pending can be seen in the target interrupt ID register in the unit CSRs. Target interrupts are also set by arbitrated messages if the corresponding mask bit is set.
84	Target interrupt mask	Core CSR [1212]	This register enables the interrupts in the previous register.

PRODUCT PREVIEW

internal registers (continued)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
512	Logical common control (CSR)†	Fbus CSR [896.2]	32-bit field representing the configuration of the system as defined in IEEE Standard 896.2. Only "Central arbiter" and "Distributed message enable" are implemented in the TFB2010. The rest of the bits may be implemented in CSR registers located in other devices. Writes should be broadcast to all devices containing bits for this register. The TFB2010 powers up with reads to this register disabled to allow a master copy of the register to exist in some other CSR device (eg., TFB2002). Bytes 0 and 1 — Not used Byte 2 CD<7> — Not used CD<6> — Not used CD<5> — Central arbiter CD<4> — Multiple packet mode CD<3> — Packet-length-64 enable CD<2> — Packet-length-32 enable CD<1> — Packet-length-16 enable CD<0> — Packet-length-8 enable Byte 3 CD<7> — Packet-length-4 enable CD<6> — Packet-length-2 enable CD<5:4> — High packet speed CD<3:2> — Low packet speed CD<1> — Distributed message enable CD<0> — Split enable
516	Logical module control (CSR)†	Fbus CSR [896.2]	32-bit field representing the configuration of the module as defined in IEEE Standard 896.2. Only "parity report enable" and "master enable" are implemented in the TFB2010. The rest of the bits may be implemented in CSR registers located in other devices. Writes should be broadcast to all devices containing bits for this register. The TFB2010 powers up with reads to this register disabled to allow a master copy of the register to exist in some other CSR device (eg., TFB2002). Byte 0 CD<7:4> — Read or write registers (undefined) CD<3> — Noncache-data-width-64 enable CD<2> — Noncache-data-width-128 enable CD<1> — Noncache-data-width-256 enable CD<0> — Cache-data-width-32 enable Byte 1 CD<7> — Cache-data-width-64 enable CD<6> — Cache-data-width-128 enable CD<5> — Cache-data-width-256 enable CD<4> — Message-data-width-32 enable CD<3> — Message-data-width-64 enable CD<2> — Message-data-width-128 enable CD<1> — Message-data-width-256 enable CD<0> — CSR-data-width-64 enable Byte 2 CD<7> — CSR-data-width-128 enable CD<6> — CSR-data-width-256 enable CD<5> — Local clock CD<4> — Reference clock CD<3:1> — Compelled data length CD<0> — Packet mode Byte 3 CD<7> — 64-bit-address enable CD<6:4> — Number of tag lines active CD<3> — Tag enable CD<2> — Parity report enable CD<1> — High speed enable. If this bit is 1, then high-speed packet mode is used exclusively. If this bit is 0, then low speed is used exclusively. CD<0> — Master enable

† Reads from these registers are enabled using bit 3 in byte 2 of the configuration register. This allows the TFB2002 I/O Controller to provide the data for these shared registers.

internal registers (continued)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
520	Bus propagation delay [CSR]†	Fbus CSR [896.2]	This 6-bit register contains the value set by the monarch to indicate the electrical length of the system bus. The value is in 2^{-32} seconds. This register defaults to 0x3F (approximately 15 ns). Only bits 5 through 3 of byte 3 are implemented in this device. This register may exist in several devices on the CSR bus. The TFB2010 powes up with reads to this register disabled as with the logical common and logical module control registers.
524	Competition settling time	Fbus CSR [896.2]	This register defines the settling time for the worst-case arbitration number for this module. This is a 12-bit value located in bytes 2 and 3. The value is in 2^{-32} seconds. This value is loaded during initialization and must not be changed during an arbitration sequence. This register defaults to 0x600 (about 358 ns) when RST* or BINIT* is asserted.
3712	RQ0 priority	Unit-specific [read or write]	This register contains the 8-bit priority used when RQ0 is asserted. It is located in byte 3. In distributed mode, this number is used to determine the arbitration number. In central mode, this number is sued to automatically program the central arbiter via an arbitrated message. This allows greater portability of software between various arbiter configurations.
3716	RQ1 priority	Unit-specific [read or write]	This register contains the 8-bit priority used when RQ1 is asserted. It is located in byte 3. In distributed mode, this number is used to determine the arbitration number. In central mode, this number is sued to automatically program the central arbiter via an arbitrated message. This allows greater portability of software between various arbiter configurations.
3720	Send arbitration message/message FIFO	Unit-specific [read or write]	This register contains the 8-bit message. It is located in byte 3. When this register is written, an arbitration message is sent. If a request is pending, the arbitration message is sent first. This operation causes a preemption of a master elect if one exists. Reading from byte 3 retrieves the first message received. When the FIFO is empty, it returns the last value read. The RFNE bit in the interrupt status register is set when the FIFO is not empty. Up to four incoming arbitration messages can be buffered in this FIFO. A message matching one of the masks is received by the FIFO; all others are ignored. If an incoming message matches one already in the FIFO, the duplicate message is ignored if ignore duplicate messages is enabled in the configuration register.
3724	Interrupt status clear	Unit-specific [read or write 1 to clear]	Bytes 0 and 1: Not used Byte 2: CD<7> PGAIL. Power-fail message received CD<6> ARBERR. An arbitration error occurred during Futurebus+ competition. CD<5> CMPPARERR. A compare or parity error occurred during Futurebus+ competition. CD<4> PHS24TO. Phase 2 or 4 1-μs timeout occurred. CD<3> DMTOUT. Deadman timeout occurred. This indicates that phase 1 or phase 0 for a two-pass competition exceeded the timeout value. CD<2> CSR_PAR_ERR. A CSR parity error has been detected. CD<1> RE. Interrupt if RE* is asserted. CD<0> AMOV. Arbitration message FIFO overflow has occurred. Byte 3: CD<7> 0 CD<6> TARGET_INT. A target interrupt has been received. CD<5:4> 00 CD<3> GRANT. Bus has been granted (GR asserted) Informs software when the priority registers may be updated without affecting an on going bus acquisition. CD<2> RFNE. The arbitration message receive FIFO is not empty. CD<1> MSG_SENT. The arbitration message has been sent. CD<0> PRI_UPD. The arbitration priority has been updated. Writing a one to a bit in this register clears the bit until the interrupt condition is released and then recurs.

† Reads from these registers are enabled using bit 3 in byte 2 of the configuration register. This allows the TFB2002 I/O Controller to provide the data for these shared registers.

internal registers (continued)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
3728	Interrupt status set	Unit-specific [read or write 1 to set]	Bytes 0 and 1: Not used Byte 2: CD<7> PGAIL. Power-fail message received CD<6> ARBERR. An arbitration error occurred during Futurebus+ competition. CD<5> CMPPARERR. A compare or parity error occurred during Futurebus+ competition. CD<4> PHS24TO. Phase 2 or 4 1-µs timeout occurred. CD<3> DMTOUT. Deadman timeout occurred. This indicates that phase 1 or phase 0 for a two-pass competition exceeded the timeout value. CD<2> CSR_PAR_ERR. A CSR parity error has been detected. CD<1> RE. Interrupt if RE* is asserted. CD<0> AMOV. Arbitration message FIFO overflow has occurred. Byte 3: CD<7> 0 CD<6> TARGET_INT. A target interrupt has been received. CD<5:4> 00 CD<3> GRANT. Bus has been grantd (GR asserted) Informs software when the priority registers may be updated without affecting an on going bus acquisition. CD<2> RFNE. The arbitration message receive FIFO is not empty. CD<1> MSG_SENT. The arbitration message has been sent. CD<0> PRI_UPD. The arbitration priority has been updated. Writing a one to a bit in this register sets the bit until the interrupt condition is cleared.
3732	Interrupt enable	Unit-specific [read or write]	This register is used to enable the interrupt conditions in the interrupt status register. When an interrupt is enabled and the interrupt condition is set, INT is asserted to the host module, and the ID of the interrupt condition is reported in the interrupt ID register.
3736	Interrupt ID	Unit-specific [read only]	This five-bit value represents the bit number of the highest priority interrupt that currently exists and is enabled. This value can be used to vector to the service routine. The next interrupt is seen when the interrupt condition has been cleared. This field is located in byte 3, bits CD<4:0>. The IDs are as follows: 31–17 Not used 16 PFAIL 15 ARBERR 14 CMPPARERR 13 PHS24TO 12 DMTOUT 11 CSR_PAR_ERR 10 RE 9 AMOV 8 Not used 7 TARGET_INT 6:5 Not used 4 GRANT 3 RFNE 2 MSG_SENT 1 PRI_UPD 0 No Interrupt
3740	Targeted interrupt clear	Unit-specific [read or write 1 to clear]	This register is used to clear target interrupts set in the target interrupt set register or by a target interrupt message. Writing to a bit in this register causes a targeted interrupt to be cleared. Reading this register returns the bits that had been set. The ID of the highest priority targeted interrupt pending can be seen in the target interrupt ID register in the unit CSRs.
3744	Targeted interrupt ID	Unit-specific [read only]	This register contains the value of the highest priority target interrupt that has been set.

internal registers (continued)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
3748	Configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> (PCBA only:) Enable central arbiter. When set, this module performs central arbitration for the system. This overrides the central_en pin that was used at power up to tell this device that it was the power-up central arbiter. Byte 2: CD<7> Not used CD<6> Only Master Enable. Setting this informs the TFB2010 that it is the only potential master in a distributed arbitration system. The arbitration process is bypassed and GR is asserted immediately in response to RQ1 or RQ0. CD<5> Bypass glitch filter CD<4> = 0: 40-MHz to 50-MHz reference clock used = 1: 30-MHz to 40-MHz reference clock used CD<3> Enable standard CSR reads. When this bit is released, reads of the logical module control, logical common control, and bus propagation delay CSRs are ignored (the CSR data bus is three-stated), while all other CSR reads operate normally. Reads of these CSR registers are typically handled by another device on the module since so few bits are implementd in this device. CD<2> Disable competition compare errors CD<1> CSR Bus Parity mode: = 0: odd parity = 1: even parity CD<0> Enable CSR bus parity error reporting: = 0: disable = 1: check Byte 3: CD<7> Profile-B encoding of power fail. If zero, power fail = arbitration message FF. CD<6> Enable FIFO overflow reporting to Futurebus+ (via ac0 error). Set ac0 error when this bit is set and FIFO overflow would result if present arbitration cycle ended normally. If this bit is released, FIFO overflow will occur. Stall overrides this operation. CD<5> Stall. Remain in phase 3 of the second pass of an arbitration message cycle if the receive FIFO is full. CD<4> Preemption mode (distributed mode only). If this bit value is 0, PE is set when another module of equal or higher priority requests the bus. If this bit value is 1, PE is set only when a higher-priority module requests the bus. CD<3> Preemption Enable. Enable TFB2010 to preempt a master elect during distributed arbitration. Note that arbitration messages preempt a master elect regardless of this bit. CD<2> Priority only: = 0: round robin = 1: priority only CD<1> Enable deadman timer. If enabled, each phase of arbitration is checked to ensure that it doesn't exceed 1.31 ms (phase 0 is checked only between first and second passes of two-pass arbitration). CD<0> Ignore duplicate messages: = 0: store all incoming messages in the FIFO = 1: ignore received messages that are already in the message FIFO

PRODUCT PREVIEW

internal registers (concluded)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
3752	Message control	Unit-specific [read or write]	This register contains the message mask values and enable parameters. Byte 0: Message mask enable 0 Byte 1: Message mask value 0 Byte 2: Message mask enable 1 Byte 3: Message mask value 1
3756	Optional arbitration settling times	Unit-specific [read or write]	If any byte in this register is zero, the corresponding group uses the value in the arbitration settling time register (524). Each byte represents a delay in 2^{-28} seconds. **NI** refers to the maximum number of bus iterations required by the arbitration number. An Ni of zero means that the device will know whether it is the winner as soon as its number has propagated down the bus and back. Ni = 4 may require four iterations of the bus delay plus the initial bus delay. The Ni number is equal to the number of 1-to-0 transitions there are in the outgoing competition number. These values are loaded during initialization and must not be changed during an arbitration sequence. This register is cleared when either RST* or BINIT* is asserted. Byte 0 for Ni = 0 or 1 Byte 1 for Ni = 2 Byte 2 for Ni = 3 Byte 3 for Ni = 4
3760	Master ID	Unit-specific [read only]	Bytes 0 and 1: Current master's ID and priority Bytes 2 and 3: Master elect's ID and priority
3764	Arbitration bus monitor	Unit-specific [read only]	Byte 0: Not used Byte 1: CD<7:5> Not used CD<4:0> GA<4:0> Byte 2: CD<7> AC0 CD<6> AC1 CD<5> AR CD<4> AQ CD<3> AP CD<2> WIN CD<1> Not used CD<0> ABP Byte 3: CD<7:0> AB<7:0>
3768	Test port	Unit-specific [read only]	Silicon testing only
3772	Test port	Unit-specific [read only]	Silicon testing only

PRODUCT PREVIEW

module configuration registers

These registers are used to program the preemption mode for each module. They may be used as back doors for programming the priorities of the modules. The normal mode of priority programming of the central arbiter uses arbitration messages.

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
3776	Module 0 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode: = 0: PE0 is set when another module of equal or greater priority requests the bus. = 1: PE0 is set only when a higher-priority module requests the bus. Byte 2: RQ00 priority (for module 0) Byte 3: RQ10 priority (for module 0)
3780	Module 1 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 1 Byte 2: RQ01 priority Byte 3: RQ11 priority
3784	Module 2 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 2 Byte 2: RQ02 priority Byte 3: RQ12 priority
3788	Module 3 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 3 Byte 2: RQ03 priority Byte 3: RQ13 priority
3792	Module 4 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 4 Byte 2: RQ04 priority Byte 3: RQ14 priority
3796	Module 5 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 5 Byte 2: RQ05 priority Byte 3: RQ15 priority
3800	Module 6 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 6 Byte 2: RQ06 priority Byte 3: RQ16 priority

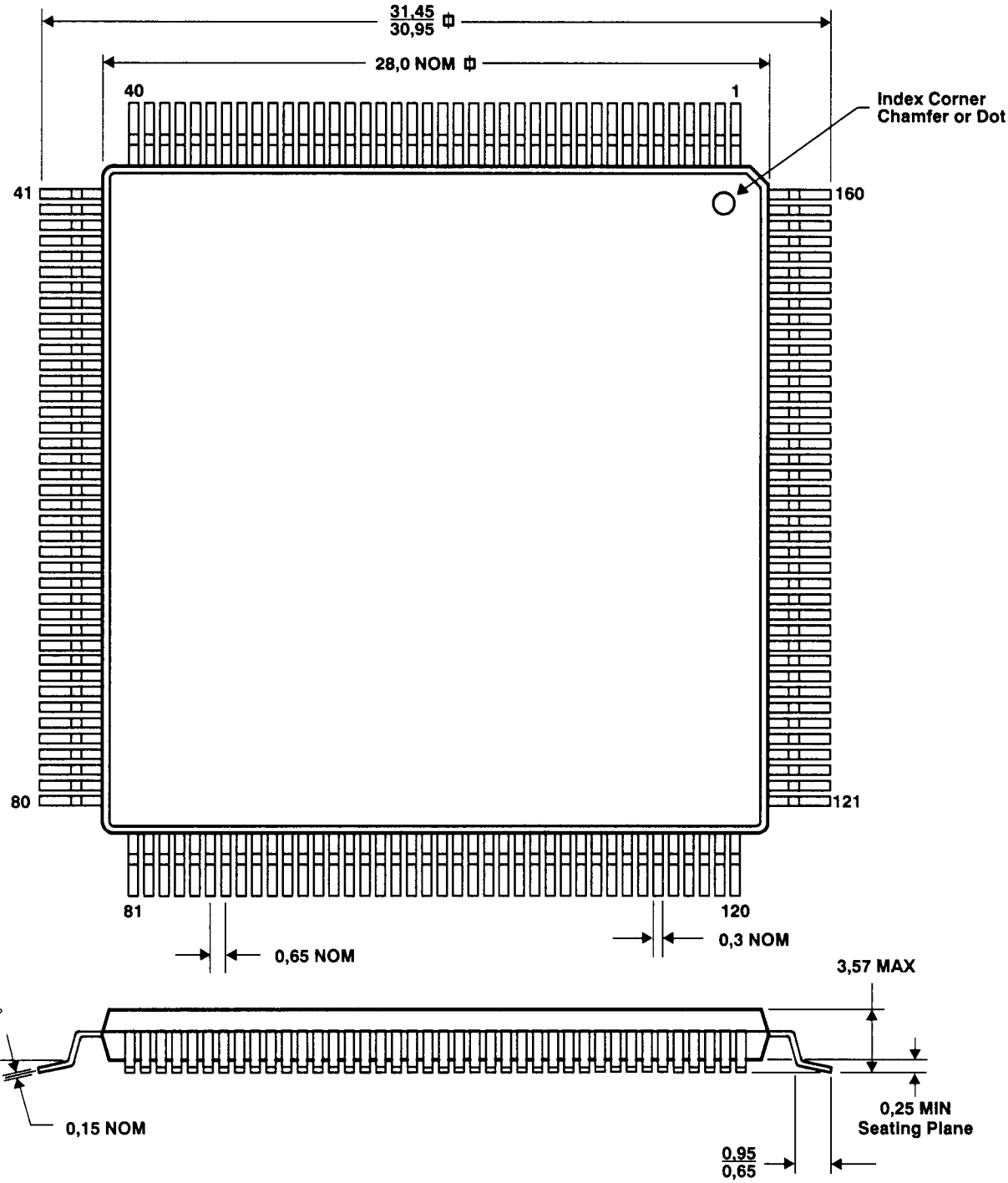
module configuration registers (concluded)

ADDRESS	NAME	TYPE	REGISTER DESCRIPTION
3804	Module 7 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 7 Byte 2: RQ07 priority Byte 3: RQ17 priority
3808	Module 8 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 8 Byte 2: RQ08 priority Byte 3: RQ18 priority
3812	Module 9 configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module 9 Byte 2: RQ09 priority Byte 3: RQ19 priority
3816	Module A configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module A Byte 2: RQ0A priority Byte 3: RQ1A priority
3820	Module B configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module B Byte 2: RQ0B priority Byte 3: RQ1B priority
3824	Module C configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module C Byte 2: RQ0C priority Byte 3: RQ1C priority
3828	Module D configuration	Unit-specific [read or write]	Byte 0: Not used Byte 1: CD<7:1> Not used CD<0> Preemption mode for module D Byte 2: RQ0D priority Byte 3: RQ1D priority
3832	Test port	Unit-specific [read or write]	Silicon testing only
3836	Test port	Unit-specific [read or write]	Silicon testing only

PRODUCT PREVIEW

MECHANICAL DATA

160-Pin Plastic Quad Flat Package (PCM Package)



Leads are coplanar to within 0,1 mm.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.

PRODUCT PREVIEW