GoldStar
GOLDSTAR ELECTRON CO., LTD.

GM82C803A/B

FDC, UARTS with FIFO,
EPP/ECP, IDE Controller

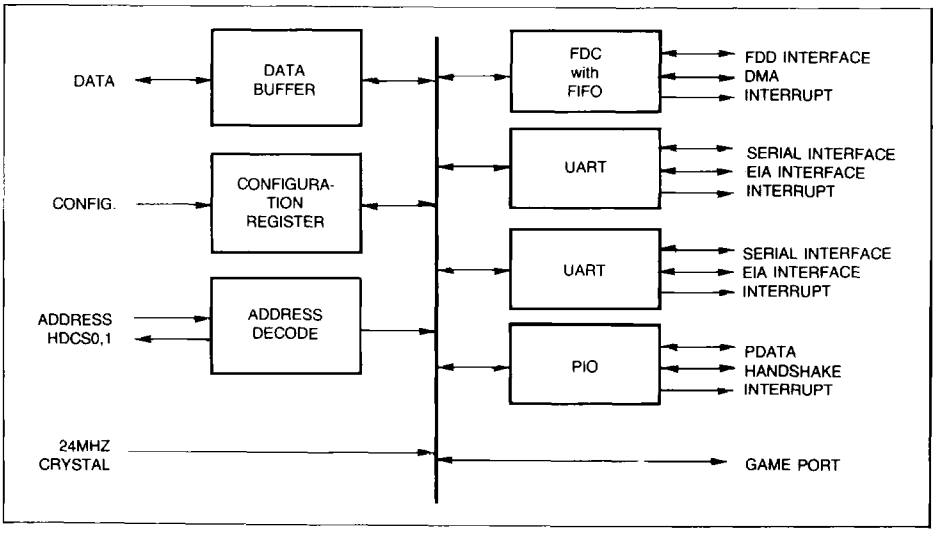
General Description

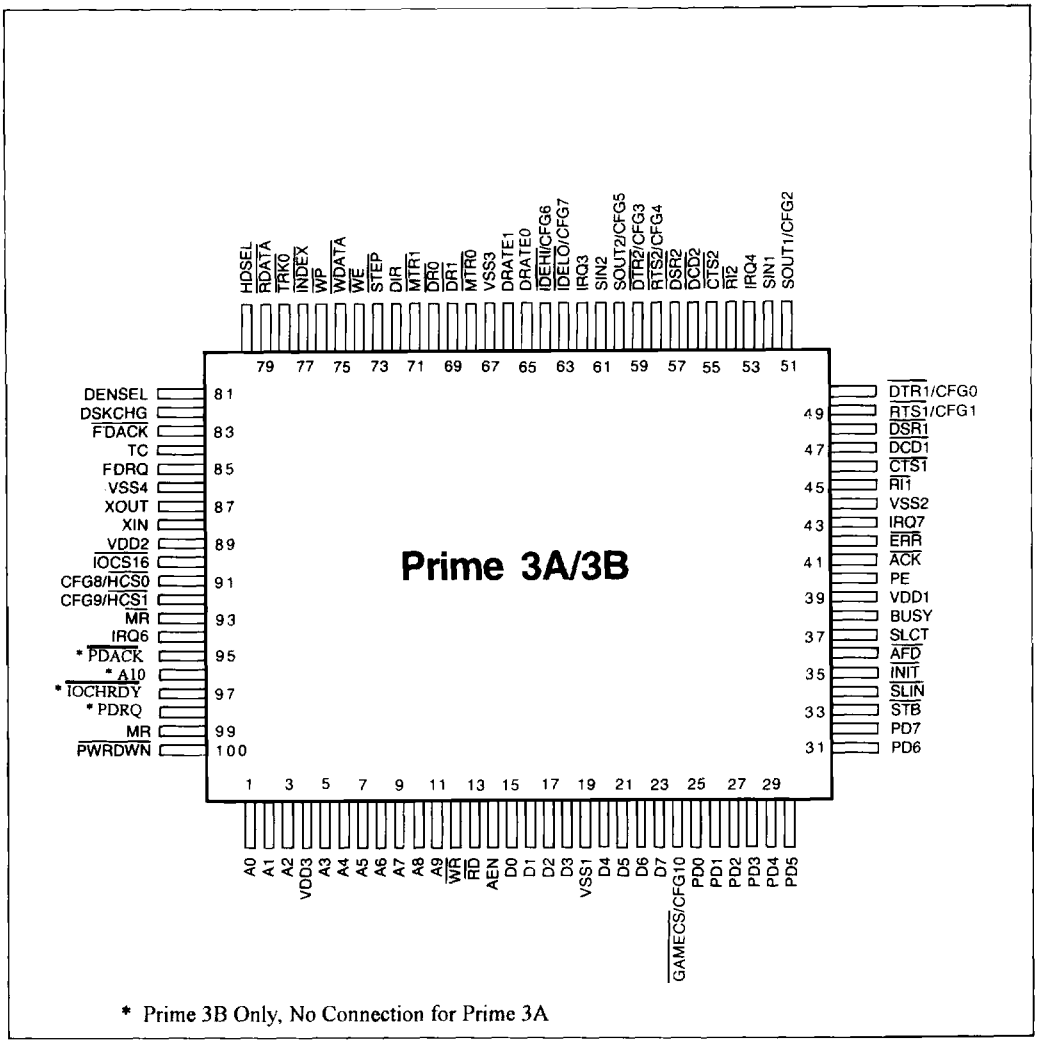
The GM82C803A/B chip replaces with a single 100 pin chip, a floppy disk controller (FDC) with data separator, two UARTs(GM16C550), one IEEE 1284 parallel port. The GM82C803A/B also includes one game port chip select, hard disk controller interface and standard AT address decoding for on-chip function. The floppy disk control part provides all the needed functionality between the host processor peripheral bus and the cable connector to the floppy disk driver. It integrates the function of the formatter/controller, data separator, write, precompensation, data rate selection, clock generation and high current drivers and supports the 4MB drive as well as the other standard drives. The UARTs perform the parallel to serial/serial to parallel conversion on the data characters received from the CPU or Modem. The IEEE 1284 parallel port is full compatible with the new IEEE 1284 standard. Configuration registers can be used to enable or disable any on-chip function independently of the others.

Features

- 100% hardware and software compatible to the IBM PC/AT
- Floppy disk controller with 16byte FIFO (default disable)
- 100% compatible to the 765B architecture
- FDD SWAP
- Data rate up to 1Mbps
- Perpendicular recording drive support
- Drives up to four FDD
- 48mA floppy disk drive interface
- Dual UART compatible to the GM16C550
- MIDI interface
- 16 byte transmitter and receiver FIFO
- Programmable character lengths (5,6,7,8)
- Even, odd, stick or no parity bit generation and detection
- Independent transmit and receive control
- IDE interface
- Additional PIO Mode (Prime 3B only)
- ECP (IEEE1284)
- EPP (Version 1.9 : Default, Version 1.7)
- One game chip select
- Low power mode
- Fabricated in GS's 0.8μm DLM CMOS technology
- 100-pin PQFP

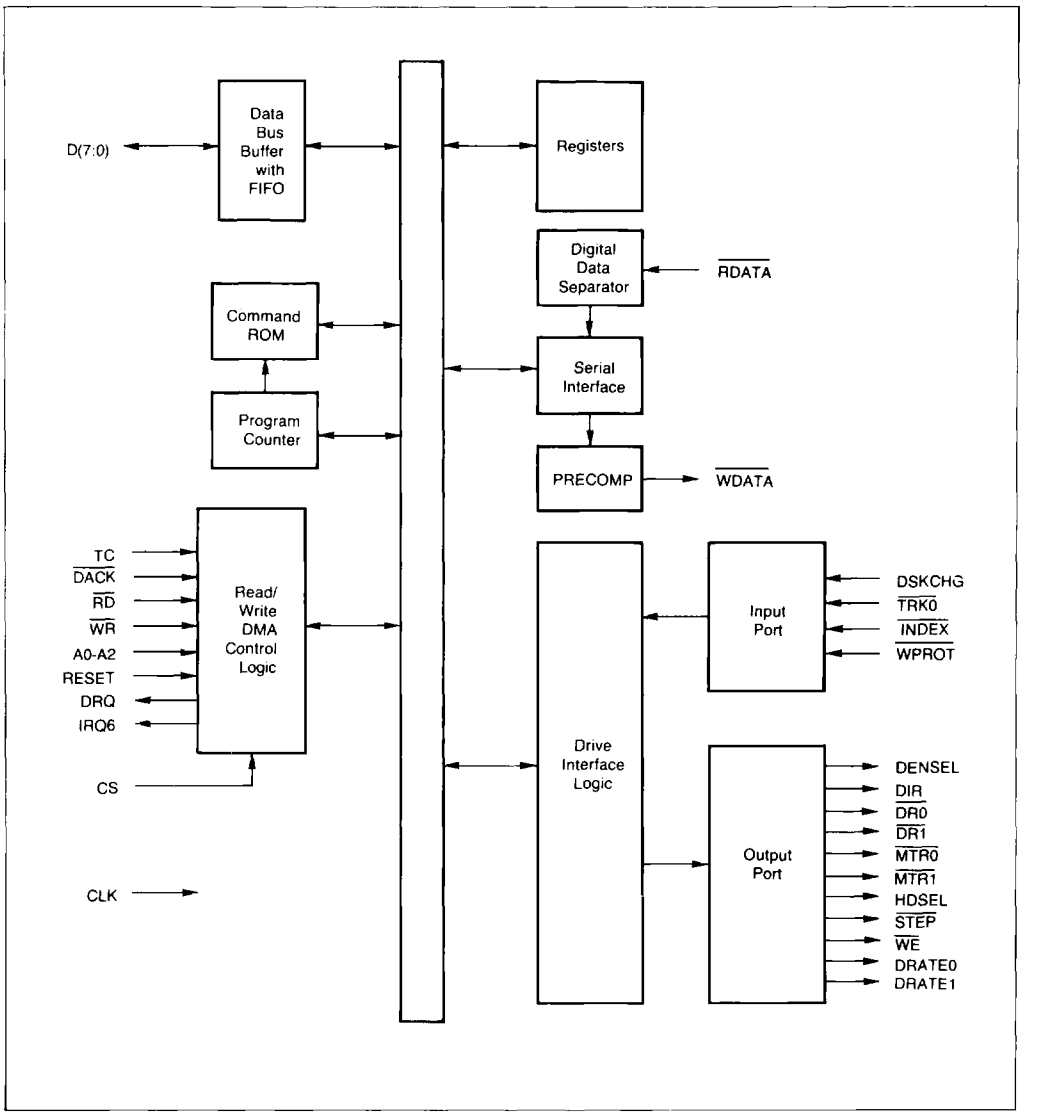
INTERNAL BLOCK DIAGRAM



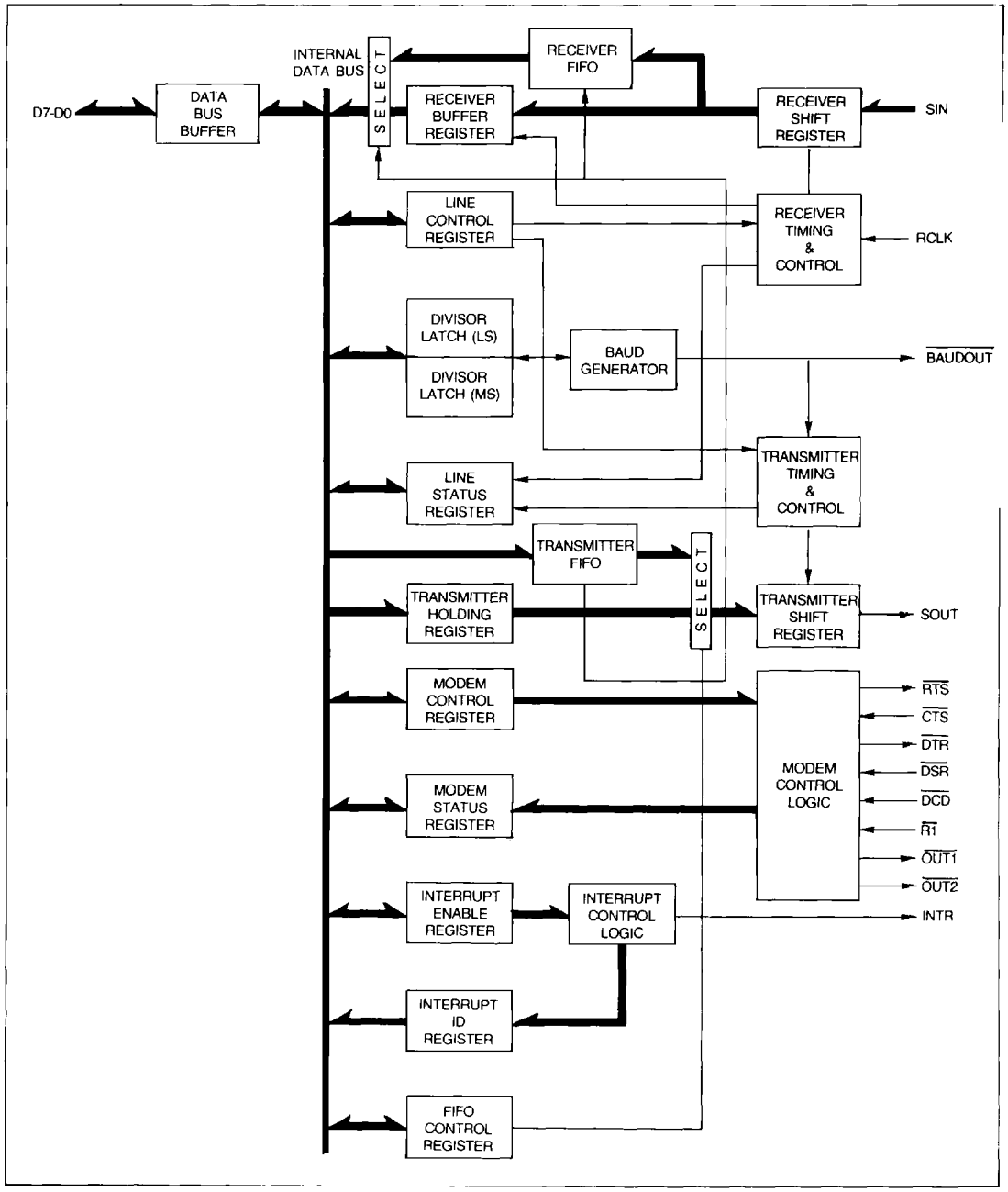


* Prime 3B Only, No Connection for Prime 3A

2. BLOCK DIAGRAM OF FDC



BLOCK DIAGRAM OF UART



3. PIN DESCRIPTIONS

(1) Host Interface

Pin No	Pin Name	I/O	Description
53	IRQ4	O	This active high output is serial port (assigned as COM1) interrupt. See PIN 62 (IRQ3).
62	IRQ3	O	This active high output is serial port (assigned as COM2) interrupt. It goes high whenever enabled via the IER and any of following serial interrupt conditions are active: Receiver Error Flag set, Receiver Empty or Modem Status Set. The interrupt is reset low upon appropriate service or a reset operation.
94	IRQ6	O	This active high output indicates that the completion of command execution or data transfer requests (in non-DMA mode) during FDC operation.
43	IRQ7	O	This active high output is parallel port interrupts. When enabled (Control Register bit 4 = 1), the appropriate interrupt signal will follow the $\overline{ACK}$ signal input.
11-5 3-1/96	A9-A0 /A10	I	The address lines select the internal registers during CPU bus operation.
14	AEN	I	This active high input disables address selection.
13	$\overline{RD}$	1	This active low input is a control signal for transfer of data or status onto the data bus by the GM82C803A/B.
12	$\overline{WR}$	I	This active low input is a control signal for latching data from the bus into the selected internal register.
99	MR	I	This active high input clears registers. In FDC, it clears device outputs, sets data rate to 250 kb/s. UART goes into an idle mode in which all serial data activities are suspended.
93	$\overline{MR}$	O	This active low output is reset signal. It is used for IDE interface.
15-18 20-23	D0-D7	I/O	The Data Bus provides eight 3-state I/O lines for the transfer of data, control and status information between GM82C803A/B and CPU.
97	$\overline{IOCHRDY}$	O	In EPP mode, this pin is pulled low to extended the read, write command.
84	TC	I	This active high input indicates the termination of a DMA transfer. TC will be qualified by $\overline{DACK}$.
100	$\overline{PWRDWN}$	I	This active low input will stop the clocks and make outputs Hi-Z state.
98	PDRQ	O	This active high output requests the DMA controller to transfer data. This signal is enabled by the bit 3 of Extended Control Register (ECR).
95	$\overline{PACK}$	I	This active low input is used by the DMA controller to trnsfer date from the GM82C803A/B onto the data bus. This signal is enabled by the bit 3 of Extended Control Register (ECR).

(2) Serial Interface

Pin No	Pin Name	I/O	Description
51	SOUT1	O	This output signal is serial data out from the UART's transmitter circuitry after reset or after 00H is written to the IIR. It is set to the Marking (logic 1) state upon a reset operation.
	BOUT1	O	This output provides the associated serial channel Baudout signal, after data 10H has been written to the IIR.
	CFG2	I	During rest, this input determines UART1 enable.
46	$\overline{CTS1}$	I	This active low input is a Modem status input and indicates that the modem has data to send. The CPU can test its condition by reading bit 4 of MSR. Bit 0 of MSR indicates whether this input has changed state since the previous reading of the MSR. It has no effect on the transmitter. If this signal changes state with the Modem status interrupt enabled, an interrupt is generated.
48	$\overline{DSR1}$	I	This active low input means that the Modem is ready to establish the communication link with the UART. This input is a Modem status input and reflected in bit 5 of Modem Status Register (MSR). Bit 1 of MSR indicates whether this signal has changed state since the previous reading of the MSR. It this signal change state with the Modem status interrupt enabled, an interrupt is generated.
50	$\overline{DTR1}$	O	This active low output indicates that the UART is ready to establish a communication link. This pin is set low by writing high to bit 0 of MCR. This pin is inactive (high) after reset.
	CFG0	I	During reset, this input determines IDE enable.
49	$\overline{RTS1}$	O	This active low output indicates that the UART has data ready to transmit. This pin is set to low by writing a logic 1 to bit 1 of Modem Control Register (MCR). This pin is inactive (high) after reset.
	CFG1	I	During reset, this input determines FDC enable.
45	$\overline{RI1}$	I	This active low input is Modem status input and indicates that telephone ringing signal has been received by the Modem. The CPU can test its condition by reading bit 6 of MSR. Bit 2 of MSR indicates whether this input has changed from high to low since the previous reading of the MSR. If this signal changes from high to low with the Modem status interrupt enabled, an interrupt is generated.
52	SIN1	I	This input receives serial data from the communication line or Modem.

(2) Serial Interface

Pin No	Pin Name	I/O	Description
47	$\overline{DCD1}$	I	This active low input indicates that the data carrier has been detected by the Modem. This is Modem input whose condition can be tested by the CPU by reading bit 7 of MSR. Bit 3 of MSR indicates whether this input has changed since the previous reading of the MSR. It has no effect on the receiver. If this signal changes state with the Modem status interrupt enabled, an interrupt is generated.
60	SOUT2	O	See PIN 51 (SOUT1)
	CFG5	I	During reset, this input determines state of configuration bit 5.
55	$\overline{CTS2}$	I	See PIN 46 ($\overline{CTS1}$)
57	$\overline{DSR2}$	I	See PIN 48 ($\overline{DSR1}$)
59	$\overline{DTR2}$	O	See PIN 50 ($\overline{DTR1}$)
	CFG3	I	During reset, this input determines UART2 enable.
58	$\overline{RTS2}$	O	See PIN 49 ($\overline{RTS1}$)
	CFG4	I	During reset, this input determines state of configuration bit 4.
54	$\overline{RI2}$	I	See PIN 45 ($\overline{RI1}$)
61	SIN2	I	See PIN 52 (SIN1)
56	$\overline{DCD2}$	1	See PIN 47 ($\overline{DCD1}$).

(3) Parallel Port Interface

Pin No	Pin Name	I/O	Description
32-25	PD7-PD0	I/O	These bidirectional pins provide a byte wide input or output port to the system.
37	SLCT	I	This active high input means that the printer is selected.
33	$\overline{STB}$	O	This active low output indicates to the printer that the data at the parallel port is valid.
34	$\overline{SLIN}$	O	This active low output selects the printer.
40	PE	I	This active high input means that the printer is out of paper.
36	$\overline{AFD}$	O	This active low output makes the printer to line feed automatically after each line printed.
38	BUSY	I	This active high input means that the Printer has a local operation in progress.
42	$\overline{ERR}$	O	This active low input means that the printer has detected an error.
35	$\overline{INIT}$	O	This active low output initializes the printer.
41	$\overline{ACK}$	I	This active low input means that the printer has received data.

(4) IDE Interface

Pin No	Pin Name	I/O	Description
63	$\overline{IDELO}$	O	This active low output enables the low byte data latch during a read or write to the hard drive.
	CFG7	I	During reset, this input determines UART1 address range.
64	$\overline{IDEHI}$	O	This active low output enables the high byte data latch during a read or write to the hard drive if the hard drive returns $\overline{IOCS16}$.
	CFG6	I	During reset, this input determines UART2 address range.
91	$\overline{HCS0}$	0	This active low output provides a harddisk enable signal.
	CFG8	I	During reset, this input determines FDC address range.
92	$\overline{HCS1}$	O	In AT application, this active low output provides a harddisk enable signal.
	CFG9	I	During reset, this input determines IDE address range.
90	$\overline{IOCS16}$	I	This active low input is driven by the peripheral device when it can accommodate a 16-bit access.

(5) FDD Interface

Pin No	Pin Name	I/O	Description
81	DENSEL	O	This output indicates whether a low (250/300 Kbps) or high (500 Kbps/1 Mbps) data rate has been selected.
72	DIR	O	This open drain output indicates the direction of the head movement. Logic 0 = step in, logic 1 = step out.
66, 65	DRATE1,0	O	This outputs reflect the contents of bits 1, 0 of the Control Register.
69, 70	$\overline{DR1, 0}$	O	These open drain outputs select drive 1 and drive 0. They are ANDed with the corresponding motor enable lines. These pins contain encoded drive select information if Bit 7 of the Function Selection Register is logic 1.
82	DSKCHG	I	This active high input indicates that the disk drive door has been opened. The active high state of this input is read from bit D7 of I/O address 3f7H.
77	$\overline{INDEX}$	I	This active low input indicates the beginning of a track.
80	HDSEL	O	This open drain output indicates which disk drive head is active. Logic 0 = Head 1, logic 1 (open) = Head 0.
79	$\overline{RDATA}$	I	This input is the raw serial bit stream from the disk drive.
71,68	$\overline{MTR1,0}$	O	These open drain outputs enable drive 1 and drive 0. These pins contain encoded drive select information if Bit 7 of the Function Selection Register is logic 1.
73	$\overline{STEP}$	O	This active low output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
78	$\overline{TRK0}$	I	This active low input indicates that the head is at track 0.
75	$\overline{WDATA}$	O	This open drain output is write precompensated serial data to be written onto the selected disk drive.
74	$\overline{WE}$	O	This open drain output becomes true just prior to writing on the diskette. This allows current to flow through the write head.
76	$\overline{WP}$	I	This active low input indicates that the diskette is write protected.
85	FDRQ	O	This active high output requests the DMA controller to transfer data. This signal is enabled by the bit 3 of Operation Register.
83	$\overline{FACK}$	I	This active low input is used by the DMA controller to transfer data from the GM3104F onto the data bus. This signal is enabled by the bit 3 of Operation Register.

(6) Game Interface

Pin No	Pin Name	I/O	Description
24	$\overline{\text{GAMECS}}$	O	This is the game port chip select output-active low.
	CFG10	I	During reset, this input determines Parallel port address range.

(7) Power and Ground

Pin No	Pin Name	I/O	Description
39	VDD1	P	+5V DC digital power supply
89	VDD2	P	+5V DC digital power supply
4	VDD3	P	+5V DC digital power supply
19	VSS1	G	0V Reference
44	VSS2	G	0V Reference
67	VSS3	G	0V Reference
86	VSS4	G	0V Reference
88	XIN	I	One side of an external 24Mhz crystal is attached here. An external clock is required if crystal is not used.
87	XOUT	O	One side of an external 24Mhz crystal is attached here. If an external clock is used, this pin should not be connected.

4. FUNCTIONAL DESCRIPTIONS

4.1 Configuration Register

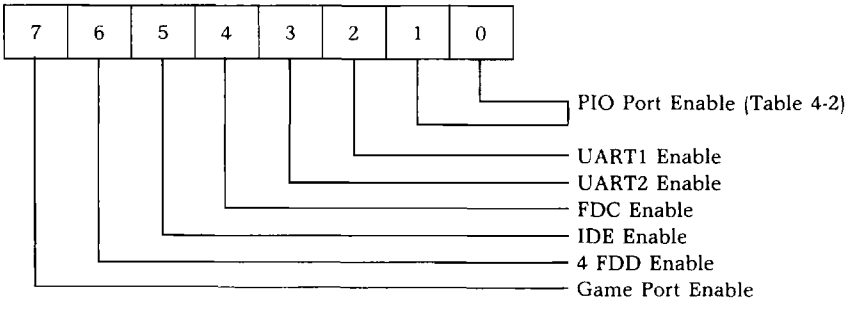
The GM82C803A/B has six byte-wide configuration registers. These Registers are called Function Selection Register (FSR), Address Selection Register (ASR), Power Down Register (PDR), Test Mode Register (TMR), Miscellaneous Function Register (MFR) and ECP Register, respectively. The FSR enables or disables each functional blocks such as FDC, UART1, UART2, PIO, IDE and Game Port. The ASR selects the I/O address ranges of these blocks. The PDR controls the Power Down Mode for the portable system applications. The TMR is used to enhance chip testability.
The configuration registers can be programmed via hardware or software. The states of the 11 configuration pins determine the default value of these registers during system reset. This defines the setting of all configuration registers via hardware. An index and data register pair is used to read and write these registers. Each configuration register is pointed to by the value loaded into the index register. The data to be written into the configuration register is transferred via the data register. Reading a configuration register is done in a similar way. The I/O addresses of the index and data register are 398H and 399H, and the indexes of the six registers are A0, A1, A2, A3, A4 and A5, respectively.

Table 4-1. Index and Data Register I/O Address

Register	I/O Address	Index
Index	398	
Data	399	
FSR		A0
ASR		A1
PDR		A2
TMR		A3
MFR		A4
ECP		A5

4.1.1 Function Selection Register (FSR)

Index = A0



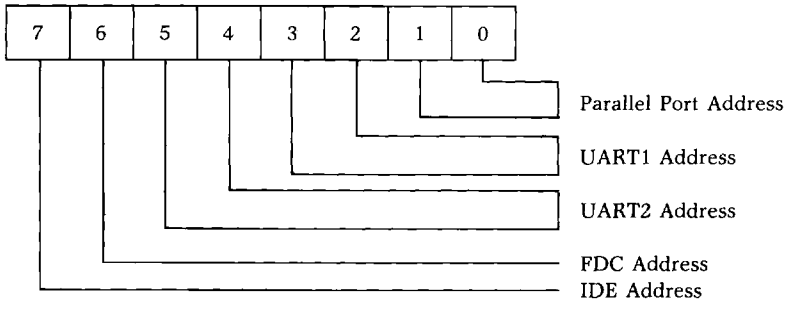
Bit (7:2) are active high enable.

Table 4-2. PIO Port Function Selection

D1	D0	PIO Port Enable
0	0	Bidirection Mode
0	1	ECP (Prime 3B)
1	0	EPP (Prime 3B)
1	1	PIO Disable

4.1.2 Address Selection Register (ASR)

Index = A1



This register selects the ISA I/O address range to which each peripheral function will respond.

Table 4-3. Parallel Port Address Selection

D1	D0	LPT Address Range
0	0	LPT2 (378-37F)
0	1	LPT3 (278-27F)
1	X	LPT1 (3BC-3BE)

Table 4-4. UART1 Address Selection

D3	D2	COM Address Range
0	0	COM1 (3F8 – 3FF)
0	1	COM2 (2F8 – 2FF)
1	0	COM3 (3E8 – 3EF)
1	1	COM4 (2E8 – 2EF)

Table 4-5. UART2 Address Selection

D5	D4	COM Address Range
0	0	COM1 (3F8 – 3FF)
0	1	COM2 (2F8 – 2FF)
1	0	COM3 (3E8 – 3EF)
1	1	COM4 (2E8 – 2EF)

Table 4-6. FDC Address Selection

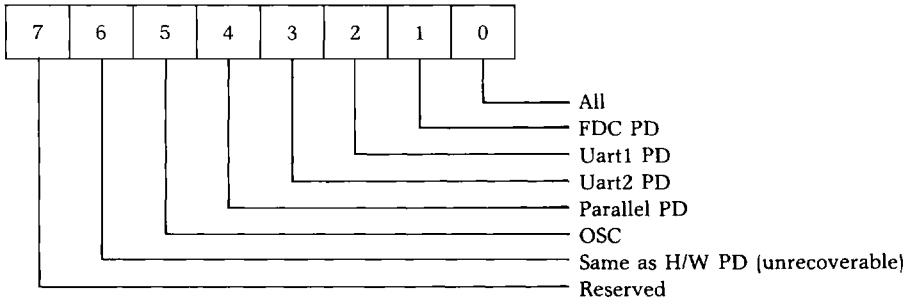
D6	FDC Address Range
0	3F0 – 3F7
1	370 – 377

Table 4-7. IDE Address Selection

D7	IDE Address Range
0	1F0 – 1F7, 3F6, 3F7
1	170 – 177, 376, 377

4.1.3 Power Down Register (PDR)

Index = A2



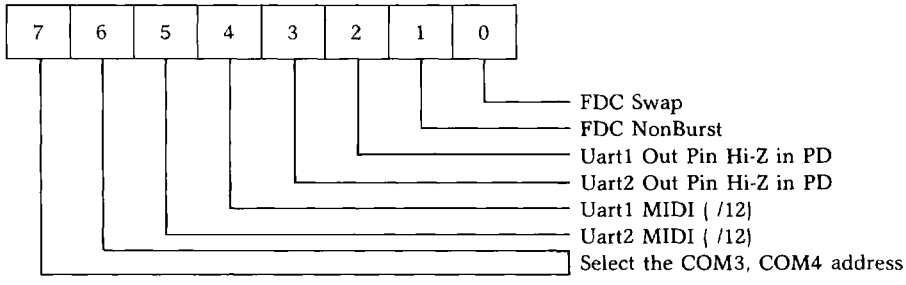
4.1.4 Test Mode Register (TMR)

This register is used to support chip debugging and testing. The system should not access this register.

Index = A3
Data = 00

4.1.5 Miscellaneous Function Register (MFR)

Index = A4

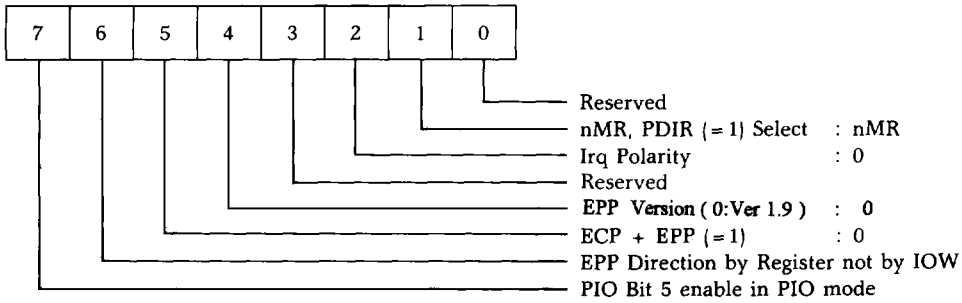


7 6	COM3	COM4	
0 0	3E8-F	2E8-F	
0 1	338-F	238-F	(Default)
1 0	2E8-F	2E0-F	
1 1	220-7	228-F	

Table 4-8. COM3, 4 Address

4.1.6 ECP Register

Index = A5



4.1.7 Hardware Configuration

The eleven configuration pins (CFG0 — 10) determine the default values of FSR and ASR during system reset. CFG0-5 are used for FSR and CFG6-10 are used for ASR. After system reset, the system can modify the configuration registers by software. Table 4-7 shows the hardware configuration of FSR. The default value of the bit 6 (4 FDD select) and the bit 7 (Game Enable) of FSR are 0 (Disable) and 1 (Enable), respectively. And the default values of PDR and TMR are 00H.

Table 4-9. Hardware Configuration of FSR

CFG pin	Enabled Functions
0	IDE Enable
1	FDC Enable
2	UART2 Enable
3	UART1 Enable

CFG pin (3:0) are active high enable.

Table 4-10. PIO Hardware Configuration

CFG 5	CFG 4	PIO Port Enable
1	1	Bidirection Mode
1	0	ECP (Prime3B)
0	1	EPP (Prime3B)
0	0	PIO Disable

Table 4-11. UART1 Hardware Configuration

CFG6	UART1 Address
1	COM1 (3F8 — 3FF)
0	COM3 (3E8 — 3EF)

Table 4-12. UART2 Hardware Configuration

CFG7	UART2 Address
0	COM2 (2F8 — 2FF)
0	COM4 (2E8 — 2EF)

Table 4-13. FDC Hardware Configuration

CFG8	FDC Address
1	Primay (3FO — 3F7)
0	Secondary (370 — 377)

Table 4-14. IDE Hardware Configuration

CGF9	IDE Address
0	Primary (1F0 — 1F7, 3F6-7)
0	Secondary (170 — 177, 376-7)

Table 4-15. Parallel Port Address Hardware Configuration

CFG10	Parallel Port Address
1	LPT2 (378-37F)
0	LPT3 (278 — 27F)

4.1.8 S/W configuration procedure

Configuration is accomplished in three basic steps:

1. Enter configuration mode
2. Configure the GM82C803A/B
3. Escape from configuration mode

Any deviation from this sequence causes the configuration state machine to return to its initial idle state. The configuration procedure is intentionally complicated to prevent an errant program from making accidental changes to the chip configuration.

Enter Configuration Mode

Write two consecutive writes of value 33h to port 398h.
The following is an example in 8086 assembly language:

```
MOV   DX, 398h  : Port Address
MOV   AL, 33h   : Data
OUT   DX, AL
OUT   DX, AL    : In configuration mode
```

Cnfigure the Chip

The six configuration registers can be written to or read.
To read or write data to the registers:
1. Write index to port 398h
2. Write data to port 399h
(where "data" is the data to be written into the register that port 398h points to)

Escape from Configuration Mode

Write cch to port 398h.
The following is an example

```
MOV   DX,398h  : Port Address
MOV   AL,cch   : Data
OUT   DX,AL    : Exit from configuration mode
```

4.2 Floppy Disk Controller

The FDC contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. The FDC is capable of supporting either IBM3740 single density format(FM), or IBM system 34 double density format (MFM) including double sided recording. It simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface. It supports data rates of 250/300/500 Kb/s and 1Mb/s. This block integrates; Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, Drive interface drivers and receivers.
It has five registers which may be accessed by the main system processor; a main status register(MSR), a data rate selection register(DSR), a data register(DR), a control register(CR), and a operations register(OR). The main status register contains the status information of the FDC, and may be accessed at any time. The data rate selection register is used to program the data rate, amount of write precompensation, power down mode, and software reset. The data register (actually consists of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into the data register in order to program or obtain the results after execution of a command. The status register may only be read and is used to facilitate the transfer of data between the processor and FDC.

Table 4-16. Register Description and Address

Address (Hex)	R/W	Register
3F2	R/W	Operations Register
3F4	R	Main Status Register
	W	Data Rate Select Register
3F5	R/W	Data Register (FIFO)
3F7	W	Control Register
	R	Read DSKCHG (D7 only,.inverse)

FIFO (Data)

The FIFO is used to transfer disk data.It is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.
The FIFO has the defaults with 765B compatible mode after a hardware reset. Software resets (Reset via OR or DSR register) can also place the FDC into 765B compatible mode if the LOCK bit is set to zero (See the definition of the LOCK bit in Lock command). This maintains PC-AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 4-15 gives several examples of the delays with a FIFO. The data is based upon the following formula.

$$\text{Threshold\#} \times \left| \frac{1}{\text{Data Rate}} \right| \times 8 - 1.5\mu s = \text{Delay}$$

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\mu s - 1.5\mu s = 6.5\mu s$
2 bytes	$2 \times 8\mu s - 1.5\mu s = 14.5\mu s$
8 bytes	$8 \times 8\mu s - 1.5\mu s = 62.5\mu s$
15 bytes	$15 \times 8\mu s - 1.5\mu s = 118.5\mu s$

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1 \times 16\mu s - 1.5\mu s = 14.5\mu s$
2 bytes	$2 \times 16\mu s - 1.5\mu s = 30.5\mu s$
8 bytes	$8 \times 16\mu s - 1.5\mu s = 126.5\mu s$
15 bytes	$15 \times 16\mu s - 1.5\mu s = 238.5\mu s$

Table 4-17. FIFO service delay

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk Write will complete the current sector by generating a 00H pattern and valid CRC.

Main Status Register (MSR)

MSR indicates the current status of the disk controller. It is always available to be read and controls the flow of data to and from the Data Register (FIFO).

Table 4-18. Main Status Register

Bit	Symbol	Name	Function
D7	RQM	Request for Master	Indicates that Host can access the Data Register if one. No access should be attempted if zero.
D6	DIO	Data In/Out	Indicates the direction of the data transfer only when RQM is one. If one, transfer is from Data Register to Host. If zero, transfer is from Host to Data Register.
D5	EXM	Execution Mode	This bit is set to one only during execution phase in Non-DMA mode. When zero, execution phase has ended and result phase has started. EXM remains 0, if DMA mode is selected.
D4	CB	Controller Busy	A Read or Write is in progress. FDC will not accept any other command.
D3	F3B	FDD 3 Busy	If one, FDD number 3 is in seek mode. It won't accept Read or Write Command. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.
D2	F2B	FDD 2 Busy	Same as above for FDD 2.
D1	F1B	FDD 1Busy	Same as above for FDD 1.
D0	F0B	FDD 0 Busy	Same as above for FDD 0.

Result Phase Status Registers (ST0, ST1, ST2, ST3)

The result phase of a command contains bytes that hold status information. The four result phase status registers are read from the Data Register only during the result phase of certain commands. Those may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

Table 4-19. Status Register 0 (ST0)

Bit	Symbol	Name	Function
7,6	IC	Interrupt Code	00 : Normal termination of command was completed and properly executed. 01 : Abnormal termination of command. Execution of command was started but was not successfully completed. 10 : Invalid command issue. Command which was issued was never started. 11 : Internal drive ready status changed state during the drive polling mode. Only occurs after a reset.
5	SE	Seek End	When the FDC completes the Seek command, this flag is set to 1.
4	EC	Equipment Check	If Track 0 signal fails to occur after 255 step pulses (Recalibrate command), then this flag is set to 1.
3		Unused	Always 0.
2	HS	Head Select	Indicates the HDSEL (pin#: 80) status.
1,0	DS1,0	Drive Select 1,0	Indicates the logical drive status selected. 00 : Drive 0, 01 : Drive 1 10 : Drive 2, 11 : Drive 3

Table 4-20. Status Register 1 (ST1)

Bit	Symbol	Name	Function
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of a cylinder. It will be set if TC is not issued after Read or Write Data command.
6		Unused	Always 0.
5	DE	Data Error	When the FDC detects a CRC error in either ID field or data field, this flag is 1.
4	OR	Overrun	If the FDC is serviced by Host during data transfers within a certain timer interval, this flag is 1.
3		Unused	Always 0.
2	ND	No Data	Any one of the following: 1. During Read (Deleted) Data command, FDC did not find the specified sector. 2. During Read ID command, FDC cannot read the ID field without an error. 3. During Read a Track command, the FDC can not find the proper sector sequence.
1	NW	Not Writable	During Write (Deleted) Data or Format a Track command, if FDC detects a WP (pin#:76) signal from the FDD, then this flag is 1.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index hole pulse twice. 2. The FDC can not detect a data address mark or a deleted data address mark on the specified track.

Table 4-21. Status Register 2 (ST2)

Bit	Symbol	Name	Function
7		Unused	Always 0.
6	CM	Control Mark	Any one of the following: 1. During Read Data command, the FDC encounters a deleted data address mark. 2. During Read Deleted Data command, the FDC encounters a data address mark.
5	DE	Data Error	The FDC detected a CRC error in data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3	SE	Scan Equal	During Scan command, the Equal condition satisfied.
2	SN	Scan Not	During Scan command, the FDC can not find a sector on the cylinder which meets the desired condition.
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF(hex) which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 4-22. Status Register 3 (ST3)

Bit	Symbol	Name	Function
7		Unused	Always 0.
6	WP	Write Protected	Indicates the status of the WP pin.
5		Unused	Always 1.
4	T0	Track 0	Indicates the status of the TRK0 pin.
3	WP	Write Protected	Same as Bit 6
2	HS	Head Select	Same as Bit 2 of ST0.
1,0	DS 1,0	Drive Select 1,0	Same as Bit 1,0 of ST0.

Data Rate Select Register (DSR)

This write-only register is used to program the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing. The data rate is programmed via the Control Register, not the DSR. Other applications can set the data rate in the DSR. The data rate of the floppy controller is determined by the most recent write to either the DSR or CR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H which corresponds to the default precompensation setting and 250 Kbps.

D7 Software Reset: This bit behaves the same as Operations Register RESET except that this reset is self clearing.
D6 Power Down: This bit will put the controller into the Manual Low Power mode when set to one.
D5 Undefined. Should be set to zero.
D4-2 Precompensation Select: These three bits select the amount of write precompensation which the floppy controller will use on the WDATA disk interface output. Table 4-21 shows the amount of precompensation used for each bit pattern. In most cases, the default values (Table 4-22) can be used; however, alternate values can be chosen for specific types of drives and media. Track 0 is the default starting track number can be changed in the Configure command.

Table 4-23. Write Precompensation Delays

Precomp 432	Precompensation Delay
1 1 1	0.0ns — Disabled
0 0 1	41.7ns
0 1 0	83.3ns
0 1 1	125.0ns
1 0 0	166.7ns
1 0 1	208.3ns
1 1 0	250.0ns
0 0 0	Default

Table 4-24. Default Precompensation Delays

Data Rate	Precompensation Delay
1 Mbps	41.7ns
500 Kbps	125.0ns
300 Kbps	125.0ns
250 Kbps	125.0ns

D1-0 Data Rate Select 1,0 : These bits determine the data rate for the floppy controller. See Table 4-23 for the corresponding data rate for each value of D1, D0. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Table 4-25. Data Rates

Data Rate Select		Data Rate	
1	0	MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

Control Register (CR)

This register sets the data rate and is write only. This is not affected by a software reset, and is set to 250 Kbps after a hardware reset. The data rate of the floppy controller is determined by the last write to either this register or DSR.

D7-2 Reserved: Should be set to 0.
D1-0 Data Rate Select 1,0: See Table 4-23 for the appropriate values.

Operations Register (OR)

This register controls the drive select and motor, enable disk interface outputs, enables the DMA logic, and contains a software reset bit. It is set to 00H after a hardware reset, and is unaffected by a software reset.

2 Drive Select (Bit 7 of FSR is 0)

D7-6 Should be 0.
D5 Motor on enable : Inverted output MTR1 (pin# : 71) is active
D4 Motor on enable : Inverted output MTR0 (pin# : 68) is active
D3 DMA enable : Set to 1 will enable the DRQ, DACK, TC and IRQ6 pins.
Set to 0 will disable TC, DACK pins and make IRQ6, DRQ pins Hi-Z state.
D2 Software Reset : Active low software reset signal.
D1 Should be 0.
D0 Drive Select : If 0 and D4 = 1, then DS0 (pin# : 70) is active.
If 1 and D5 = 1, then DS1 (pin# : 69) is active.

4 Drive Select (Bit 7 of FSR is 1)

Table 4-26, Operations Register for 4 Drive support

Bits						Drive Pins				Encoded Functions
7	6	5	4	1	0	DS1	DS0	MTR1	MTR0	
			1	0	0	0	0	0	0	Active Drive & Motor 0
		1		0	1	0	1	0	1	Active Drive & Motor 1
	1			1	0	1	0	1	0	Active Drive & Motor 2
1				1	1	1	1	1	1	Active Drive & Motor 3

*: Bits 2 and 3 are the same as 2 Drive select.

During command or result phase, the main status register must be read by the processor before each byte of information is written into or read from the data register. Bit 6 and 7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the FDC. Many of the commands require multiple bytes, and as a result the main status register must be read prior to each byte transfer to the FDC. On the other hand, during the result phase, bit 6 and 7 in the main status register must both be 1's before reading each byte from the data register. (This reading of the main status register before each byte transfer to the FDC is required in only the command and result phases, and not during the execution phase.)

During the execution phase, the main status register need not be read. If the FDC is in the Non-DMA mode, then the receipt of each data byte (if FDC is reading data from FDD) is indicated by an interrupt signal on IRQ6 pin. The generation of a read signal will reset the interrupt as well as output the data onto the data bus. For example, if the processor cannot handle interrupt fast enough then it may poll the main status register and then bit 7 (RQM) functions just like the interrupt signal. If a Write command is in process, then the write signal performs the reset to the interrupt signal.

It is important to note that during the result phase all bytes shown in the command table must be read. The Read Data Command, for example has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

The bytes of data which are sent to the FDC to form the command phase, and are read out of the FDC in the result phase, must occur in the order shown in the command table. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No. foreshortening of the command or result phases are allowed. After the last byte of data in the command phase is sent to the FDC, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the FDC is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to TC pin. This is a convenient means of ensuring that the processor may always get the FDC's attention even if the disk system hangs up in an abnormal manner.

The FDC continues to transfer data until the TC input is active. In Non-DMA Host transfers are not the normal precedure. If the user chooses to do so, the FDC will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive NACK. In Non-DMA mode it is necessary to examine the main status register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the FDC is in the DMA mode, no interrupts are generated during the execution phase. The FDC generates DRQ's (DMA Requests) when each byte of data is available. The DMA controller responds to this request with both a DACK = 0 (DMA Acknowledge) and a RD = 0 (host read). If a Write Command has been programmed then a Host write signal will appear instead of Host read. After the execution phase has been completed (TC occurred), then an interrupt will occur (IRQ6 = 1). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically reset (IRQ6 = 0).

4.3 Serial Ports

Serial ports are completely independent. They perform serial-to-parallel conversion or parallel-to-serial conversion between a peripheral device or a MODEM and CPU.

Serial Ports Registers
Internal registers are classified by three types, that is data, status, and control registers. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The status registers are the Line Status Register and the Modem Status Register. Also the control registers are Divisor Latch LSB and Divisor Latch MSB for baudrate selection.

Line Control Register
This register decides the format of the asynchronous serial data. Figure 1. shows 1 byte serial data composition and details on each bit are described on Figure 2.

Table 4-27. Register Address NIOL = 0, AEN = 0

DLAB1	UART-CS1	A2	A1	A0	Register	
0	1	0	0	0	Receiver Buffer (Read)	U
					Transmitter Holding (Write)	A
0	1	0	0	1	Interrupt Enable	R
0	1	0	1	0	Interrupt Identification (Read)	T
0	1	0	1	0	Test Control (Write)	
X	1	0	1	1	Line Control	
X	1	1	0	0	MODEM Control	1
X	1	1	0	1	Line Status	
X	1	1	1	0	MODEM Status	
X	1	1	1	1	Scratch (Note 1)	
1	1	0	0	0	Divisor Latch (Least Significant Byte)	
1	1	0	0	1	Divisor Latch (Most Significant Byte)	
DLAB2	UART-CS1	A2	A1	A0	Register	
0	0	0	0	0	Receiver Buffer (Read)	U
					Transmitter Holding (Write)	A
0	0	0	0	1	Interrupt Enable	R
0	0	0	1	0	Interrupt Identification (Read)	T
0	0	0	1	0	Test Control (Write)	
X	0	0	1	1	Line Control	
X	0	1	0	0	MODEM Control	2
X	0	1	0	1	Line Status	
X	0	1	1	0	MODEM Status	
X	0	1	1	1	Scratch (Note 1)	
1	0	0	0	0	Divisor Latch (Least Significant Byte)	
1	0	0	0	1	Divisor Latch (Most Significant Byte)	

Note 1: This register is only present when operating in the AT mode.

Table 4-28. Summary of Registers

	Register Address											
	0 DLAB=0	0 DLAB=0	1 DLAB=0	1	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	Receiver Buffer Register (Read Only	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident Register (Read Only)	FIFO Control Register (Write) Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trading Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Camer Delect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFO3 Enableed (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFO3 Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLA3)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1.: Bit 0 is the least significant bit seriously transmitted or received.
2.: These bits are always 0 in the GM16C450 Mode.

Registers

The system programmer may be access any of the UART registers summarized in Table II via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table II has its name and reset states shown.

LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and set the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table II shows the contents of the LCR. Details on each bit follow:

Bit 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows.

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If Bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bit are generated. The Receiver checks the first Stop bit only, regardless of the number of Stop bit selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed).

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, and odd number of logic 1s is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0. If bit 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the received UART. When it is set to logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitted logic.

Note: This feature enables the CPU to alert a terminal in During the break, the Transmitter can be used as a character timer to accurately establish the break duration, a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load on all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be tored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Interrupt Enable Register

Bit 0: This bit enables the Received Data Available Interrupt. (logic 1)

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt. (logic 1)

Bit 2: This bit enables the Receiver Line Status Interrupt. (logic 1)

Bit 3: This bit enables the MODEM Status Interrupt. (logic 1)

Bit 4-7: These bits are fixed to logic 0.

This register enables the four types of UART's interrupts. Setting bits of this register to a logic 1 enables the selected interrupt. Contrary, setting bits to a logic 0, disables the interrupt.

Baud Rate Generator (BRG)

UART contains two independently programmable baud generators. The crystal oscillator frequency input is divided by 13. This is input of each Baud Generator and divided by the programmed divisor. The result frequency of the Baud Generator is 16 × baud rate, divisor number = (frequency input)/(baud rate × 16). Two 8-bit latches per channel store the divisor in a 16 bit binary format.

Test Control Register

This register is used for UART test.

Bits 0-3,6-7: These bits are reserved.

Bit 4: This bit decides whether the Baudout (TCR 4 = 1) or Sout (TCR4 = 0) signal will be used at the output pin assigned.

Bit 5: This bit is used to for checking Baud counter output to generate corresponding bits. If this bit is logic 1, IRQ and SOUT pins are equivalent to BRG LSB's down-counter Bit 0, 4, respectively. While NDTR and NRTS pins are equivalent to BRG MSB's downcounter Bit 0, 4.

Table 4-29. Divisors, Baud Rates and Clock Frequencies

Divisor Baud Rate	(24 ÷ 13) MHz clock	
	Decimal Divisor for 16 × Clock	Percent Error (Note 1)
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030

Note 1: The percent error for all Baud Rates, except where indicated otherwise, is 0.002%.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 2 to 2^{16}-1. 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 × the Baud [divisor # = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be located during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Tables III, IV and V provide decimal divisors to use with crystal frequencies of 1.8432 MHz 3.072 MHz and 8 MHz, respectively. For buad rates of 38400 and below, the error obtain is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

LINE STATUS REGISTER

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Details on each bit follow.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transfered to the FIFO.

Bit 2: This bit is the Parity Errer (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). the FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (B1) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The B1 indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently

with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the GM16C450 Mode this is a 0. In the FIFO mode LSR7 is set when there is at elast one partiy error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

FIFO CONTROL REGISTER

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCRO enables both the XMIT and RCVR FIFOs. Resetting FCRO will clear all bytes in both FIFOs. When changing from FIFO Mode to GM16C450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1 (see description to FXRDY and TXRDY pins).

Bit 4,5: FCR4 to FCR5 are reserved for future use.

Bit 6,7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table II shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bit 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table VI.

Bit 3: In the GM16C450 Mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bit 4 and 5: These two bits of the IIR are always logic 0.

Bit 6 and 7: These two bits are set when FCRO = 1.

INTERRUPT ENABLE REGISTER

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table II shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the GD75188) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the output 1 ($\overline{OUT1}$) signal, which is an auxillary user-designated output. Bit 2 affects the $\overline{OUT1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the output 2 ($\overline{OUT2}$) signal, which is an auxillary user-designated output. Bit 3 affects the $\overline{OUT2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur; the transmitter Serial Output (SOUT) is set to the Marking (logic 1) State; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was ready by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If but 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR0 = 1, IERO = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR-06), as before, has higher priority than the received data available (IIR-04) interrupt.

D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1) XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first transmitter interrupt affect changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR0 = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR0 will be set as long as there is one byte in the RCVR FIFO.
LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way when in the interrupt mode, the IIR is not affected since 1ER2 = 0.
LSR5 will indicate when the XMIT FIFO is empty.
LSR6 will indicate that both the XMIT FIFO and shift register are empty.
LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

4.4 Parallel ports

The prime3b supports IBM XT/AT compatible parallel port, the PS/2 type bi-directional parallel port, the Fast Centronics, the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) modes. Refer to prime 3b configuration register and hardware configuration description for information on power down, changing the base address of parallel port, and selecting the mode of operation.
The functionality of the Parallel Port is achieved through the use of ten addressable ports. The following Parallel Port Summary table shows the address map of all parallel port registers.

data port	base address + 00H
status port	base address + 00H
control port	base address + 00H
epp addr port	base address + 00H
epp data port 0	base address + 00H
epp data port 1	base address + 00H
epp data port 2	base address + 00H
epp data port 3	base address + 00H

IBM XT/AT BI-DIRECTIONAL MODE

THE bi-direction mode is selected in Function Selection Register(FSR) and supports centronics style standard mode and IBM PS/2 style bi-directional mode. The write operation in bi-direction mode is similar to that in standard mode except that data can be read from the parallel port. During normal write operation, the printer asserts BUSY (high) when it is not ready to receive data from the controller. When it has finished processing the data, the printer asserts nACK (low) and deasserts BUSY (low). If interrupts are enabled, deasserting nACK (high) generates an interrupt and the corresponding interrupt service routine functions as a parallel port driver. If interrupts are disabled, the parallel port software must poll the status register to determine when the nACK is pulsed. The parallel port driver outputs valid data on the printer data pins and asserts nSTROBE after an appropriate data stabilization interval. The nsTROBE is deasserted after a sufficient setup time has elapsed. Valid data can then be read from the port after a hold time has elapsed.

During read operation, data available on the parallel port bus is driven on to the system bus.

The write and read operation in bi-directional mode are concerned with Data Port Direction bit (CTR5) and are shown in the table.

Table. BI-Directional Data register read and write modes

DATA REGISTER (DTR)

This is bi-directional data port that transfers 8-bits data and is located at an offset of 00H from the base address. The reset value of this register is 0. Data written to this register is transmitted to parallel port or latch according to Data Direction bit; data read to it is the data on parallel port or latch according to Data Direction bit. This port is compatible with the IBM PC/AT parallel port.

STATUS REGISTER (STR)

This is located at an offset of 01H from the base address and is a read only. This register can be accessed in all parallel port modes. The bits of the Status Port are defined as follows:

BIT 0 TIMEOUT

This bit is valid in EPP mode only and indicates that a 10usec time out has occured on EPP operation. A logic 0 means that no time out error has occured; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET or writing a one to this bit. When not in EPP mode this bit is 0.

BIT 1, 2

These bits are reserved and always 1.

BIT 3 nERROR

This bit reflects the state of the nERROR input pin. A logic 0 means an error has been detected.

BIT 4 SLCT

This bit reflects the state of the SLCT input pin. A logic 1 indicates that printer is on-line; a logic 0 indicates that printer is not selected.

BIT 5 PE

This bit reflects the state of the PE input pin. A logic 1 means that printer is out of paper.

BIT 6 nACK

This bit reflects the state of the nACK pin. A logic 0 in-

dicates that the printer has been received a character and is ready to accept another. A logic 1 indicates that the printer is busy with the last character sent or has not received data.

BIT 7 nBUSY
This bit reflects the inverted state of the nBUSY pin. A logic 0 means that the printer is busy and cannot accept a new data. A logic 1 means that the printer is ready to accept a new data.

CONTROL REGISTER (CTR)
This is located at a offset of 02H from the base address. The reset value of this register is COH. This read/write register provides all output control signals. This register can be accessed in all parallel port modes.

BIT 0 STROBE
This bit is inverse of the nSTROBE pin and controls the data strobe output signal to printer.

BIT 1 AUTOFD
This bit is inverse of the nAUTOFD pin. A logic 1 causes the printer to generate an automatic line feed at the end of each line.

BIT 2 nINIT
This bit controls the nINIT output signal that initialize the printer. A logic 0 generates the active low pulse to intialize printer.

BIT 3 SLCTIN
This bit is inverse of the nSLCTIN pin that selects printer. A logic 1 selects the printer.

BIT 4 IRQEN
This bit is the interrupt request enable bit. When this bit is a logic 1, parallel interrupt is generated in respond to a transition of the printer nACK signal from active to inactive. Otherwise, all interrupts is disabled and all pending interrupts are cleared.

BIT 5 DIR
This bit controls the parallel port direction. A logic 0 means that the parallel port is in output mode (write) and a logic 1 means that parallel port is in input mode (read). In standard mode and fast centronics mode, this bit is always a logic 0 regardless of the state of this bit.

BIT 6, 7
These bits are reserved and always 1.

EPP MODE

The EPP mode is high speed and bi-direction protocols and selected in Function Selection Register (FSR). The EPP mode provides for greater throughput and more complexity than Compatible by supporting faster transfer times and a mechanism that allows the host to address peripheral device registers directly. The prime3b supports two EPP modes, EPP rev 1.7 and EPP rev 1.9(IEEE 1284). In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a timer is required to prevent system lock up. The timer indicates if more than 10 usec have elapsed from the start of the EPP cycle (nIOW or nIOR asserted) to nWait being deasserted (after command). If a timeout error occurs, the current EPP cycle is aborted and timeout condition is indicated in STR bit 0. This timeout error is available only in EPP rev 1.9. There are four operations: address write, address read, data write and data read. The software must write 0 to bit 0,1 and 3 of the CTR register before accessing the EPP registers because the output pins are controlled by hardware in EPP operation and set the Data Direction bit (bit 5 of CTR) to control direction.

CONTROL REGISTER
This register is same as CTR in Bi-Direction mode

STATUS REGISTER
This register is same as STR in Bi-Direction mode

EPP ADDRESS REGISTER (eppAddr)
This is located at an offset of 03H from the base address. This is cleared at initialization by RESET. During a WRITE operation, D<7:0> are buffered and output on to the PD<7:0>, the leading edge of nIOW cause an EPP ADDRESS WRITE cycle to be performed, the trailing edge of nIOW latchs the data for duration of the EPP WRITE cycle. During a READ operation, PD<7:0> are read, the leading edge of nIOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the inacive of nADSTRB latches the PD<7:0> for the duration of the nIOR cycle. This register is only available in EPP mode.

EPP DATA REGISTER (eppData)
This is located at an offset of 04H from the base address. This is cleared at initialization by RESET. During a WRITE operation, D<7:0>, the leading edge of nIOW cause an EPP DATA WRITE cycle to be performed, the trailing edge of nIOW latchs the data for duration of the EPP WRITE cycle.
During a READ operation, PD<7:0> are read, the leading edge of nIOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the inacive of nDASTRB latches the PD<7:0> for the duration of the nIOR cycle. This register is only available in EPP mode.

DATA (0x000 Modes 000,001)
This is the standard parallel port data register and same as DTR register.

ecpAFifo (0x000 Mode 011)
A byte written to this register is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port will transmit this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0).

DSR (0x001 Modes all)
This read-only register reflects the inputs on the parallel port interface and same as STR. This register can be accessed in all modes.

DCR (0x002 Modes all)
This register directly controls several output signals as well as enabling some functions and same as CTR. This register can be accessed in all modes.

cFifo (0x400 Mode 010)
Bytes written by PIO or DMA from the system to this FIFO are transmitted by hardware handshake to the peripheral using the standard parallel protocol. This mode is only defined for forward direction.

ecpDFifo (0x400 Mode 011)
When direction is forward, Bytes written by PIO or DMA from the system to this FIFO are transmitted by hardware handshake to the peripheral using the ecp forward parallel protocol.
When direction is backward, Bytes from the peripheral are read by hardware handshake from ECP into this FIFO using the ecp forward parallel protocol. Data read from FIFO by PIO or DMA will return bytes of ECP data to the system.

eppAddr (0x003 Mode 100)
This register can be accesed only when the ecpepp bit of ECP register is enabled and same as previous defined epp Address register in EPP mode.

eppData (0x004:7 Mode 100)
This register can be accesed only when the ecpepp bit of ECP register is enabled and same as previous defined epp data registers in EPP mode.

EPP DATA REGISTER2 (eppData2)
This is located at an offset of 05H from the base address. Refer to EPP DATA REGISTER1 for a description of operation.

EPP DATA REGISTER3 (eppData3)
This is located at an offset of 06H from the base address. Refer to EPP DATA REGISTER1 for a description of operation.

EPP DATA REGISTER4 (eppData4)
This is located at an offset of 07H from the base address. Refer to EPP DATA REGISTER1 for a description of operation.

EPP OPERATION

The EPP rev type is selected via bit 4 of ECP register: When the bit is 0, EPP 1.9 is selected, when the bit is 1, EPP 1.7 is selected.

EPP 1.7 Address Write
The following procedure selects a peripheral device or register.
1. The host writes a byte to the EPP address register. nIOW gose low to latch D<7:0> into the address register. The latched data is onto the PD<7:0> and EPP drives nWRITE low.
2. The EPP asserts nASTRB (low) to indicate that data has been sent.
3. It nWait is low during the host write cycle. IOCHRDY goes low. When nWAIT goes high, the EPP drives IOCHRDY high. If nWAIT is high during host write cycle, the EPP dose not pull IOCHRDY to low.
4. When IOCHRDY goes high it cause nIOW to go high.
5. When nIOW goes high it cause the EPP to pull nWRITE and nASTRB to high. Only when nWRITe and nASTRB are high can the EPP change PD<7:0>.

EPP 1.7 Address Read
The following procedure reads from the address register.
1. The host reads a byte from the EPP address register. nIOR goes low to gate PD<7:0> into D<7:0>.
2. The EPP drives nASTRB low the peripheral to start sending data.
3. If nWait is low during the host read cycle, IOCHRDY goes low. When nWAIT goes high, the EPP drives IOCHRDY high. If nWAIT is high during host write cycle, the EPP dose not pull IOCHRDY to low.
4. When IOCHRDY goes high it cause nIOW to go high.
5. When nIOW goes high it cause the EPP to pull nWRITE and nASTRB to high. Only when nWRITE and nASTRB are high can the EPP change PD<7:0>.

EPP 1.7 Data Write and Data Read
This procedure writes to or read from the selected peripheral device or register. An EPP 1.7 Data write operation is similar to the EPP 1.7 address write operation except that the data strobe (nDSTRB) and data register replace the address strobe (nASTRB) and address register respectively.

EPP 1.9 Address Write
1. The host writes a byte to address register and drives nIOW low.
2. The EPP drives IOCHRDY low.
3. If nWAIT is not asserted, the chip must wait until nWAIT is asserted. If nWAIT was already low, step 2 and 3 occur concurrently.
4. The EPP places address onto PD<7:0> and asserts nWRITE.

5. The EPP drives nASTRB low to indicate that PD<7:0> is a valid data and waits for nWAIT to go high.
6. The peripheral deasserts nWAIT (low) to indicate that it is ready to receive the address byte.
7. The EPP deasserts nASTRB and drives IOCHRDY high allowing the host to complete the write cycle.
8. The peripheral asserts nWAIT, indicating to the host that it is ready for the next cycle.
9. The EPP can then modify the nWRITE and address on the PD<7:0>.

EPP 1.9 Address Read
1. The host reads a byte from address register and drives nIOW low.
2. The EPP drives IOCHRDY low.
3. If nWAIT is not asserted, the chip must wait until nWAIT is asserted. If nWAIT was already low, step 2 and 3 occur concurrently.
4. The EPP tri-states the PD<7:0> and drives nWRITE high.
5. The EPP asserts nASTRB indicating that PD<7:0> is tri-stated, PDIR is set and the nWRITE signal is valid.
6. The peripheral drives PD<7:0> valid.
7. The peripheral deasserts nWAIT, indicating that PD<7:0> is valid.
8. The EPP latches the data from the PD<7:0> for D<7:0> and deasserts nASTRB and IOCHRDY allowing the host to complete the read cycle.
9. The peripheraltri-states the PD<7:0> and asserts nWAIT, indicating to the host that the PD<7:0> is tri-stated.
10. The EPP can modify nWRITE, PDIR and PD<7:0> in preparation for next cycle.

EPP 1.9 Data Write and Data Read
An EPP 1.9 data write operation is similar to the EPP 1.9 address write operation except that the data strobe (nDSTRB) and data register replace the address strobe (nASTRB) and address register respectively.

ECP MODE

The ECP mode is another high-speed bidirectional protocol that is implemented in hardware to reduce software and system overhead.
The ECP mode provides a DMA operation, a 16-byte FIFO, bidirectional command/data transfer, command/data FIFO tag (one per byte), a FIFO threshold interrupt for both directions, FIFO full and full status bits, automatic generation of strobes by hardware to fill or empty the FIFO and a Run Length Encoding (RLC) as explained below.
The ECP mode is selected in Function Selection Register (FSR). Once selected, its mode is controlled via the mode field of bit 5, 6, 7 of ECR register.
The ECP mode in prime3b has 15 registers and the registers are shown in below table.

Register definition
The register definitions are based on the standard printer address for LPT. All of standard modes are supported in ECP mode. The port register vary depending on the mode field in the ECR. The table below lists these dependencies.

Table ECP Register Definitions

data	+000h R/W	000-001	data register
eppAfifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	ALL	status register
dcr	+002h R/W	ALL	control register
cFIFO	+400h R/W	010	parallel port data fifo
ecpDfifo	+400h R/W	011	ECP FIFO (DATA)
tFIFO	+400h R/W	110	TEST FIFO
cnfgA	+400 h R	111	configuration register A
cnfgB	+401h R/W	111	configuration register B
ecr	+402h R/W	ALL	extended control register

Table Mode Descriptions

MODE	DESCRIPTION
000	SPP mode
001	PS/2 parallel mode
010	parallel port data fifo mode
011	ecp mode
100	epp eode (if this option is enable in the configuration register)
101	(reserved)
110	test mode
111	configuration mode

tFifo (0x400 mode 110)
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be derermined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntr Threshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Ox400 Mode 111)
This configuration register is a read only register. When read, 10h is returned. This indicates to the system that this is an 8-bit implementation.

cnfgB (Ox401 Mode 111)
This configuration register is a read only register.

BIT 0-5
These bits are reserved and always 0.

BIT 6
This bit returns the value on the ISA irq line to determine possible conflicts.

ECR (Ox402 Model all)
BITS 7, 6, 5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.

O: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. this prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware, it must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn = 1:
During DMA (this bit is set to a 1 when terminal count is reached).
case dmaEn = 0 direction = 0:
This bit shall be set to 1 whenever there are writeIntrThreshold or more free in the FIFO.
case dmaEn = 0 direction = 1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

OPERATION

Mode Switching/Software Control

Software will exceute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 44
Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D (6:0)
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression

Prime 3B supports Run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count in written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundry. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section.) Single byte wide transfers.

DMA TRANSFER

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting $\overline{\text{PDACK}}$ and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until $\overline{\text{PDACK}}$ is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode-Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by $\overline{PDACK}$), indicating that no more data is required. PDRQ goes inactive after $\overline{PDACK}$ goes active for the last byte of a data transfer (or on the active edge of $\overline{IOR}$, on the last byte, if no edge is present on $\overline{PDACK}$). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle.)

Interrupts

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when:

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC is received.
2. For Programmed I/O:
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b. (1) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.
3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The Fifo threshold is fixed by 8 and supported only in mode 010 and 011. Each data byte is transferred to FIFO by PIO cycle or DMA. Automatic data transfer is achived using FIFO.

Programmed I/O MODE or NON-DMA MODE

The ECP or Fast Centronics mode may also be operated using interrupt driven programmed I/O. In Prime3B WriteIntrThreshold and ReadIntrThreshold are fixed to 8 byte.

Programmed I/O transfer are to the ecpDFifo and ecpAFifo or from ecpDFifo, or to/from the tFifo. To use the PIO transfers, the host first sets up direction and state and sets dmaEN to 0 and serviceintr to 0.

The ECP requests PIO transfers from the host by activating the PINTR pin. The PIO will empty or fill the FIFO using appropriate direction and mode.

Transfer from the HOST to the FIFO

In the forward direction an interrupt occurs when service interrupt is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with WriteIntrThreshold bytes. If an interrupt occurs the host must respond to the request by writing data to the FIFO.

Transfer from the FIFO to the HOST

In the backward direction an interrupt occurs when service interrupt is 0 and there are readIntrThreshold or more bytes are available in the FIFO. At this time if the FIFO is full it can be emptied completely in a single burst. Otherwise it may be filled with WriteIntrThreshold bytes. If an interrupt occurs the host must respond to the request by reading data from the FIFO.

ECP FORWARD (WRITE) OPERATION

1. An ECP write cycle starts when the ECP drives the popped tag onto nAFD and the popped byte onto PDΠ7:0⊃.
2. When BUSY is low, the ECP asserts nSTROBE and waits for BUSY to be high.
3. When BUSY is high the ECP deasserts nSTROBE.
4. The ECP may change nAFD and PDΠ7:0⊃ in preparation for next cycle when BUSY is low.

ECP BACKWARD (read) OPERATION

1. An ECP read cycle starts when the ECP drives nAFD low.
2. The peripheral device drives BUSY high for a normal data read cycle, or drives BUSY low for a command read cycle and drives the byte to be read onto PDΠ7:0⊃.
3. When nACK is asserted the ECP reads the PDΠ7:0⊃ and drives nAFD high.
4. When nAFD is high the peripheral device deasserts nACK and may change BUSY and PDΠ7:0⊃ in preparation for the next cycle.

4.5 Hard Disk Interface

The Prime2D supports Integrated Drive Electronics (IDE) hard disk interface. It has four control output signals ($\overline{\text{IDEHI}}$, $\overline{\text{IDELO}}$, $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$), one status input signal ($\overline{\text{IOCS16}}$).
IDEHI enables the upper data lines (D15-D8) for 16 bit read or write operations at address 1FO-1F7 IDELO enables the lower data lines (D7-D0) for 1FO-1F7 read or write, and for 3F6 write or 3F7 read.
$\overline{\text{HCS0}}$ output is active low when I/O address 1F0-1F7 is chosen. The $\overline{\text{HCS1}}$ output is active low when address 3F6 or 3F7 is chosen (See Table 4-6 and 4-13).

5. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	−0.5 ~ 7	V
T_{OP}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−65 ~ +165	°C
V_{SS}	All input and Output Voltages with respects to V_{SS}	−0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1	W

6. DC Electrical Characteristics

(V_{DD} = 5V ± 5% V_{SS} = 0V)

Symbol	Parameter	Conditions	User Spec		Units
			Min	Max	
V_{IH}	High Level Input Voltage	XIN = 3.5 (Min)	2.0	V_{DD}	V
V_{IL}	Low Level Input Voltage	XIN = 1.5 (Max)	−0.5	0.8	V
I_{CC}	Average V_{DD} Supply Current	V_{DD} = 5.25V, No loads on the Outputs; $\overline{RD}$, $\overline{WR}$, $\overline{SIN}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2V All Other Inputs = 0.0V or 5.0V DIVISOR = 0002 (Hex)		50	mA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$		10	μA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$ to 0.8V	−10		μA

*Input hysterisis pins:
$\overline{TRK0}$ $\overline{INDEX}$, $\overline{WP}$, $\overline{UPWRDWN}$, SIN1-2, $\overline{RI1\text{-}2}$, $\overline{DSR1\text{-}2}$, $\overline{DCD1\text{-}2}$, $\overline{CTS1\text{-}2}$, $\overline{DSKCHG}$, $\overline{RDATA}$

6.1 Disk Drive Interface Pins

($\overline{WE}$, $\overline{STEP}$, DENSEL, $\overline{WDATA}$, DIR $\overline{DR0\text{-}1}$, $\overline{MTR0\text{-}1}$, $\overline{HDSEL}$)

V_{OL}	Low Level Output Voltage	I_{OUT} = 40mA		0.4	V

(DRATE0-1)

V_{OH}	Output High Voltage	I_{OH} = −8mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V

6.2 All Other Output Pins

V_{OH}	Output High Voltage	I_{OH} = −12mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12mA		0.4	V

7. AC ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+ 70°C$, $V_{DD} = +5V \pm 5\%$)

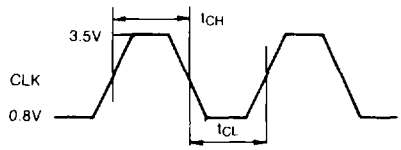
Symbol	Parameter	Conditions	Min	Max	Units
CPU INTERFACE					
t_{AR}	Delay from Address to $\overline{RD}$		19		ns
t_{AW}	Delay from Address to $\overline{WR}$		19		ns
t_{CH}	Duration of Clock High Pulse	External Clock (5M)	90		ns
t_{CL}	Duration of Clock Low Pulse	External Clock (5M)	90		ns
t_{DH}	Data Hold Time		10		ns
t_{DS}	Data Setup Time		19		ns
t_{HZ}	$\overline{RD}$ to Floating Data Delay	(Note 1)	13	25	ns
t_{MR}	Master Reset Pulse Width		100		ns
t_{RA}	Address Hold Time from $\overline{RD}$		0		ns
t_{RC}	Read Cycle Update		36		ns
t_{RD}	$\overline{RD}$ Strobe Width		60		ns
t_{RVD}	Delay from $\overline{RD}$ to Data			40	ns
t_{WA}	Address Hold Time from $\overline{WR}$		0		ns
t_{WC}	Write Cycle Update		36		ns
t_{WR}	WR Strobe Width		60		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		115		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		115		ns

Note 1: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 2: All AC timings can be met with current loads that don't exceed 3.2 mA or $-80\ \mu A$ at 100 pF capacitive loading.

Note 3: For capacitive loads that exceed 100 pF the following typical derating factors should be used:
100 pF < Cl ≤ 150 pF, t = (0.1ns/pF) (Cl-100 pF) typical
150 pF < Cl ≤ 200 pF, t = (0.08ns/pF) (Cl-100 pF) and
t = (0.5ns/mA) (Isink mA) or
t = −(0.5ns/mA) (Isource mA)
Isource is always negative, Isink ≤ 4.8 mA, Isource ≤ $-120\mu A$, Cl ≤ 250 pF

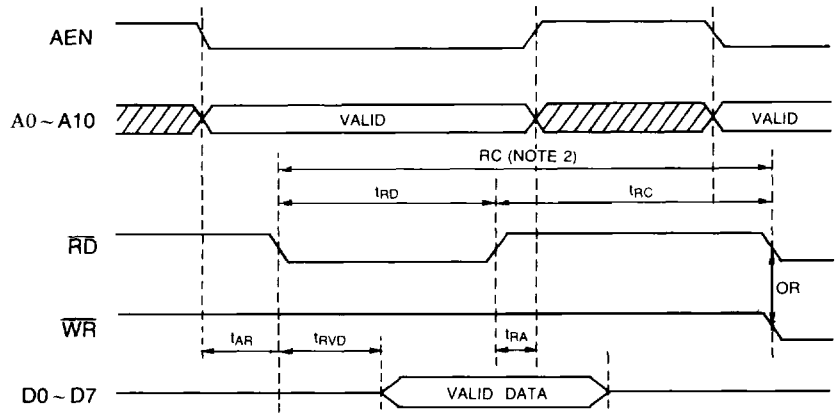
7.1 External Clock Input (24 MHz)



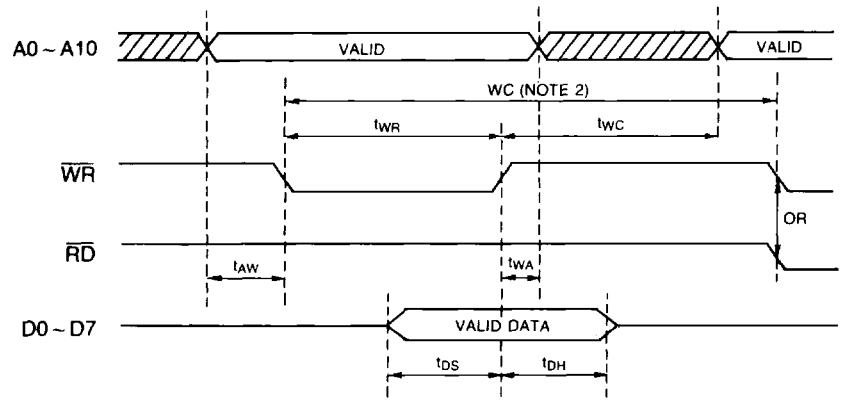
Note 1: The 3.5V and 1.5V levels are the voltages that the inputs are driven to during AC testing.

7.2 CPU Interface

Read Cycle



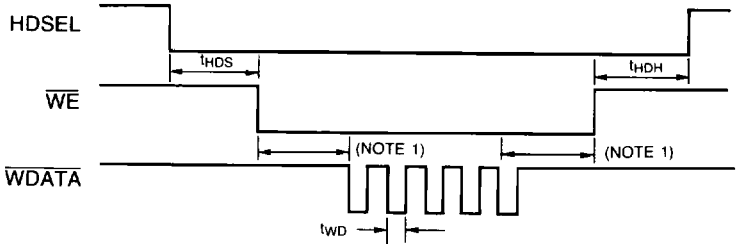
Write Cycle



7.3 Drive Write Timing

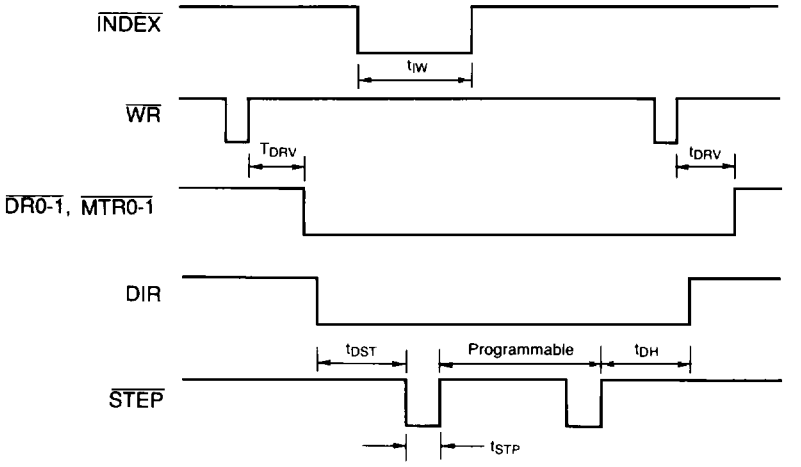
Symbol	Parameter	Conditions	Min	Max	Units
t_{WD}	Write Data Pulse Width	250kb/s (MFM)	500		ns
t_{HDS}	Head Select Setup to Write Assertion		40		μs
t_{HDH}	Head Select Hold from $\overline{WE}$		12		μs
		300kb/s (MFM)	416		ns
		500kb/s (MFM)	250		ns
		1000kb/s (MFM)	125		ns

Note 1: Whenever $\overline{WE}$ is asserted the $\overline{WDATA}$ line is active. At the end of each write one dummy byte is written before $\overline{WE}$ is deasserted.



7.4 Drive Track Access Timing

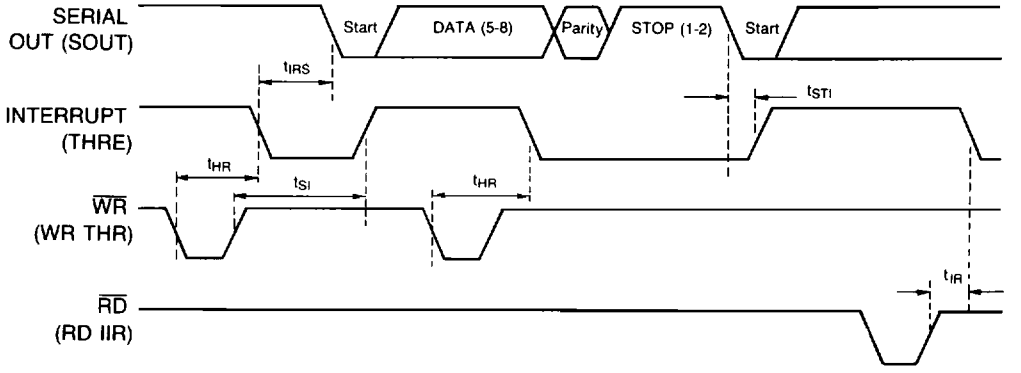
Symbol	Parameter	Min	Max	Units
t_{DH}	Direction Hold from End of Step	1 Step Time		
t_{DRV}	Drive Select or Motor Time from Write Strobe		100	ns
t_{DST}	Diection Setup prior to Step	6		μs
t_{IW}	Index Pulse Width	100		ns
t_{STP}	Step Pulse Width	6		μs



7.5 Transmitter

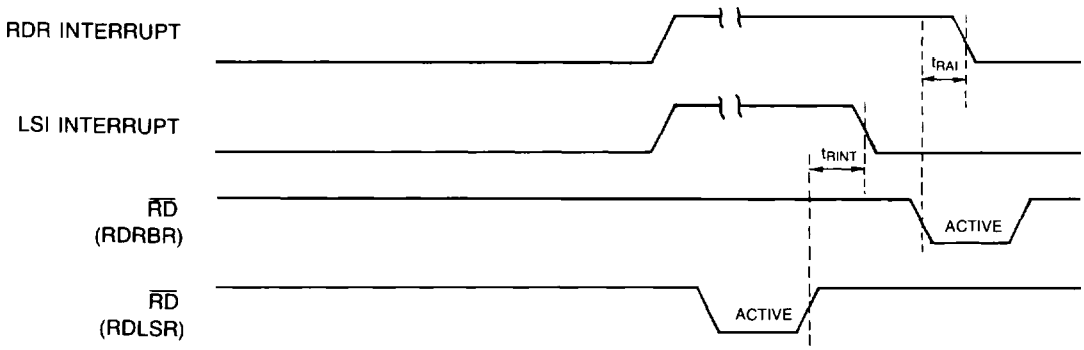
Symbol	Parameter	User Spec		Units
		Min	Max	
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset Interrupt		175	ns
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt	16	32	BAUDOUT Cycles
t_{STI}	Delay from Start to Interrupt (THRE)		8	BAUDOUT Cycles
t_{SXA}	Delay from start to TXRDY active		8	BAUDOUT Cycles
t_{WXI}	Delay from Write to TXRDY inactive		195	ns

Transmitter Timing



7.6 Receiver

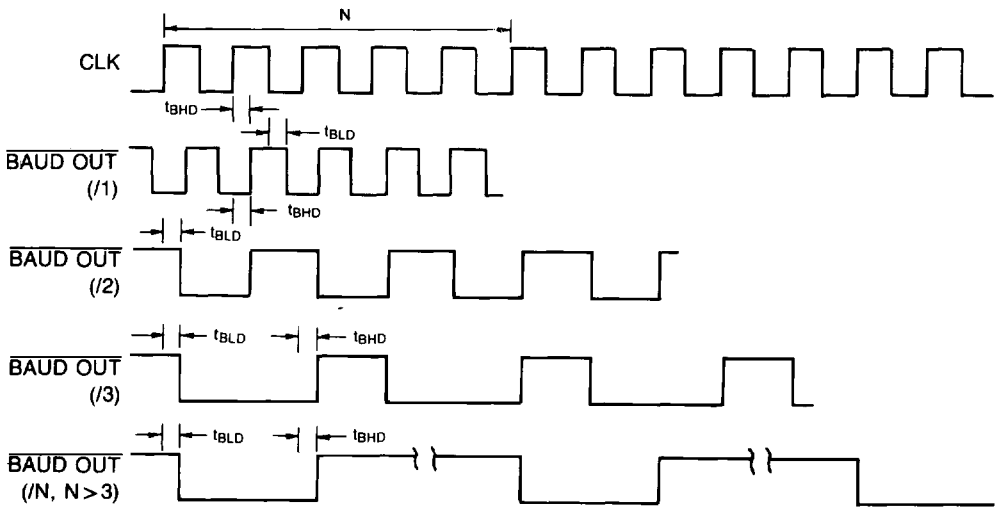
Symbol	Parameter	User Spec		Units
		Min	Max	
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset Interrupt		1	us
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset Interrupt		1	us



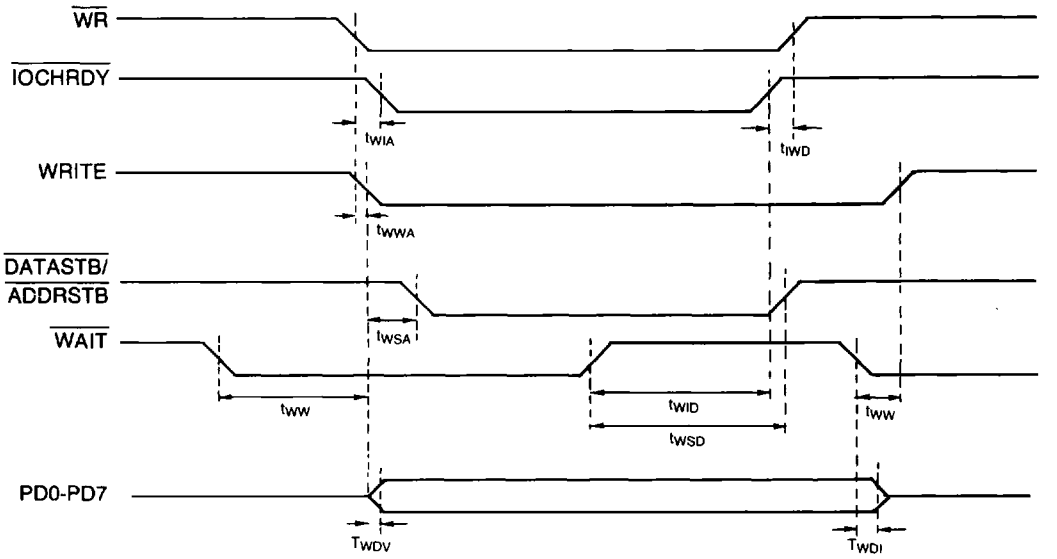
7.7 Serial Interface Baud Generator

Symbol	Parameter	User Spec		Units
		Min	Max	
N	Baud Divisor	1	2^{16}-1	
t_{BHD}	Baud Output Positive Edge Delay		56	ns
t_{BLD}	Baud Output Negative Edge Delay		56	ns

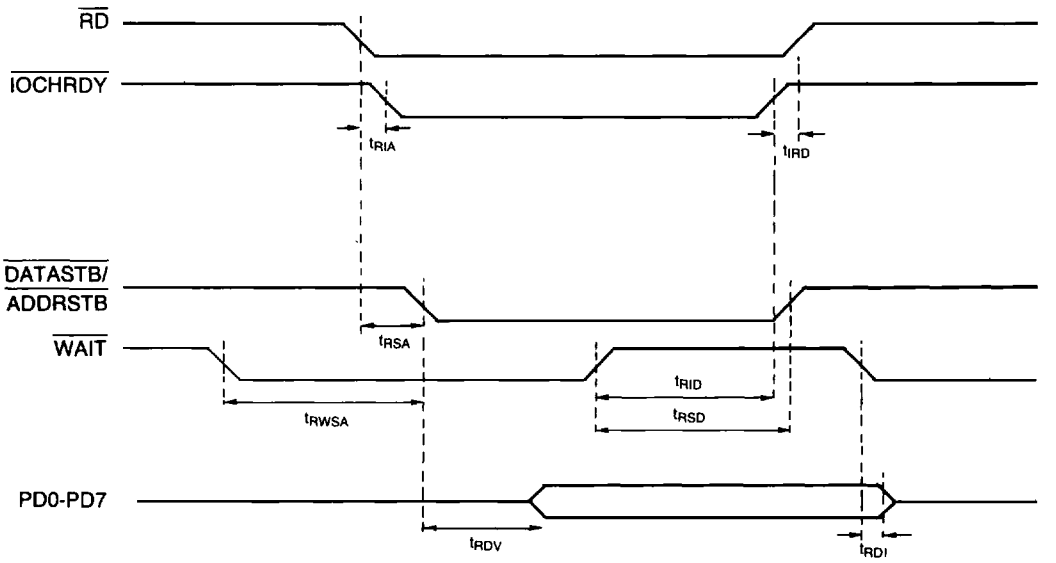
Baudout Timing



7.8 EPP Write Cycle



EPP Read Cycle

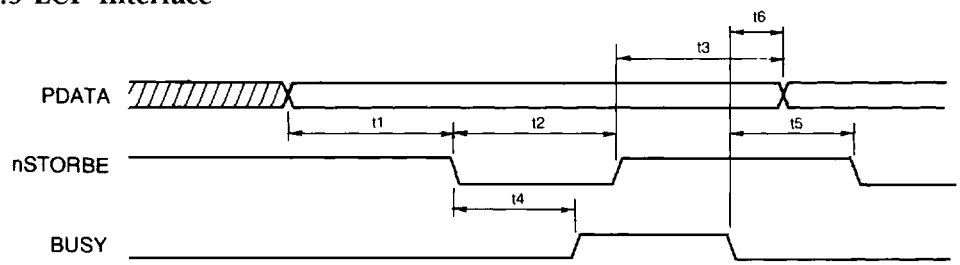


EPP

Symbol	Parameter	User Spec		Units
		Min	Max	
t_{WIA}	$\overline{WR}$ asserted to $\overline{IOCHRDY}$	0	24	ns
t_{WWA}	$\overline{WR}$ asserted to $\overline{WRITE}$	0	50	ns
t_{WSA}	$\overline{WRITE}$ asserted to $\overline{DATASTB}$/$\overline{ADDRSTB}$	5	30	ns
t_{WDV}	PD valid to $\overline{WRITE}$ asserted	0	24	ns
t_{IWD}	$\overline{IOCHRDY}$ deasserted to $\overline{WR}$	0	24	ns
t_{WID}	$\overline{WAIT}$ deasserted to $\overline{IOCHRDY}$	60	155	ns
t_{WW}	$\overline{WAIT}$ deasserted to $\overline{WRITE}$	60	155	ns
t_{WSD}	$\overline{WAIT}$ deasserted to $\overline{DATASTB}$/$\overline{ADDRSTB}$	60	155	ns
t_{WDI}	PD invalid to $\overline{WAIT}$ deasserted	60	155	ns
i_{RIA}	$\overline{RD}$ asserted to $\overline{IOCHRDY}$	0	24	ns
t_{RSA}	$\overline{RD}$ asserted to $\overline{DATASTB}$/$\overline{ADDRSTB}$	0		ns
t_{RDV}	PD valid to $\overline{DATASTB}$/$\overline{ADDRSTE}$ asserted	0		ns
t_{IRD}	$\overline{IOCHRDY}$ deasserted to $\overline{RD}$	0		ns
t_{RID}	$\overline{WAIT}$ deasserted to $\overline{IOCHRDY}$	60	155	ns
t_{RSD}	$\overline{WAIT}$ deasserted to $\overline{DATASTB}$/ $\overline{ADDRSTB}$	60	155	ns
t_{RDI}	PD invalid to $\overline{WAIT}$ deasserted	0		ns
t_{RWSA}	$\overline{WAIT}$ asserted to $\overline{DATASTB}$/ $\overline{ADDRSTB}$	60	155	ns

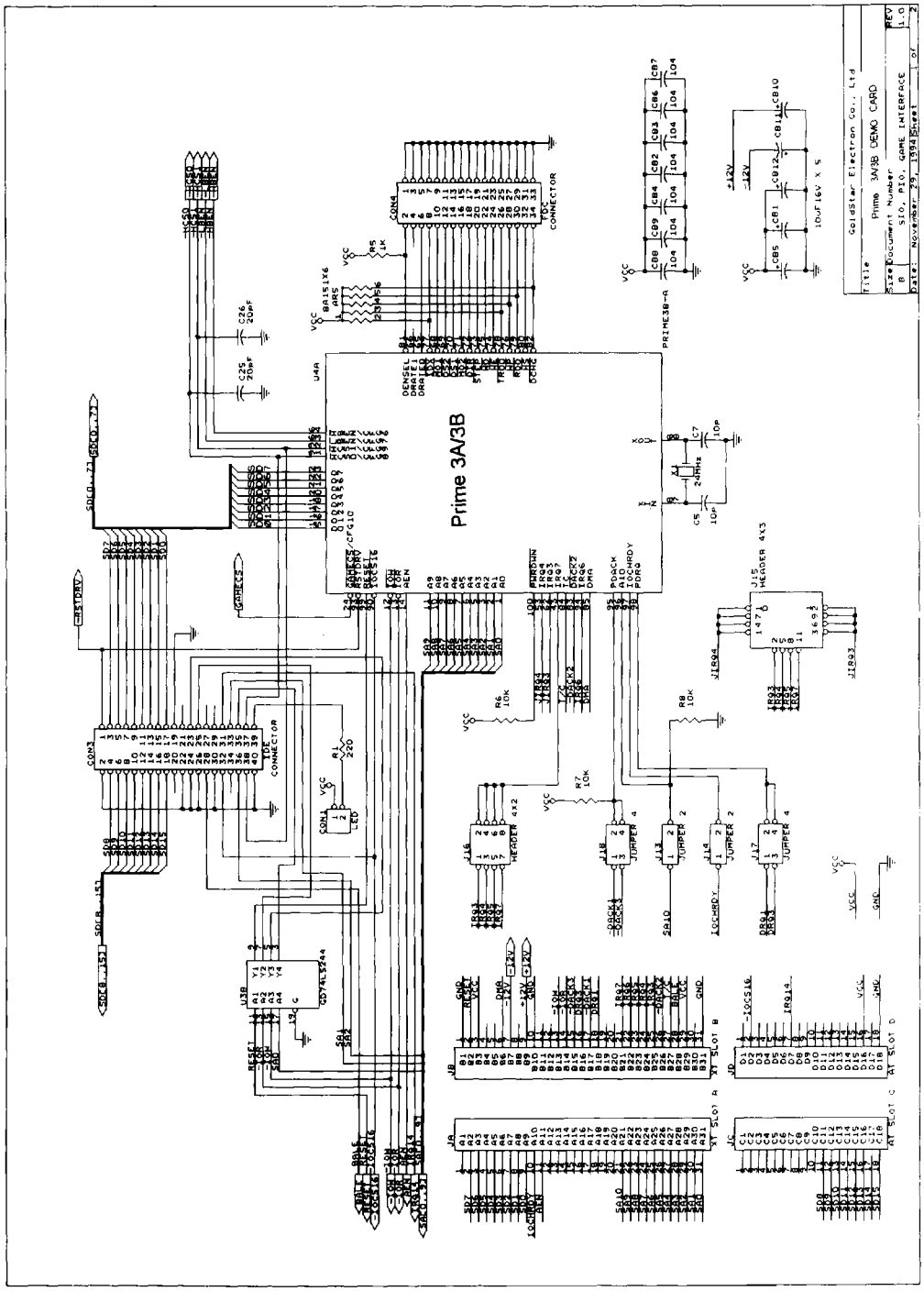
Signal Name	Pin Name
$\overline{WRITE}$	$\overline{STROBE}$
$\overline{DATASTB}$	$\overline{AFD}$
$\overline{ADDRSTB}$	$\overline{SLIN}$
$\overline{WATE}$	BUSY

7.9 ECP Interface



	Parameter	min	max	units	Notes
t1	DATA Valid to nSTROBE Active	600		ns	
t2	nSTROBE Active Pulse Width	600		ns	
t3	DATA Hold from nSTROBE Inactive	450		ns	1
t4	nSTROBE Active to BUSY Active		500	ns	
t5	BUSY Inactive to nSTROBE Active	680		ns	
t6	BUSY Inactive to PDATE Invalid	80		ns	1

* The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.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Date: November 29, 1994
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HEADER 4X2
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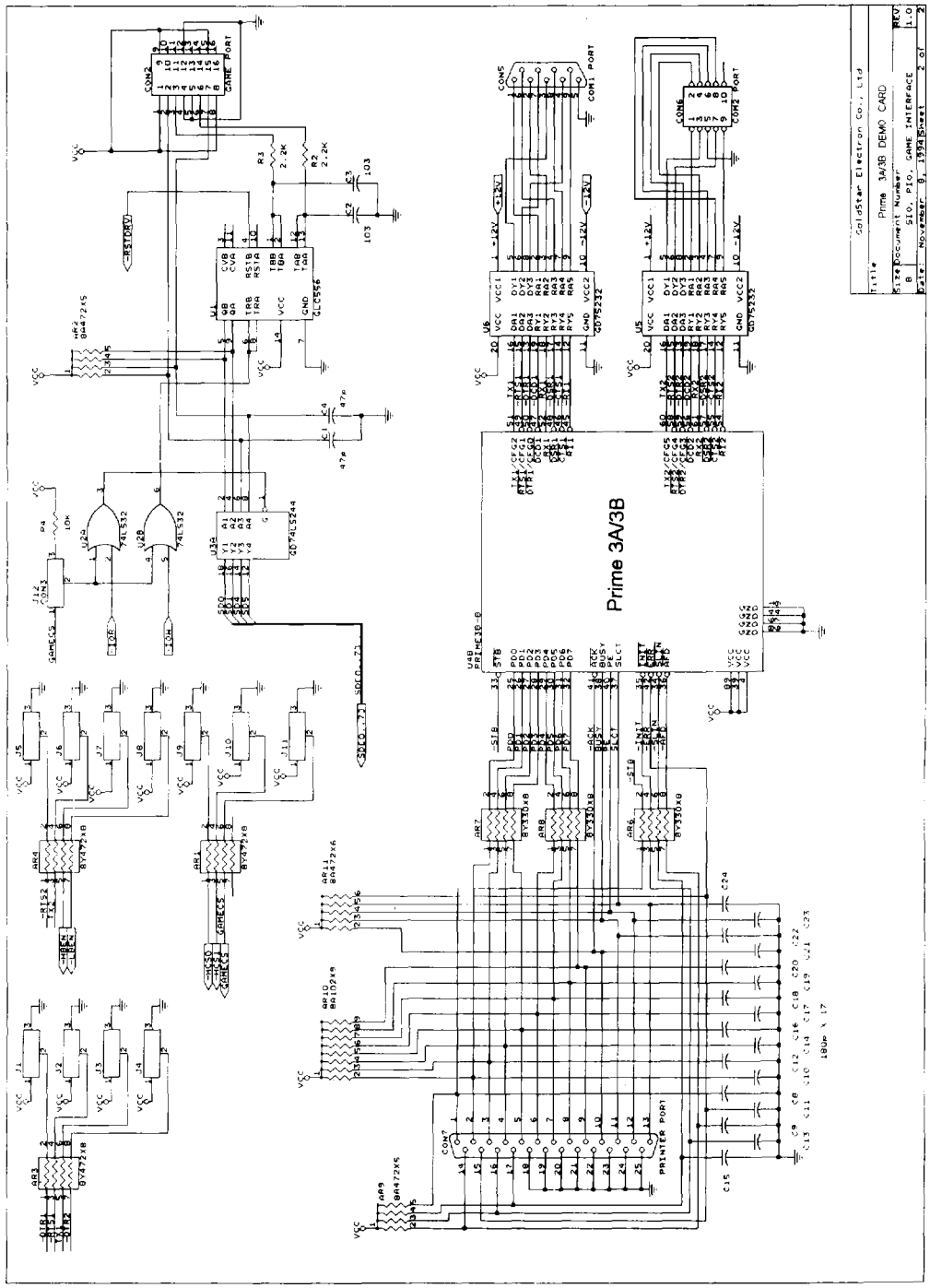
JUMPER 2
LED
AT SLOT A
AT SLOT B
AT SLOT C
AT SLOT D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SIO, PIO, GAME INTERFACE
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GAME PORT
PRINTER PORT
COM1 PORT
COM2 PORT