

**16M x 4-Bit Dynamic RAM
(4k & 8k Refresh, EDO-version)**

**HYB 3164405J/T(L) -50/-60
HYB 3165405J/T(L) -50/-60**

Preliminary Information

- 16 777 216 words by 4-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
 - RAS access time:
 - 50 ns (-50 version)
 - 60 ns (-60 version)
 - Cycle time:
 - 84 ns (-50 version)
 - 104 ns (-60 version)
 - CAS access time:
 - 13 ns (-50 version)
 - 15 ns (-60 version)
- Hyper page mode (EDO) cycle time
 - 20 ns (-50 version)
 - 25 ns (-60 version)
- Single + 3.3 V ($\pm 0.3V$) power supply
- Low power dissipation
 - max. 396 active mW (HYB 3164405J/T(L)-50)
 - max. 360 active mW (HYB 3164405J/T(L)-60)
 - max. 504 active mW (HYB 3165405J/T(L)-50)
 - max. 432 active mW (HYB 3165405J/T(L)-60)
 - 7.2 mW standby (TTL)
 - 720 W standby (MOS)
 - 14.4 mW Self Refresh (L-version only)
- Read, write, read-modify-write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh (CBR),
RAS-only refresh, hidden refresh and self refresh modes
- Hyper page mode (EDO) capability
- 8192 refresh cycles/128 ms , 13 R/ 11C addresses (HYB 3164405J/T(L))
- 4096 refresh cycles/ 64 ms , 12 R/ 12C addresses (HYB 3165405J/T(L))
- Plastic Package:

P-SOJ-34-1	500 mil	HYB 3164(5)400J
P-TSOPII-34-1	500 mil	HYB 3164(5)400T

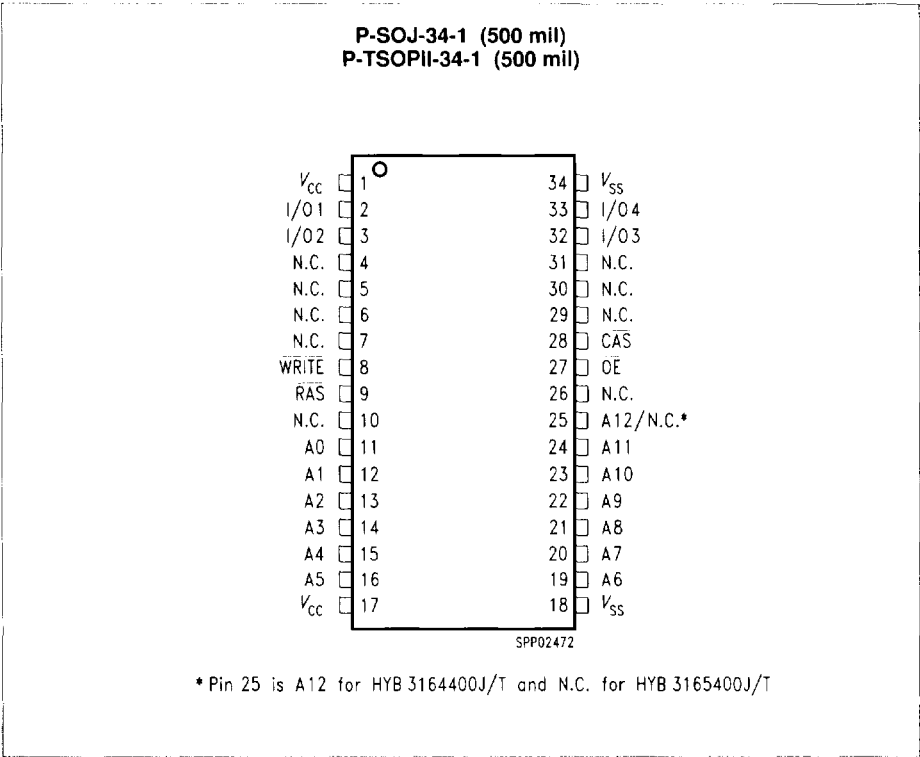
This HYB3164(5)405 is a 64 MBit dynamic RAM organized 16 777 216 by 4 bits. The device is fabricated in SIEMENS/IBM most advanced first generation 64Mbit CMOS silicon gate process technology. The circuit and process design allow this device to achieve high performance and low power dissipation. The HYB3164(5)405 operates with a single 3.3 +/-0.3V power supply and interfaces with either LVTTTL or LVCMOS levels. Multiplexed address inputs permit the HYB 3164(5)400J/T to be packaged in a 500mil wide SOJ-34 or TSOP-34 plastic package. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. The HYB3164(5)405TL parts have a very low power „sleep mode“ supported by Self Refresh.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3164405J-50	on request	P-SOJ-34-1 500 mil	DRAM (access time 50 ns)
HYB 3164405J-60	on request	P-SOJ-34-1 500 mil	DRAM (access time 60 ns)
HYB 3164405T-50	on request	P-TSOPII-34-1 500 mil	DRAM (access time 50 ns)
HYB 3164405T-60	on request	P-TSOPII-34-1 500 mil	DRAM (access time 60 ns)
HYB 3164405TL-50	on request	P-TSOPII-34-1 500 mil	DRAM (access time 50 ns)
HYB 3164405TL-60	on request	P-TSOPII-34-1 500 mil	DRAM (access time 60 ns)
HYB 3165405J-50	on request	P-SOJ-34-1 500 mil	DRAM (access time 50 ns)
HYB 3165405J-60	on request	P-SOJ-34-1 500 mil	DRAM (access time 60 ns)
HYB 3165405T-50	on request	P-TSOPII-34-1 500 mil	DRAM (access time 50 ns)
HYB 3165405T-60	on request	P-TSOPII-34-1 500 mil	DRAM (access time 60 ns)
HYB 3165405TL-50	on request	P-TSOPII-34-1 500 mil	DRAM (access time 50 ns)
HYB 3165405TL-60	on request	P-TSOPII-34-1 500 mil	DRAM (access time 60 ns)

Pin Names

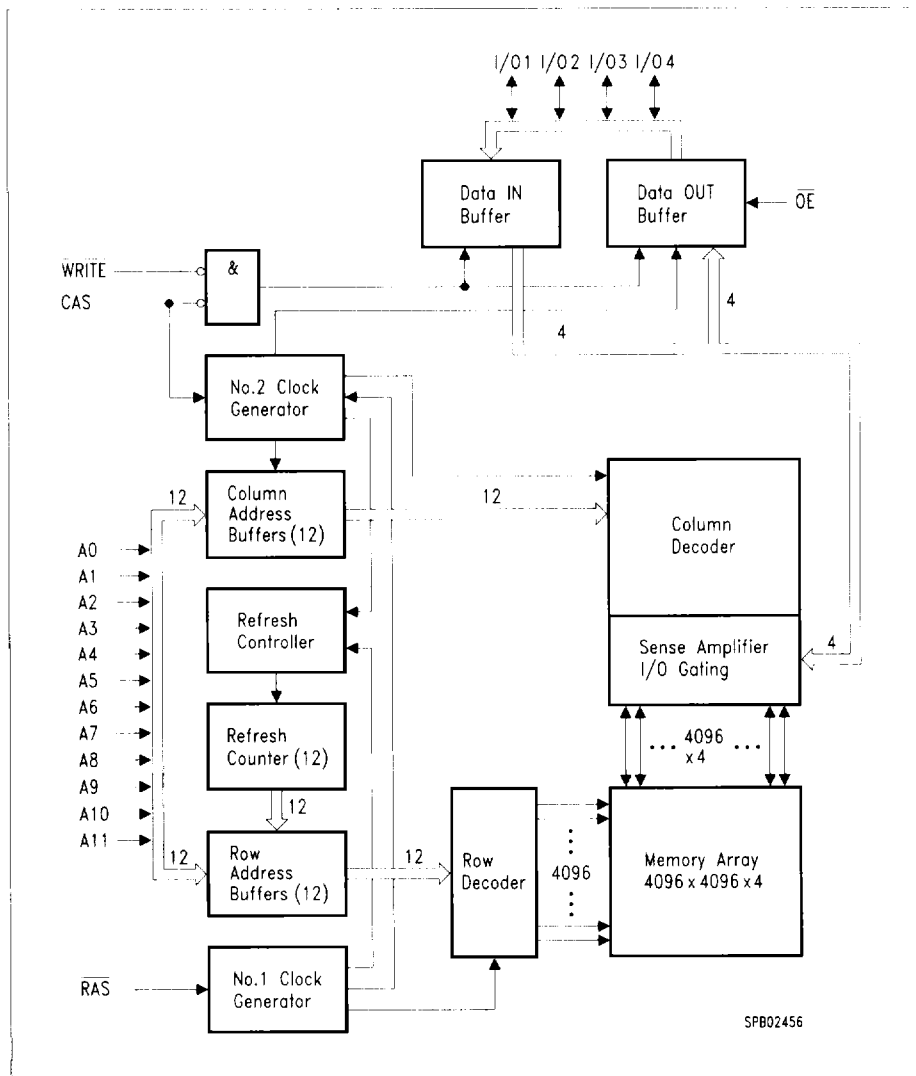
A0-A12	Address Inputs for HYB 3164405J/T(L)
A0-A11	Address Inputs for HYB 3165405J/T(L)
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WRITE}}$	Read/Write Input
Vcc	Power Supply (+ 3.3V)
Vss	Ground



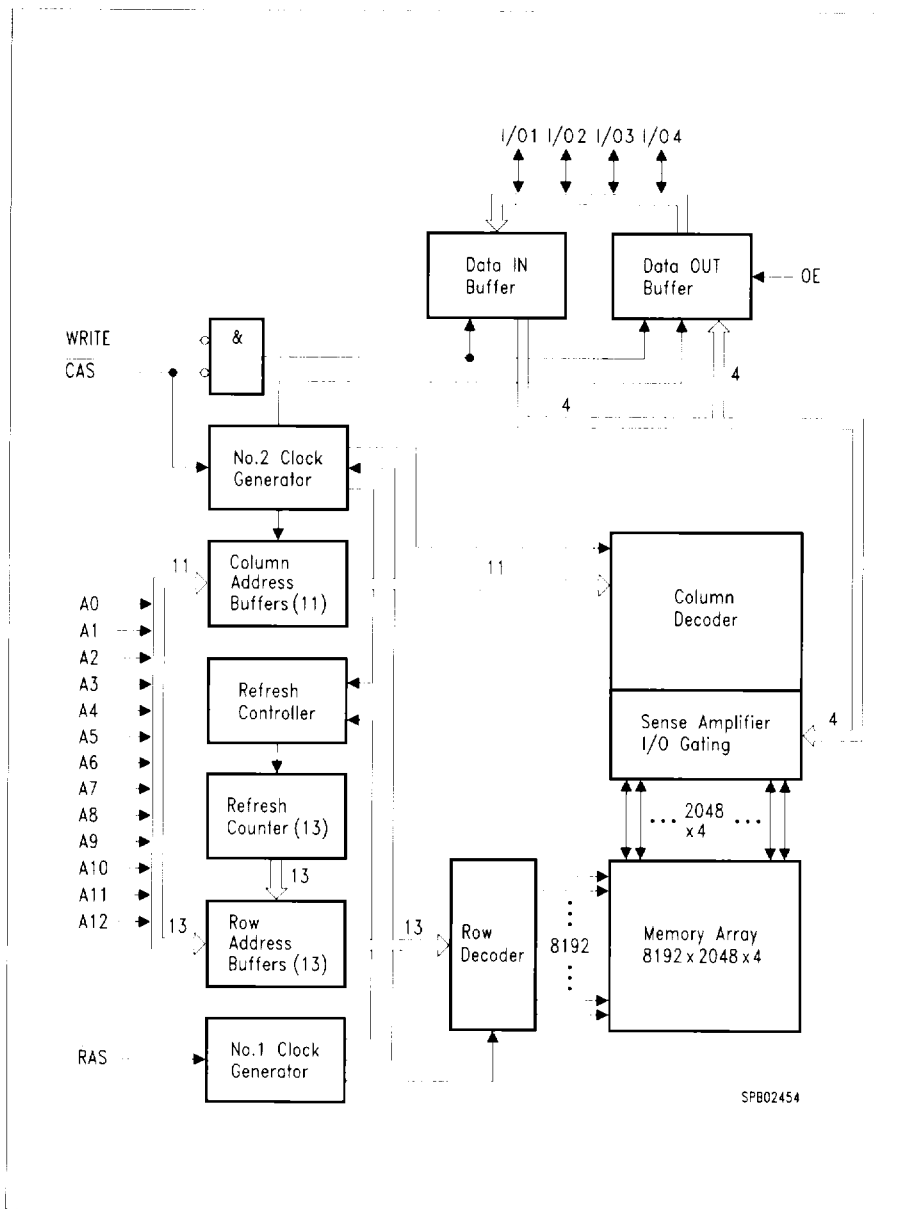
Pin Configuration

TRUTH TABLE

FUNCTION		RAS	CAS	WRITE	OE	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	H - X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H - L	L - H	ROW	COL	Data Out, Data In
Hyper Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
Hyper Page Mode Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
Hyper Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
RAS only refresh		L	H	X	X	ROW	n/a	High Impedance
CAS-before-RAS refresh		H - L	L	H	X	X	n/a	High Impedance
Test Mode Entry		H - L	L	L	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In
Self Refresh (L-version only)		H - L	L	H	X	X	X	High Impedance



Block Diagram for HYB 3164405J/T(L)



Block Diagram for HYB 316405J/T(L)

Absolute Maximum Ratings

Operating temperature range.....	0 to 70 °C
Storage temperature range.....	– 55 to 150 °C
Input/output voltage.....	–0.5 to min (Vcc+0.5,4.6) V
Power supply voltage.....	–0.5V to 4.6 V
Power dissipation.....	1.0 W
Data out current (short circuit).....	50 mA

Note

Stresses above those listed under „Absolute Maximum Ratings“ may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $V_{CC} = 3.3$ V $\pm$ 0.3 V, (values in brackets for HYB 3165405J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL)	V_{OH}	2.4	–	V	
Output „H“ level voltage (Iout = –2mA)					
Output low voltage (LVTTL)	V_{OL}	–	0.4	V	
Output „L“ level voltage (Iout = +2mA)					
Output high voltage (LVCMOS)	V_{OH}	Vcc-0.2	–	V	
Output „H“ level voltage (Iout = –100uA)					
Output low voltage (LVCMOS)	V_{OL}	–	0.2	V	
Output „L“ level voltage (Iout = +100uA)					
Input leakage current, any input (0 V < Vin < Vcc, all other pins = 0 V)	$I_{IL(L)}$	– 2	2	µA	
Output leakage current (DO is disabled, 0 V < Vout < Vcc)	$I_{OL(L)}$	– 2	2	µA	
Average Vcc supply current:	I_{CC1}				
–50 ns version		–	110 (140)	mA	2) 3) 4)
–60 ns version		–	100 (120)	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)					
Standby Vcc supply current ($\overline{RAS}=\overline{CAS}=V_{ih}$)	I_{CC2}	–	2	mA	–

DC Characteristics (cont'd)

$T_A = 0$ to 70°C , $V_{SS} = 0\text{ V}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, (values in brackets for HYB 3165405J/T)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average V_{CC} supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: $\overline{\text{CAS}} = V_{IH}$; $t_{RC} = t_{RC\text{ min.}}$)	I_{CC3}	—	110 (140)	mA	2) 4)
		—	100 (120)	mA	
Average V_{CC} supply current, during hyperpage mode (EDO): -50 ns version -60 ns version ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, address cycling: $t_{HPC} = t_{HPC\text{ min.}}$)	I_{CC4}	—	115 (150)	mA	2) 3) 4)
		—	100 (120)	mA	
Standby V_{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{ V}$)	I_{CC5}	—	200	A	—
Average V_{CC} supply current, during $\overline{\text{CAS}}$ -before-RAS refresh mode: -50 ns version -60 ns version ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling: $t_{RC} = t_{RC\text{ min.}}$)	I_{CC6}	—	110 (140)	mA	2) 4)
		—	100 (120)	mA	
Self Refresh Current (L-version only) Average Power Supply Current during Self Refresh. (CBR cycle with $t_{RAS} > t_{RAS\text{ min.}}$, $\overline{\text{CAS}}$ held low, $\overline{\text{WE}} = V_{CC} - 0.2\text{ V}$, Address and $\overline{\text{Din}} = V_{CC} - 0.2\text{ V}$ or 0.2 V)	I_{CC7}	—	400	A	

Capacitance

$T_A = 0$ to 70°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $f = 1\text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11, A12)	C_{I1}	—	5	pF
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$, $\overline{\text{OE}}$)	C_{I2}	—	7	pF
I/O capacitance (I/O1-I/O4)	C_{I0}	—	7	pF

AC Characteristics ⁵⁾⁶⁾

$T_A = 0$ to 70°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 2\text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	84	—	104	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	ns	
RAS pulse width	t_{RAS}	50	100k	60	100k	ns	
CAS pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	ns	
RAS to CAS delay time	t_{RCD}	12	37	14	45	ns	
RAS to column address delay time	t_{RAD}	10	25	12	30	ns	
RAS hold time	t_{RSH}	8	—	10	—	ns	
CAS hold time	t_{CSH}	45	—	50	—	ns	
CAS to RAS precharge time	t_{CRP}	5	—	5	—	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	7
Refresh period for HYB3164405	t_{REF}	—	128	—	128	ms	
Refresh period for HYB3165405	t_{REF}	—	64	—	64	ms	

Read Cycle

Access time from RAS	t_{RAC}	—	50	—	60	ns	8, 9
Access time from CAS	t_{CAC}	—	13	—	15	ns	8, 9
Access time from column address	t_{AA}	—	25	—	30	ns	8,10
OE access time	t_{OEA}	—	13	—	15	ns	
Column address to RAS lead time	t_{RAL}	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	11
Read command hold time referenced to RAS	t_{RRH}	0	—	0	—	ns	11

AC Characteristics (continued)

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12
Output buffer turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	12
Data to $\overline{\text{CAS}}$ low delay	t_{DZC}	0	—	0	—	ns	13
Data to $\overline{\text{OE}}$ low delay	t_{DZO}	0	—	0	—	ns	13
$\overline{\text{CAS}}$ high to data delay	t_{CDD}	13	—	15	—	ns	14
$\overline{\text{OE}}$ high to data delay	t_{ODD}	13	—	15	—	ns	14

Write Cycle

Write command hold time	t_{WCH}	8	—	10	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	ns	
Write command setup time	t_{WCS}	0	—	0	—	ns	15
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	8	—	10	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	8	—	10	—	ns	
Data setup time	t_{DS}	0	—	0	—	ns	16
Data hold time	t_{DH}	7	—	10	—	ns	16

Read-modify-Write Cycle

Read-write cycle time	t_{RWC}	111	—	135	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	67	—	79	—	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	30	—	34	—	ns	15
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	42	—	49	—	ns	15
$\overline{\text{OE}}$ command hold time	t_{OEH}	7	—	10	—	ns	

Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	t_{HPC}	20	—	25	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	8	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	—	27	—	35	ns	7
Output data hold time	t_{COH}	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width in hyper page mode	t_{RAS}	50	200k	60	200k	ns	

AC Characteristics (cont'd) 5)6)

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Notes
		-50		-60			
		min.	max.	min.	max.		
CAS precharge to $\overline{\text{RAS}}$ Delay	t_{RHCP}	27	—	35	—	ns	
OE pulse width	t_{OEP}	7	—	10	—	ns	
OE hold time from CAS high	t_{OEHC}	7	—	10	—	ns	
WE pulse width to output disable at $\overline{\text{CAS}}$ high	t_{WPZ}	7	—	10	—	ns	
Output buffer turn-off delay from $\overline{\text{WE}}$	t_{WPZ}	0	10	0	10	ns	

Hyper Page Mode (EDO) Read-modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	t_{PRWC}	51	—	66	—	ns	
CAS precharge to WE	t_{CPWD}	41	—	49	—	ns	

CAS before RAS refresh cycle

CAS setup time	t_{CSR}	5	—	5	—	ns	
CAS hold time	t_{CHR}	8	—	10	—	ns	
RAS to CAS precharge time	t_{RPC}	5	—	5	—	ns	
Write to RAS precharge time	t_{WRP}	8	—	10	—	ns	
Write hold time referenced to RAS	t_{WRH}	8	—	10	—	ns	

CAS-before-RAS counter test cycle

CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	35	—	40	—	ns	
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Self Refresh Cycle

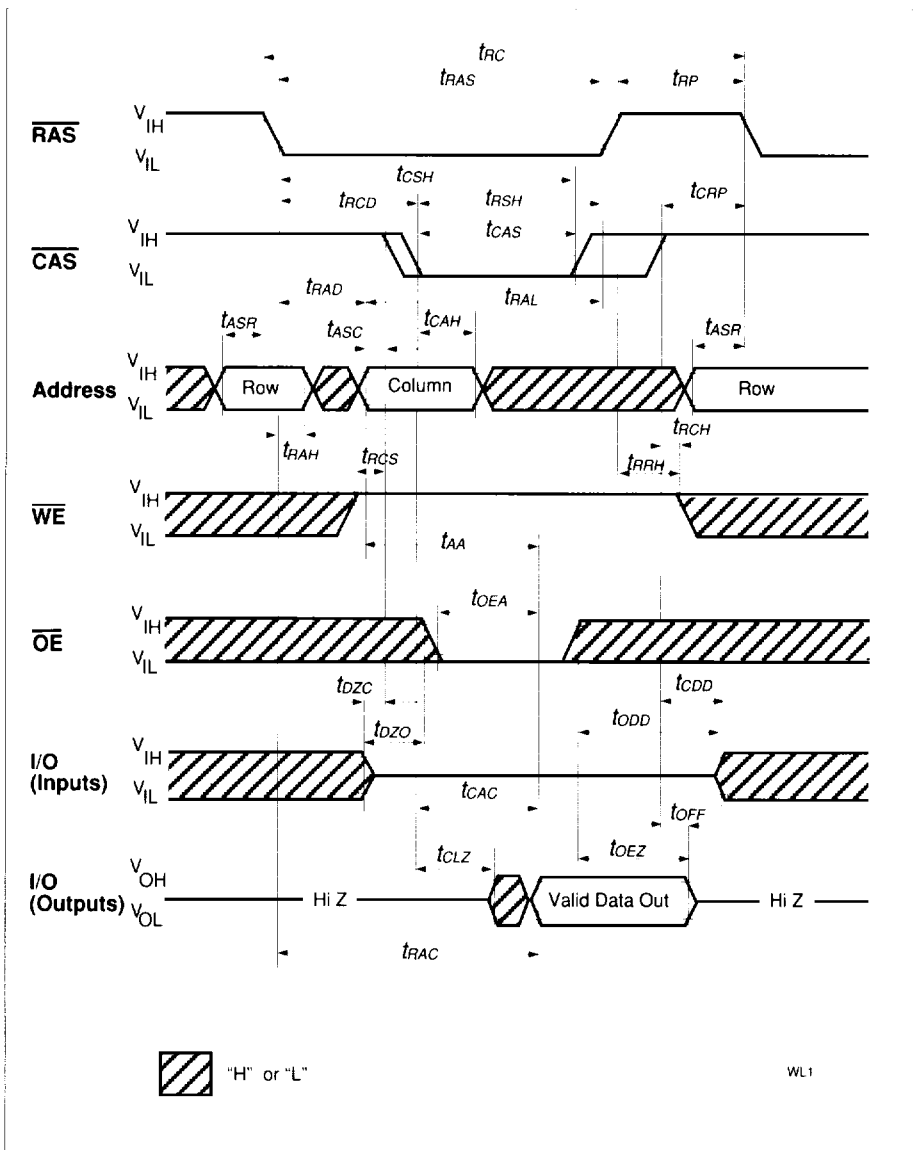
RAS pulse width during self refresh	t_{RASS}	100k	—	100k	—	ns	17
RAS precharge time during self refresh	t_{RPS}	84	—	104	—	ns	17
CAS hold time during self refresh	t_{CHS}	-50	—	-50	—	ns	17

AC Characteristics (cont'd) 5)6)
 $T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$, $t_T = 2 \text{ ns}$

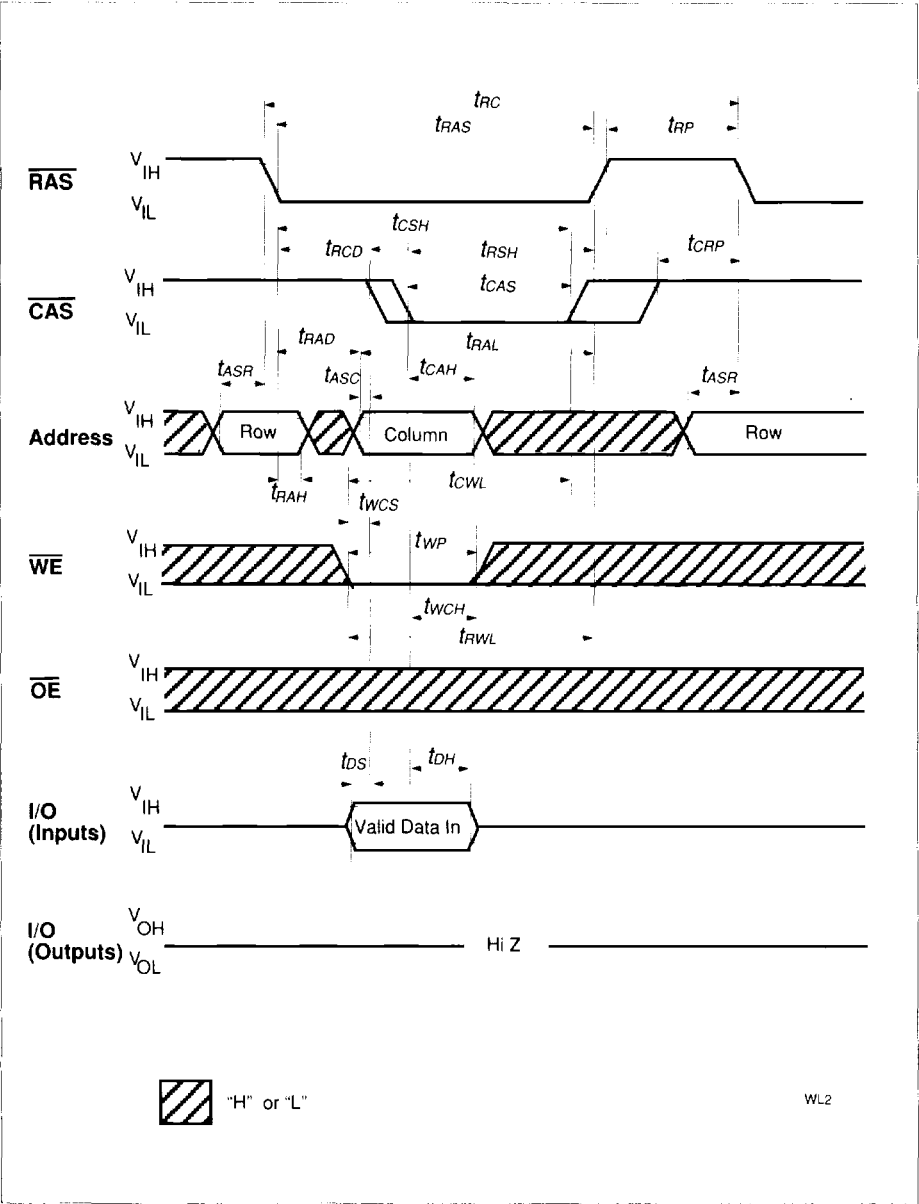
Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Test Mode							
Write command setup time	t_{WTS}	10	—	10	—	ns	18)
Write command hold time	t_{WTH}	10	—	10	—	ns	18)

Notes:

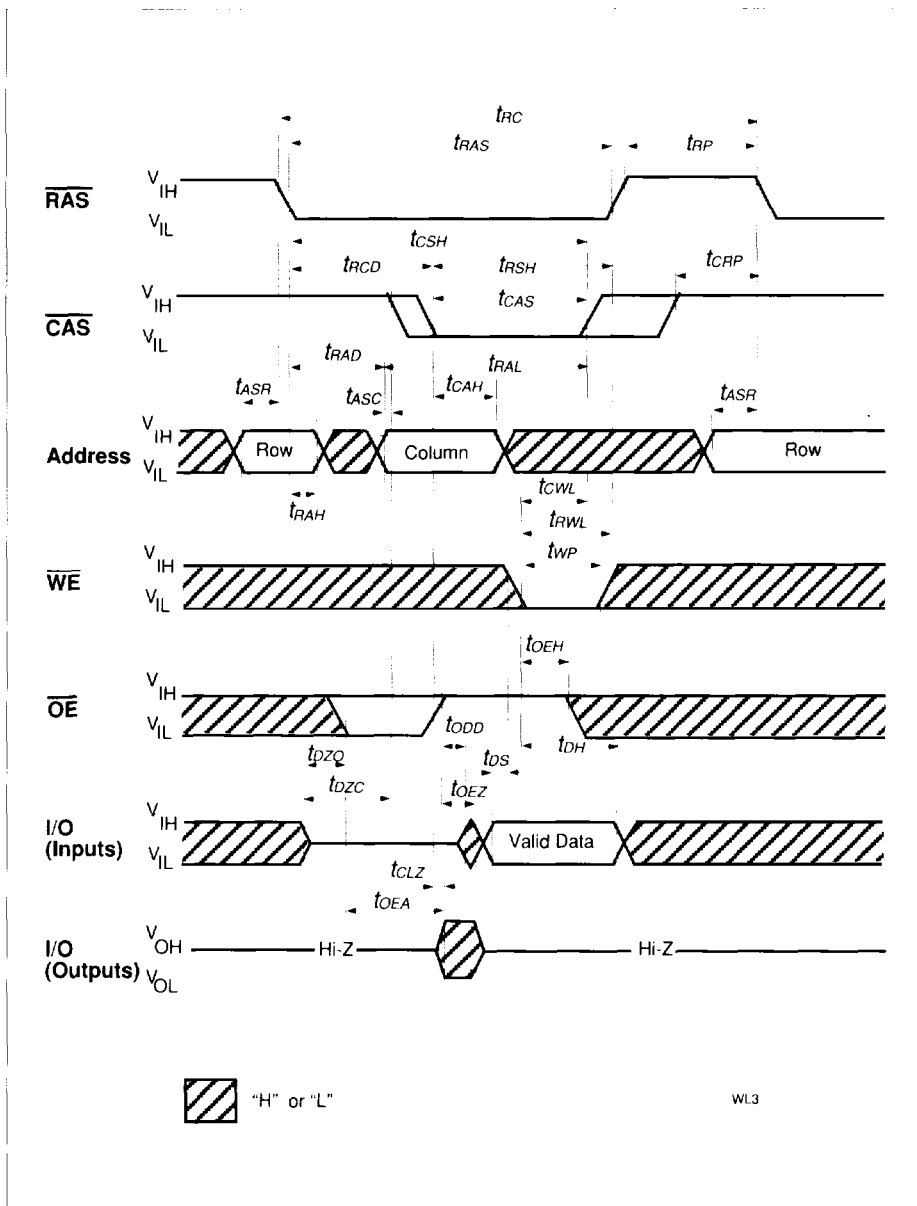
- 1) All voltages are referenced to VSS.
V_{IH} may overshoot to V_V + 0.2V for pulse widths of < 4ns with 3.3V. V_{IL} may undershoot to -2.0V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
- 2) ICC1, ICC3, ICC4 and ICC6 and ICC7 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}. In the case of ICC4 it can be changed once or less during a hyper page mode cycle (thpc).
- 5) An initial pause of 100 s is required after power-up followed by 8 $\overline{\text{RAS}}$ -only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 6) AC measurements assume t_I = 2 ns.
- 7) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- 8) Measured with the specified current load and 100 pF at V_{oh} = 2.0 V and V_{ol} = 0.8 V.
- 9) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
- 10) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} > t_{WCS} (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if t_{RWD} > t_{RWD} (min.), t_{CWD} > t_{CWD} (min.), t_{AWD} > t_{AWD} (min.) and t_{CPWD} > t_{CPWD} (min.), the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in Read-Modify-Write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediately after exit from Self Refresh
- 18) In a Test Mode Read Cycle, the value of t_{rac}, t_{aa}, t_{ac} and t_{cpa} are delayed by 5 ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must be adjusted by 5 ns.



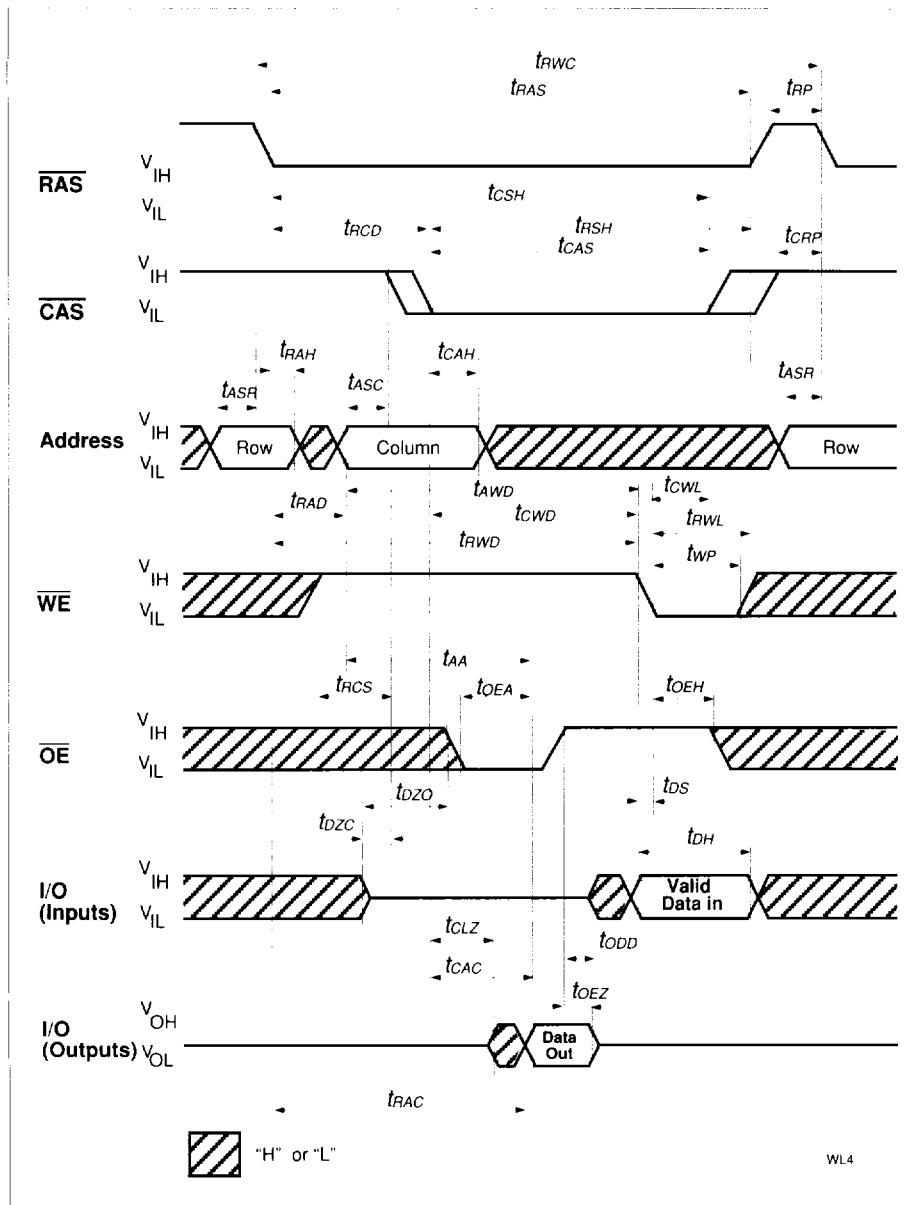
Read Cycle



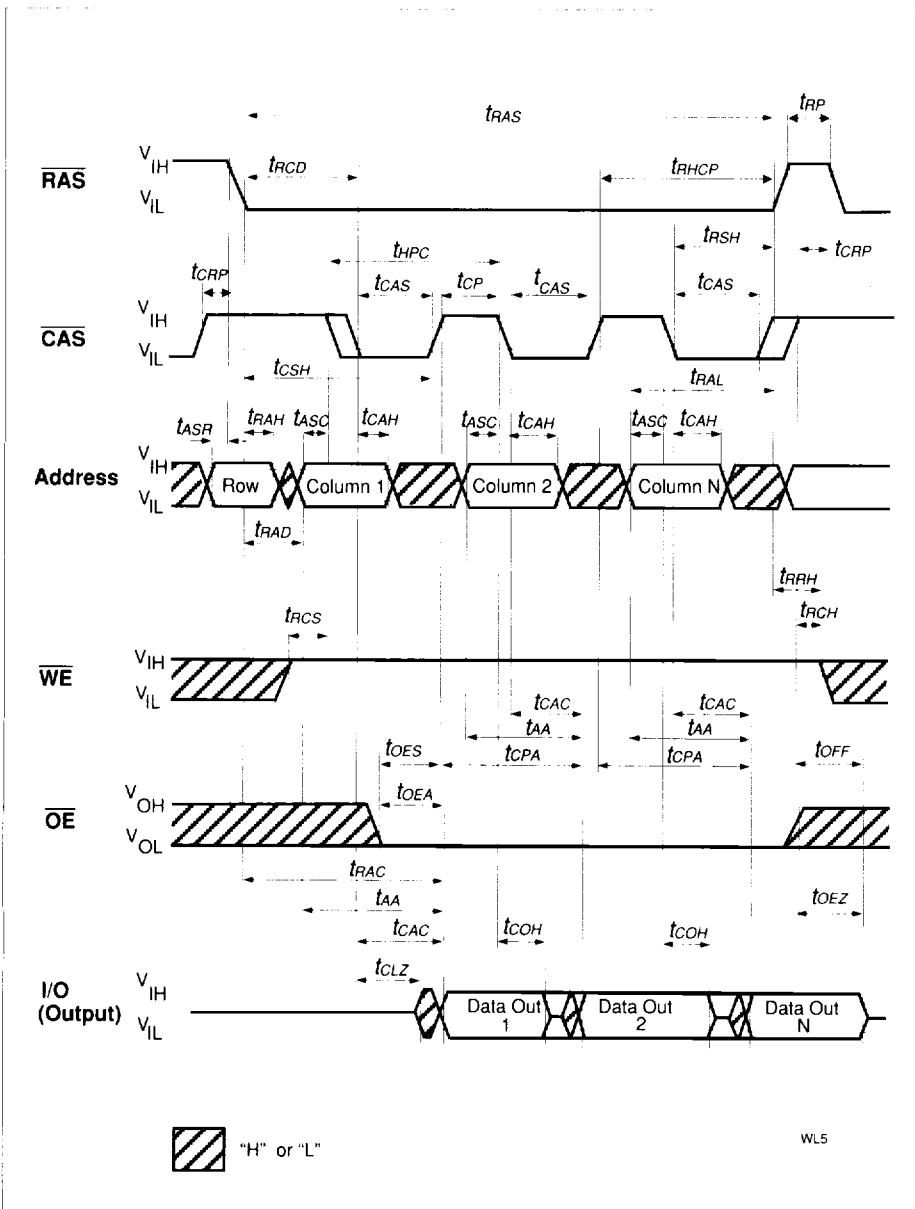
Write Cycle (Early Write)



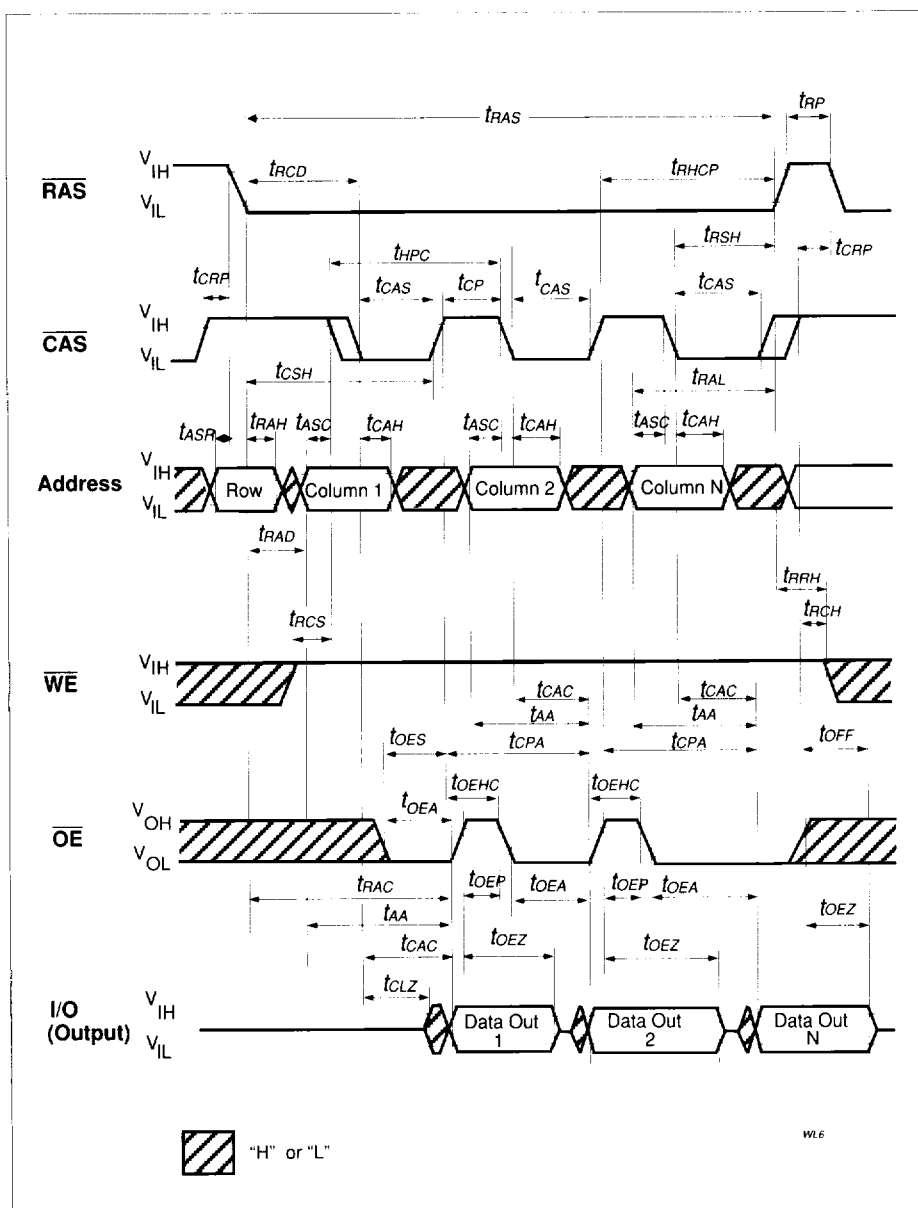
Write Cycle ($\overline{OE}$ Controlled Write)



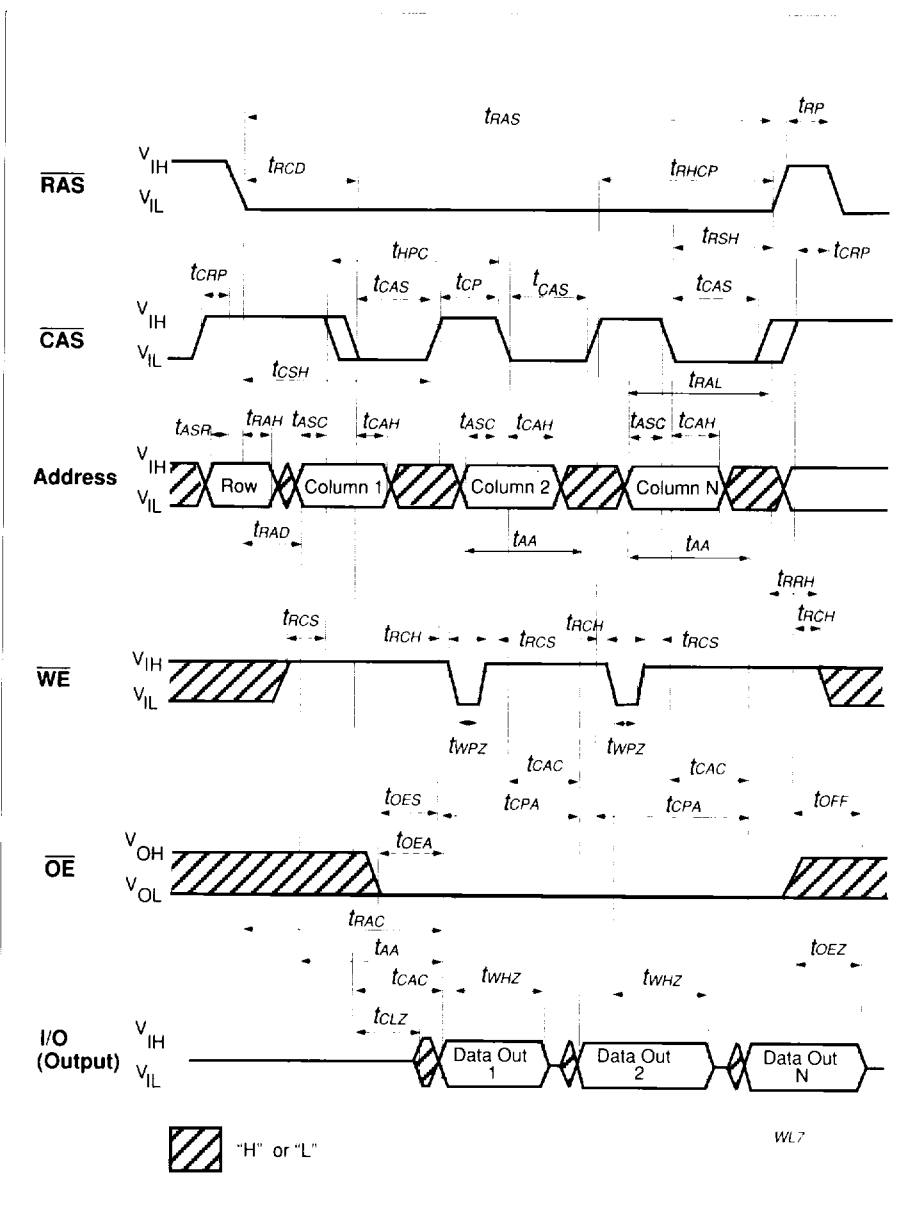
Read-Write (Read-Modify-Write) Cycle



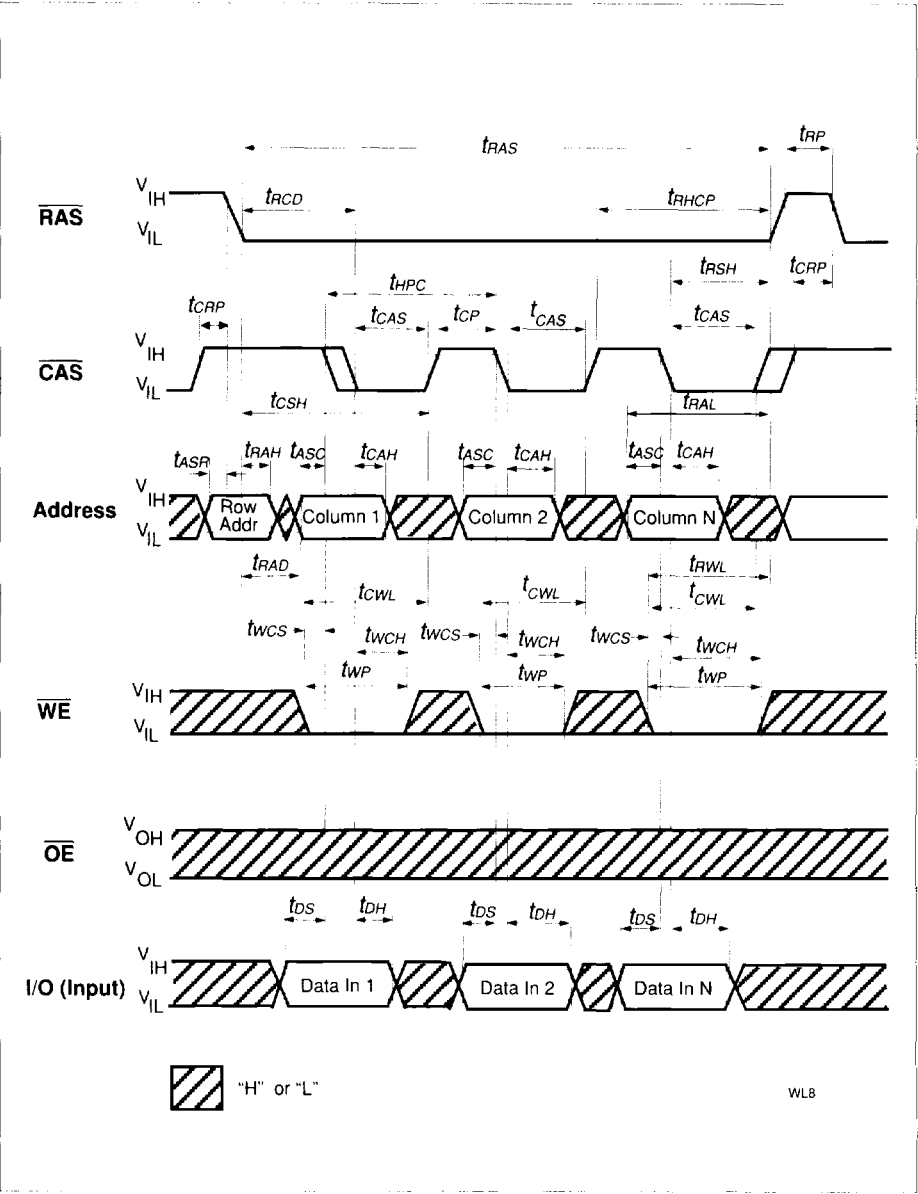
Hyper Page Mode (EDO) Read Cycle



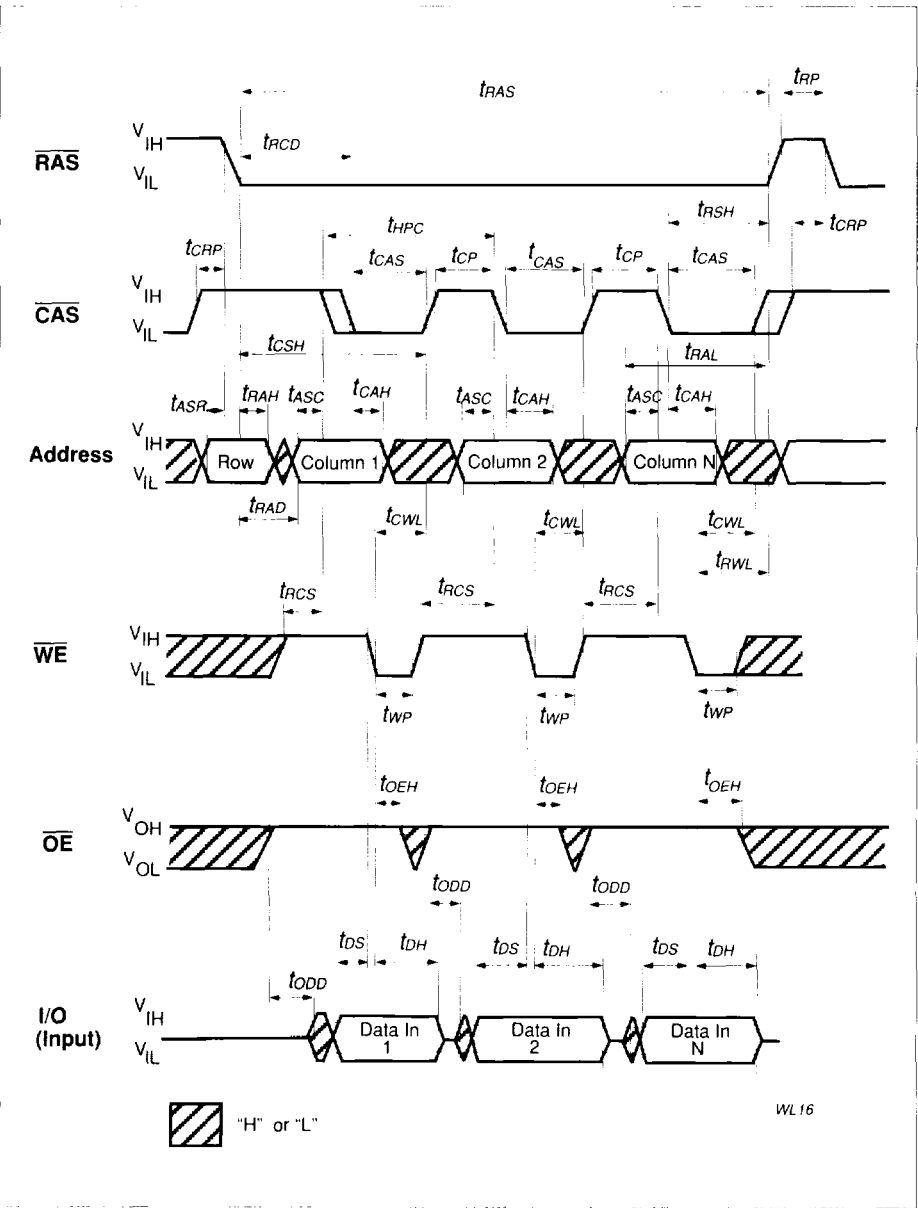
Hyper Page Mode (EDO) Read Cycle ($\overline{\text{OE}}$ Control)



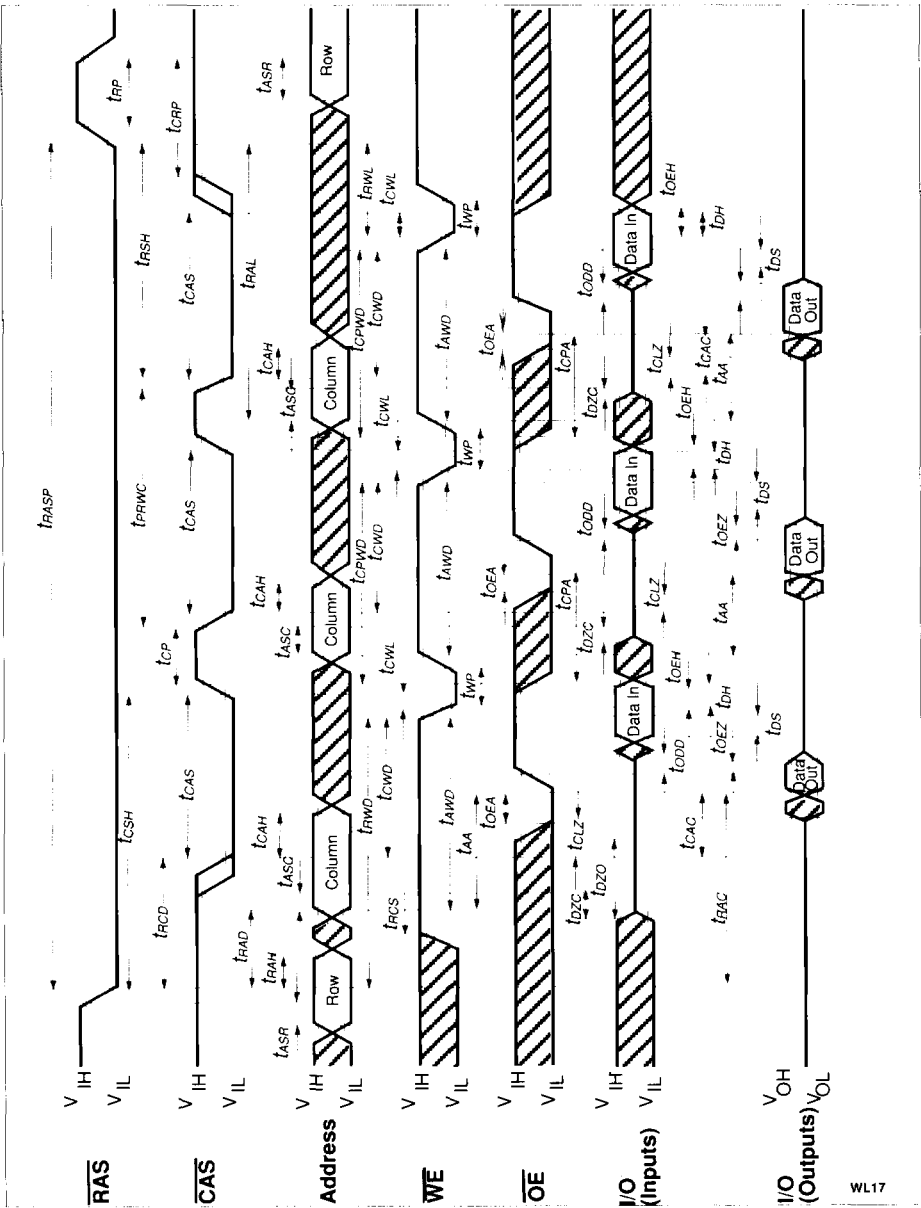
Hyper Page Mode (EDO) Read Cycle ($\overline{\text{WE}}$ Control)



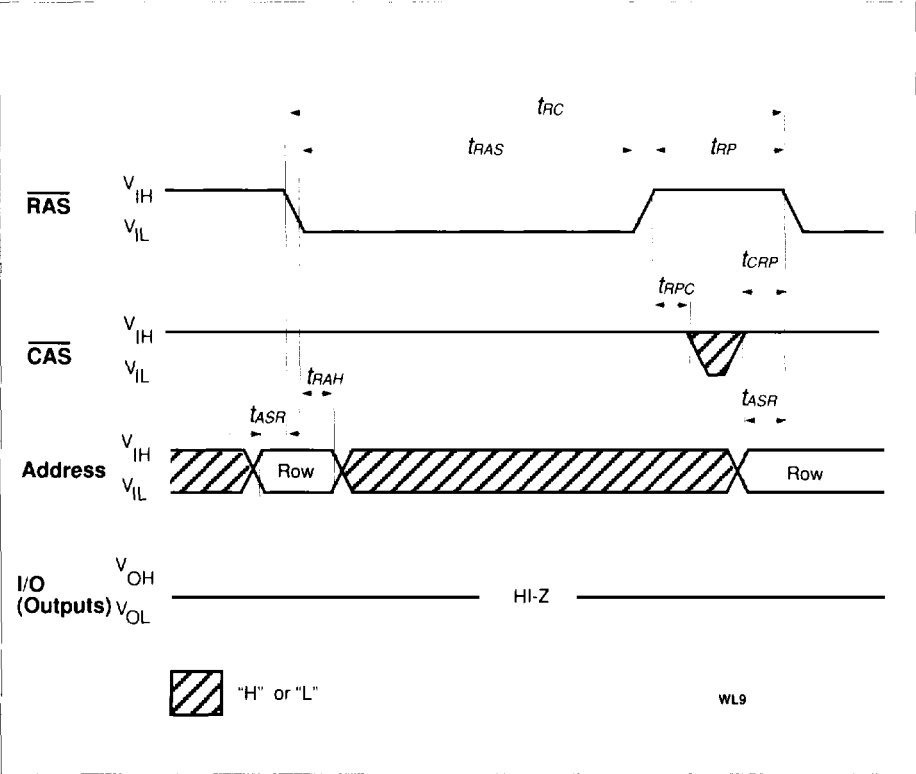
Hyper Page Mode (EDO) Early Write Cycle



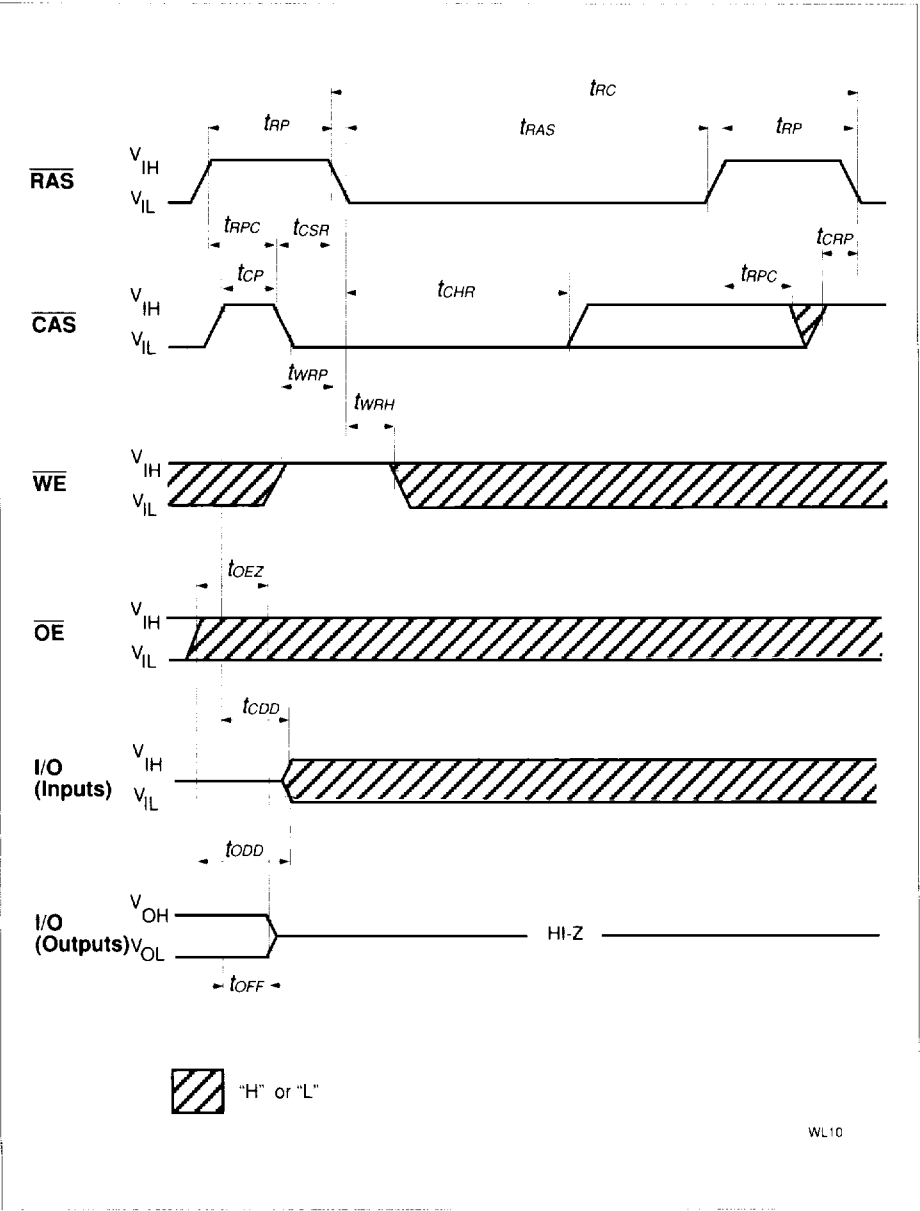
Hyper Page Mode (EDO) Late Write Cycle



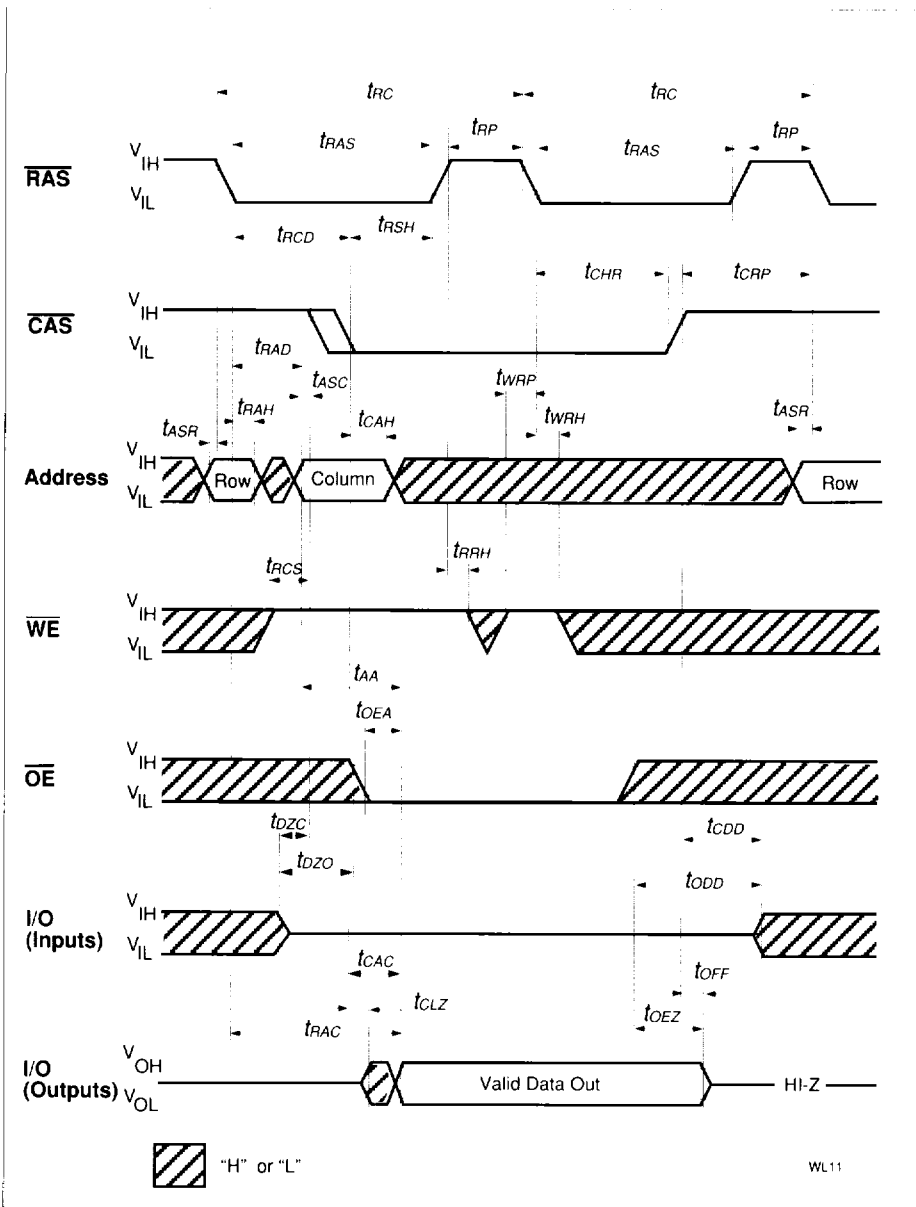
Hyper Page Mode (EDO) Read-Modify-Write Cycle



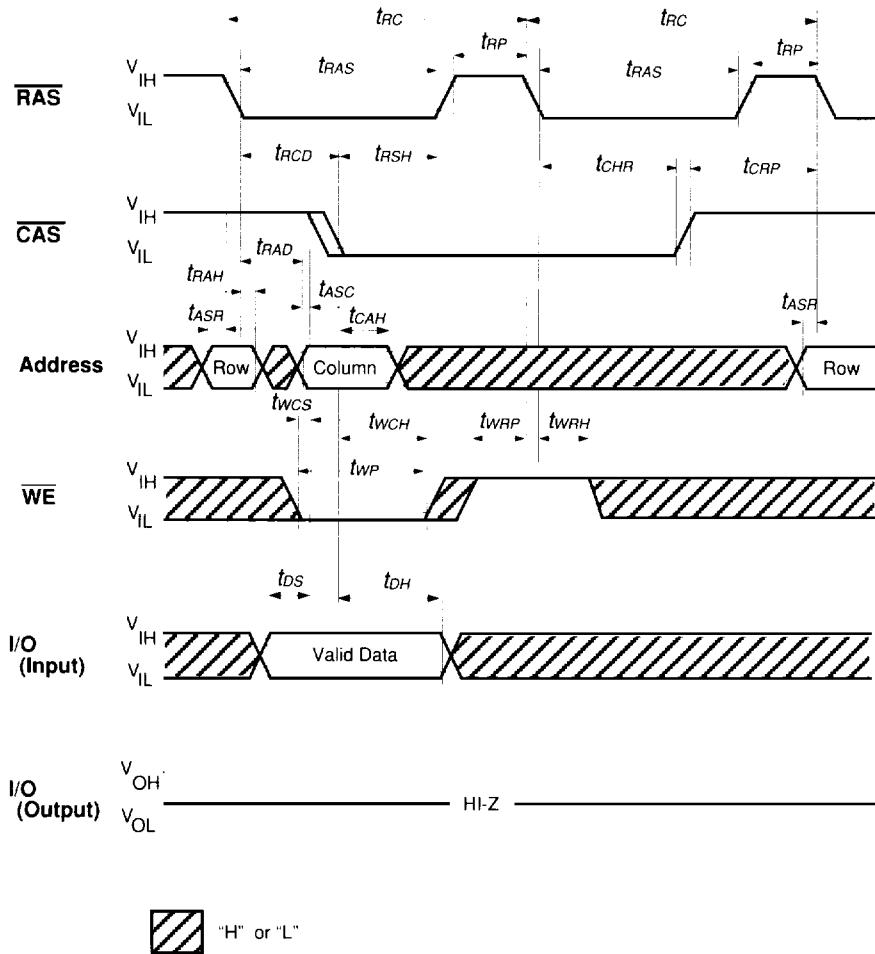
$\overline{\text{RAS}}$ Only Refresh Cycle



CAS-before-RAS Refresh Cycle

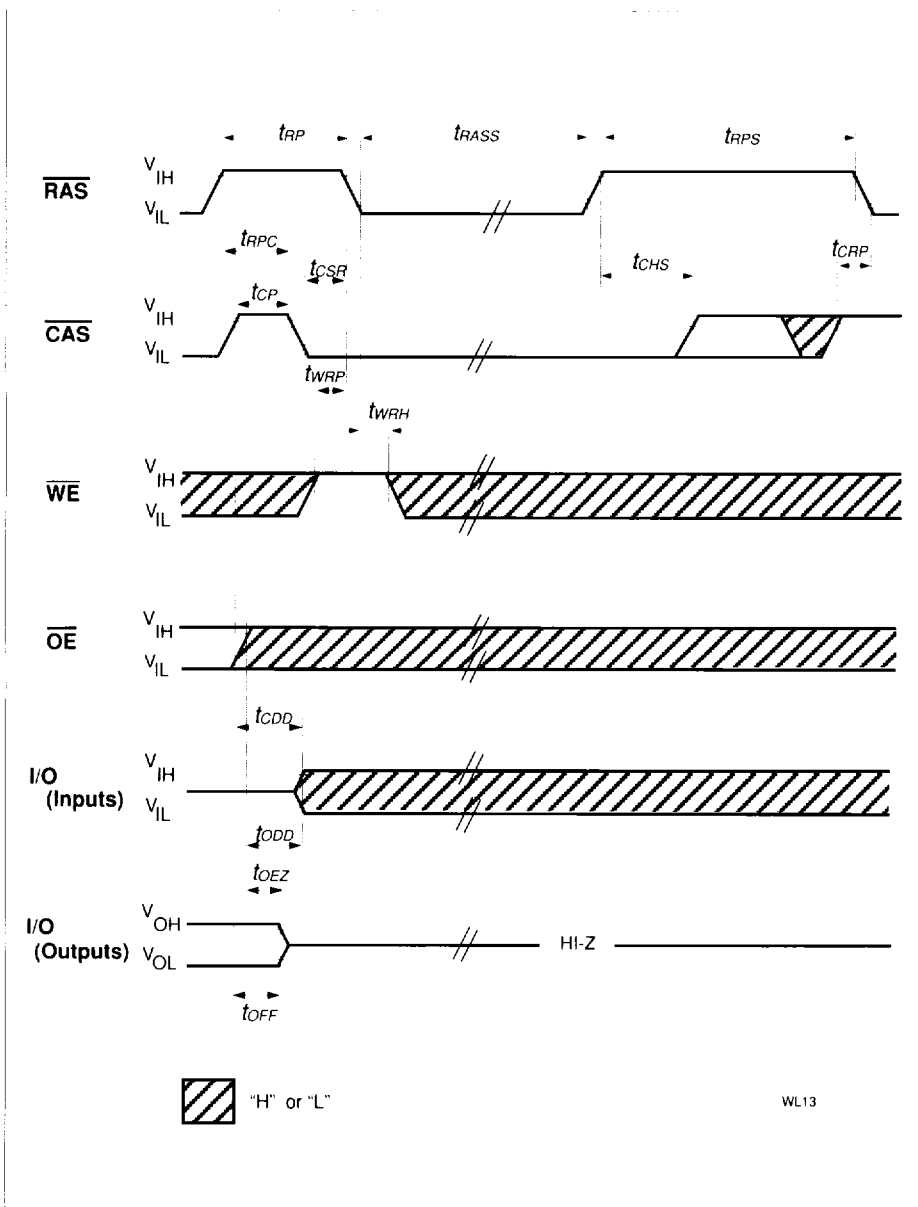


Hidden Refresh Read Cycle

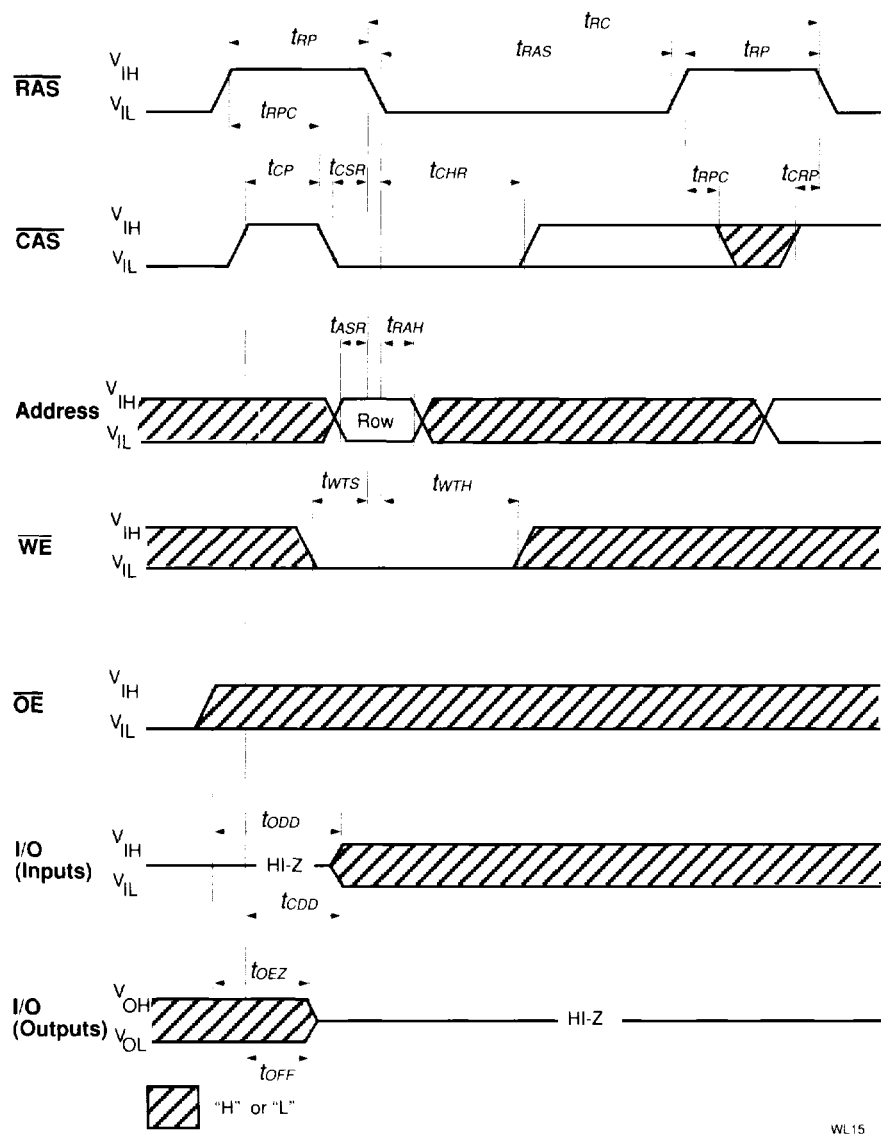


WL12

Hidden Refresh Early Write Cycle

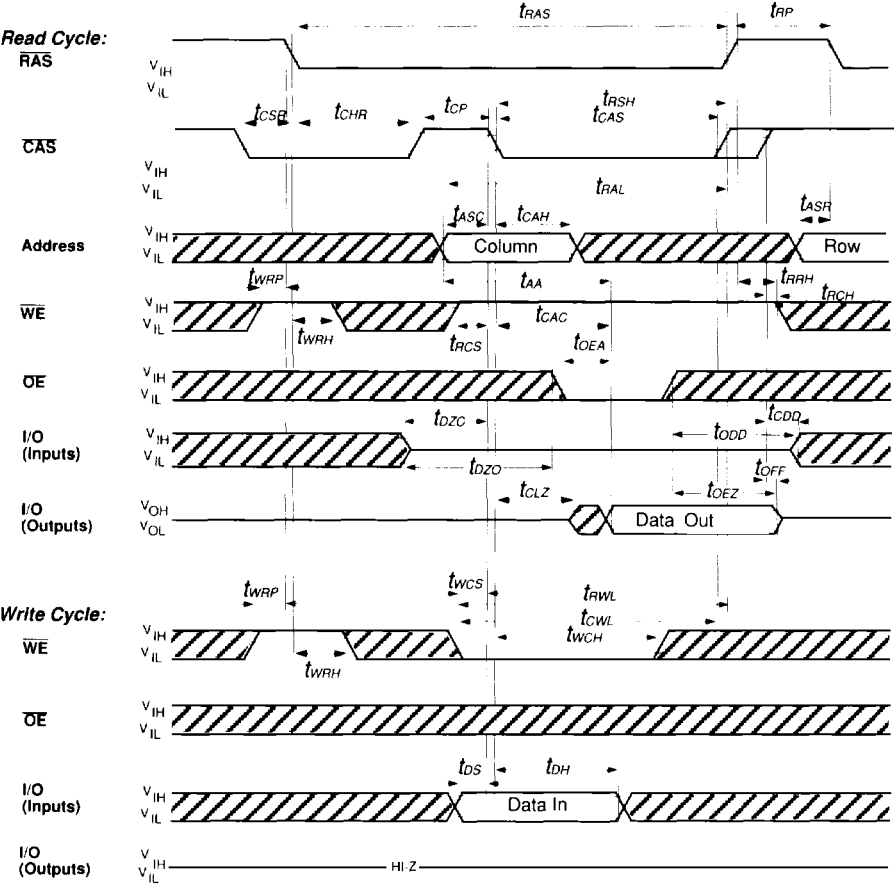


Self Refresh (Sleep Mode)



WL15

Test Mode Entry Cycle

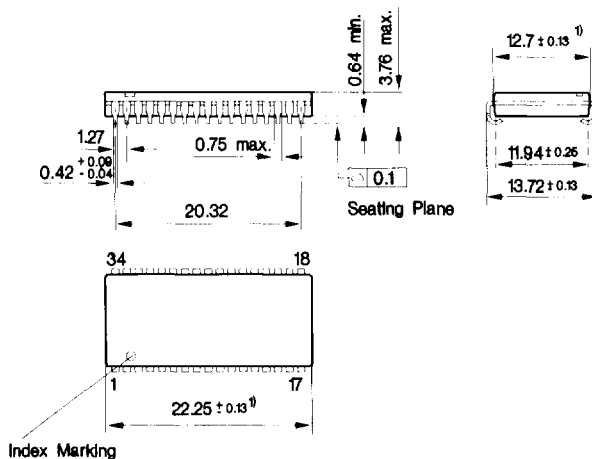


CAS-before-RAS Refresh Counter Test Cycle

Package Outlines

P-SOJ-34-1 (500 mil)

(Plastic Small Outline J-leaded Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing

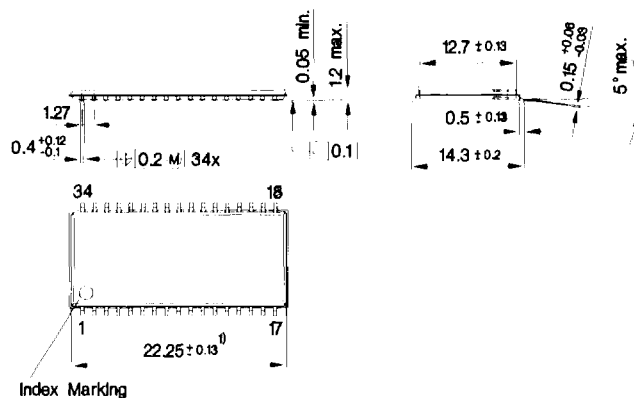
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-TSOPII-34-1 (500 mil)

(Plastic Thin Small Outline Package Type II)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm