MOTOROLA

MC14444

CMOS LSI

(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

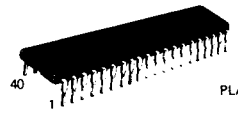
MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER

3

ANALOG-TO-DIGITAL CONVERTER (ADC)

The MC14444 ADC is a 40-pin bus-compatible 8-bit A/D converter with additional digital I/O capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles at 1 MHz and allows for up to 15 analog inputs. In addition, the part has a 3-bit digital I/O port and can accept up to 9 digital inputs. Six of these inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, bus interface and maskable interrupt capability is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Polled or Interrupt Driven Operation
- 3 Dedicated Digital Inputs
- 3-Bit Digital I/O Port
- 9 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%



P SUFFIX
PLASTIC PACKAGE
CASE 711

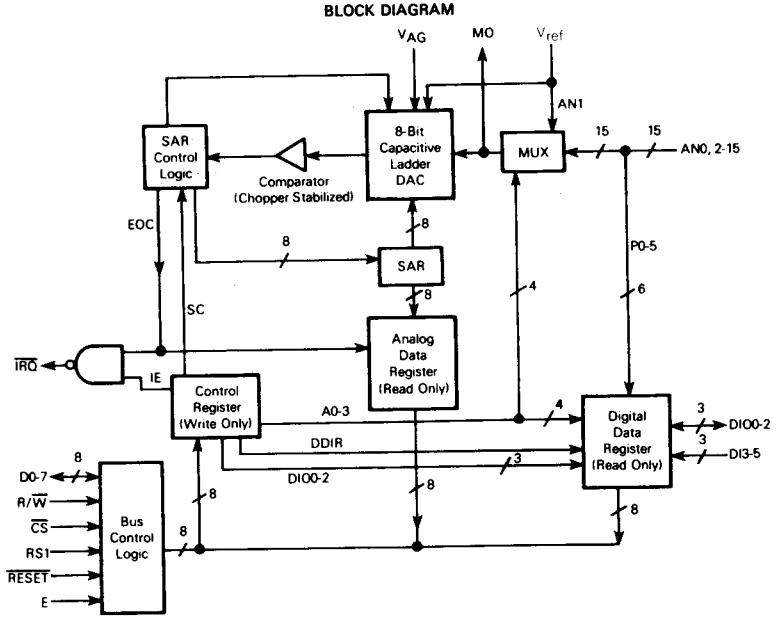
L SUFFIX
CERAMIC PACKAGE
CASE 734

ORDERING INFORMATION

MC14XXX
- L — Ceramic Package
- P — Plastic Package

Suffix Denotes

BLOCK DIAGRAM



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: no derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V ±10%, V_{SS}=0 V, T_A=−40° to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5 V	–	±1	μA
Interrupt Output ($\overline{IRQ}$)					
Output Low Voltage	V_{OL}	I_{Load}=1.6 mA	–	0.4	V
Output Leakage Current (Off State)	I_{LOH}	$V_{OH}=V_{DD}$=5.5 V	–	10	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Peripheral I/O (DIO0-DIO2, DI3-DI5, P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current DI3-DI5, P0-P5	I_{in}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Output High Voltage DIO0-DIO2	V_{OH}	I_{OH}=−0.19 mA	V_{DD}−0.4	–	V
Output Low Voltage DIO0-DIO2	V_{OL}	I_{OL}=0.975 mA	–	0.4	V
Three-State (Off State) Input Leakage Current DIO0-DIO2	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{out} \le V_{DD}$	–	±10	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD}=5.5 V, f_E=1 MHz	–	10	mA
Converter Input Current	I_{ADC}	Analog input current at f_E=1 MHz with multiplexer inputs between V_{SS} and V_{DD}	–	±500	nA
Reference Input Current V_{ref}	I_{ref}	V_{ref}=4.5 to 5.5 V	–	800	μA

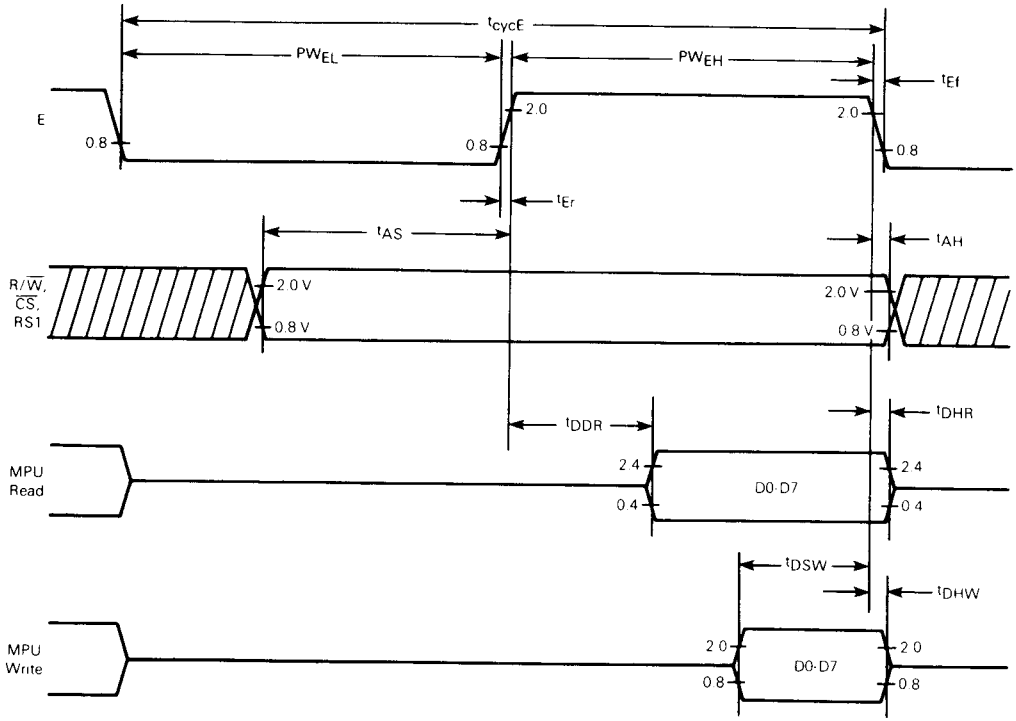
ANALOG CHARACTERISTICS (T_A = −40°C to 85°C)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
On Resistance	Resistance between each analog input and multiplexer output	–	5	kΩ
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±400	nA
A/D Converter (V_{SS} = 0 V, V_{AG} = 0 V, 4.5 V ≤ V_{ref} ≤ V_{DD})				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	–	± ½	LSB
Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	–	± ½	LSB
Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	± 1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

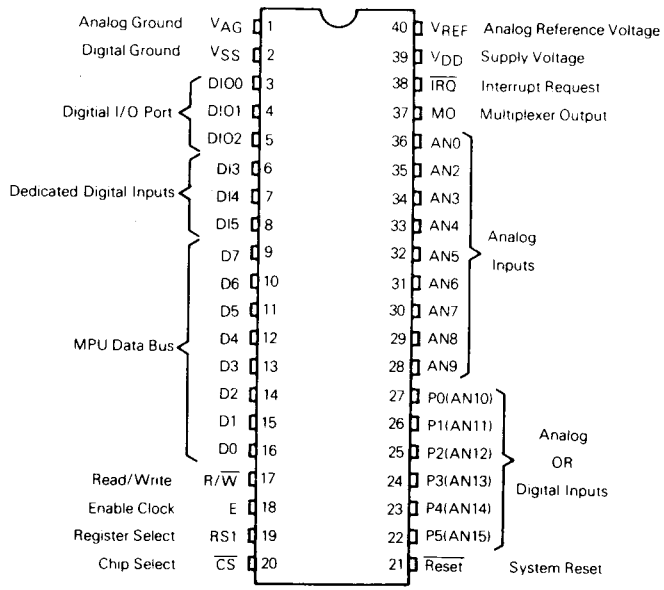
AC CHARACTERISTICS (T_A = −40° to 85°C) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	t_{cycE}	943	–	ns
Enable Clock Pulse Width, High	E	PW_{EH}	440	–	ns
Enable Clock Pulse Width, Low	E	PW_{EL}	410	–	ns
Clock Rise Time	E	t_{Er}	–	25	ns
Clock Fall Time	E	t_{Ef}	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (READ)	D0-D7	t_{DDR}	–	335	ns
Data Setup (WRITE)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	AN0-AN15	C_{in}	–	55	pF
	DI0-DI5, R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	DIO0-DIO2 D0-D7	C_{out}	–	15	pF
High-Impedance Output Capacitance	$\overline{IRQ}$	C_{out}	–	15	pF

FIGURE 1 — BUS TIMING



PIN ASSIGNMENT



PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	DIO0	Digital Port	Input/Output
4	DIO1	Digital Port	Input/Output
5	DIO2	Digital Port	Input/Output
6	DI3	Digital Port	Input
7	DI4	Digital Port	Input
8	DI5	Digital Port	Input
9	D7	Data Bus Bit 7 (MSB)	Input/Output
10	D6	Data Bus Bit 6	Input/Output
11	D5	Data Bus Bit 5	Input/Output
12	D4	Data Bus Bit 4	Input/Output
13	D3	Data Bus Bit 3	Input/Output
14	D2	Data Bus Bit 2	Input/Output
15	D1	Data Bus Bit 1	Input/Output
16	D0	Data Bus Bit 0 (LSB)	Input/Output
17	R/$\overline{W}$	Read/Write	Input
18	E	Enable Clock (ϕ2)	Input
19	RS1	Register Select	Input
20	$\overline{CS}$	Chip Select	Input
21	$\overline{Reset}$	Reset	Input
22	P5(AN15)	Digital Port or Analog Channel 15	Input
23	P4(AN14)	Digital Port or Analog Channel 14	Input
24	P3(AN13)	Digital Port or Analog Channel 13	Input
25	P2(AN12)	Digital Port or Analog Channel 12	Input
26	P1(AN11)	Digital Port or Analog Channel 11	Input
27	P0(AN10)	Digital Port or Analog Channel 10	Input
28	AN9	Analog Channel 9	Input
29	AN8	Analog Channel 8	Input
30	AN7	Analog Channel 7	Input
31	AN6	Analog Channel 6	Input
32	AN5	Analog Channel 5	Input
33	AN4	Analog Channel 4	Input
34	AN3	Analog Channel 3	Input
35	AN2	Analog Channel 2	Input
36	AN0	Analog Channel 0	Input
37	MO	Analog Multiplexer Output	Test Only
38	$\overline{IRQ}$	Interrupt Request	Open-Drain Output
39	V_{DD}	Supply Voltage	Supply
40	V_{ref}	A/D Converter Positive Reference Voltage	Input

MC14444 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) — The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) — The enable clock provides two functions for the MC14444. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ signal is provided to the MC14444 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{RESET}$) — The reset line supplies the means of externally forcing the MC14444 into a known state. When a low is applied to the $\overline{RESET}$ pin, the start conversion, interrupt enable and I/O port data direction bits of the control register are cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus and I/O port output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{RESET}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) — Chip select is an active-low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14444.

MC14444 ANALOG INPUTS AND DIGITAL I/O
(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN9) — These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 16-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN10-AN15) — These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) – P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

Digital I/O Port (DIO0-DIO2) – These pins serve as a 3-bit digital I/O port. At reset the port is configured as an input and may be read from the ADC digital data register. The port may be programmed as an output by setting the DDIR bit in the control register to a logical 1. See the control register discussion for further details. When configured as an output, the DIO port will provide CMOS logic levels for limited dc load currents. (Refer to the Electrical Specifications for the dc drive capability of this port.) New output states are transferred to the external pins on the last falling edge of E during a 16-bit write to the control register. When configured as an input, the port will accept both TTL and CMOS logic levels.

Dedicated Digital Inputs (DI3-DI5) – These three pins are dedicated as digital inputs whose values may be read from the ADC digital data register. They are also TTL and CMOS compatible.

MC14444 SUPPLY VOLTAGE PINS AND TEST PIN

Positive Supply Voltage (V_{DD}) – V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14444 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) – V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) – This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

A/D Ground Reference Voltage (V_{AG}) – This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

Multiplexer Output (MO) – The analog multiplexer selects one of 16 analog input channels and connects it to the input of the A/D converter. The multiplexer output is internally connected to the A/D input and requires no external jumpers. Since loading of the MO pin affects the charging time of the DAC, **it is recommended that no connection be made to the MO pin.**

MC14444 INTERNAL REGISTERS

The MC14444 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

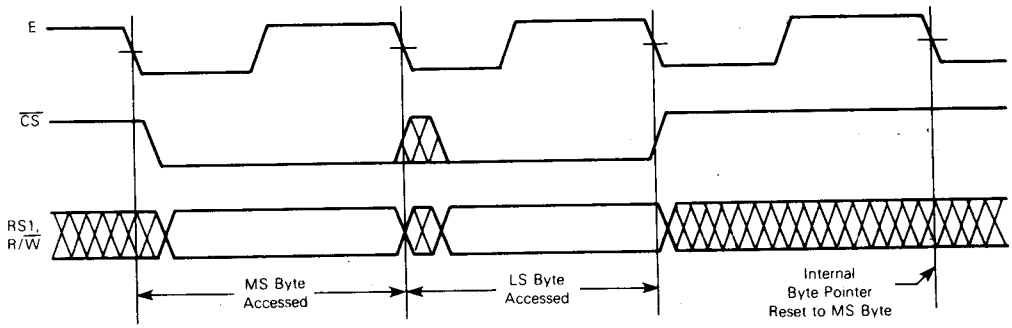
CAUTION: RS1 should not be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

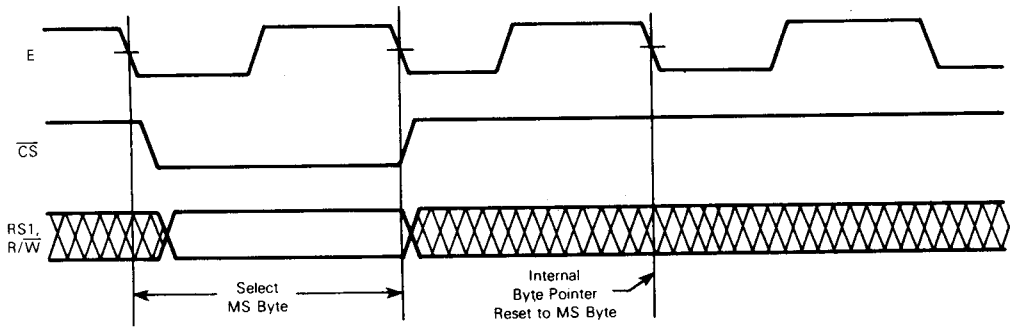
Addressing Signals				
$\overline{RESET}$	$\overline{CS}$	R/$\overline{W}$	RS1	ADC Response
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

FIGURE 2 — ADC ACCESS TIMING

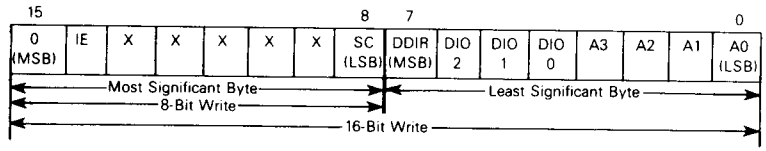
a — Typical 16-Bit ADC Access



b — Typical 8-Bit ADC Access



MC14444 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{REF}
2-9	AN2-AN9
A-F	AN10-AN15(P0-P5)

Digital I/O Output (DIO0-DIO2) – When the MPU configures the 3-bit I/O port as an output, these are the bit locations into which the output states are written.

I/O Port Data Direction (DDIR) – This is the data direction bit for the 3-bit I/O port. A logical 1 configures the port as output while a logical 0 configures the port as input.

Start A/D Conversion (SC) – When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

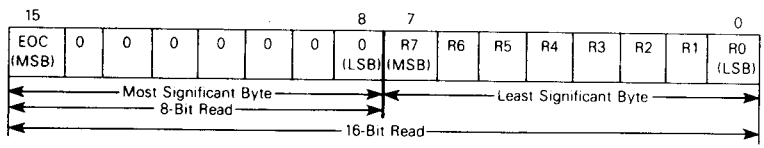
Unused Bits (X) – Bits 9-13 of the ADC Control Register are not used internally.

Interrupt Enable (IE) – The interrupt enable bit, when set to a logical 1, allows the $\overline{IRQ}$ pin to be activated at the completion of the next analog to digital conversion.

Control Register MSB – The MSB of the most significant byte of the ADC control register must be written as a logical 0.

NOTE: A 16-bit control register write is required to change the analog multiplexer address or to update the DIO port. However, 8-bit writes to the MC14444 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

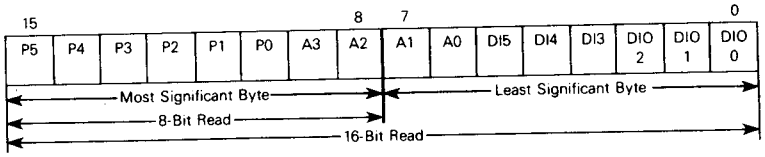
MC14444 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) – The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) – The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single 8-bit M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14444 DIGITAL DATA REGISTER
(Read Only)



Digital I/O Port (DIO0-DIO2) – The states of the three digital I/O pins are read from these bits regardless of whether the port is configured as input or output.

Dedicated Digital Input (DI3-DI5) – The states of the three dedicated digital inputs are read from these bits.

Analog Multiplexer Address (A0-A3) – The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

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ANALOG SUBSYSTEM
(See Block Diagram)

General Description

The analog subsystem of the MC14444 is composed of a 16-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of sixteen channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14444 allows 2 enable clock cycles for the write into the control register even if only 8 bits are written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte, and the interrupt request (IRQ) pin goes low if interrupt has been enabled by the IE bit of the control register. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logical 0) if an A/D conversion is in progress.

FIGURE 3 – TYPICAL A/D TIMING SEQUENCE

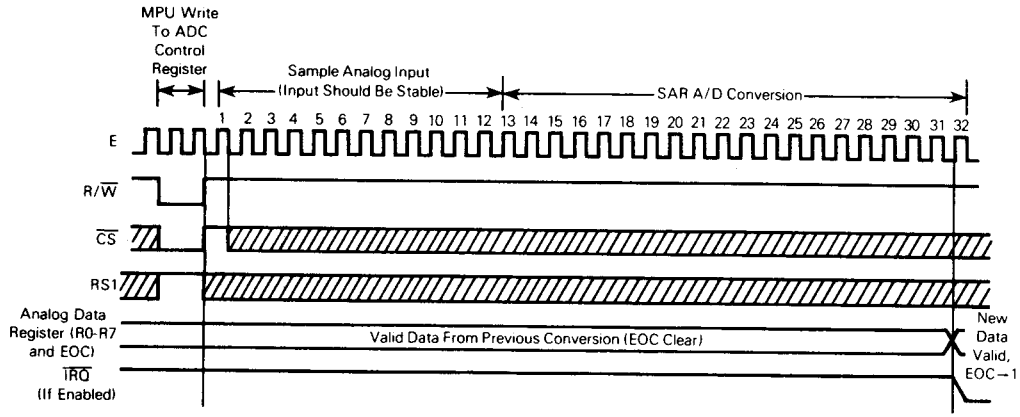

FIGURE 4 – TYPICAL MC14444 APPLICATION IN A CLIMATE CONTROLLER