MONOLITHIC 12-BIT QUAD DAC

Features

- Four 12-bit DAC's on a Single Chip
- Low Power (600mW)
- Double-Buffered Inputs
- Voltage Output

Applications

- Process Control
- Numerical Control
- Instrumentation
- Automatic Test Equipment

Description

The **SP9345** is a QUAD 12-bit digital-to-analog converter with a bipolar voltage output on a single chip. The **SP9345** features a double-buffered input structure for each DAC, allowing easy microprocessor interface. Each DAC is independently addressable allowing a versatile control architecture. All four

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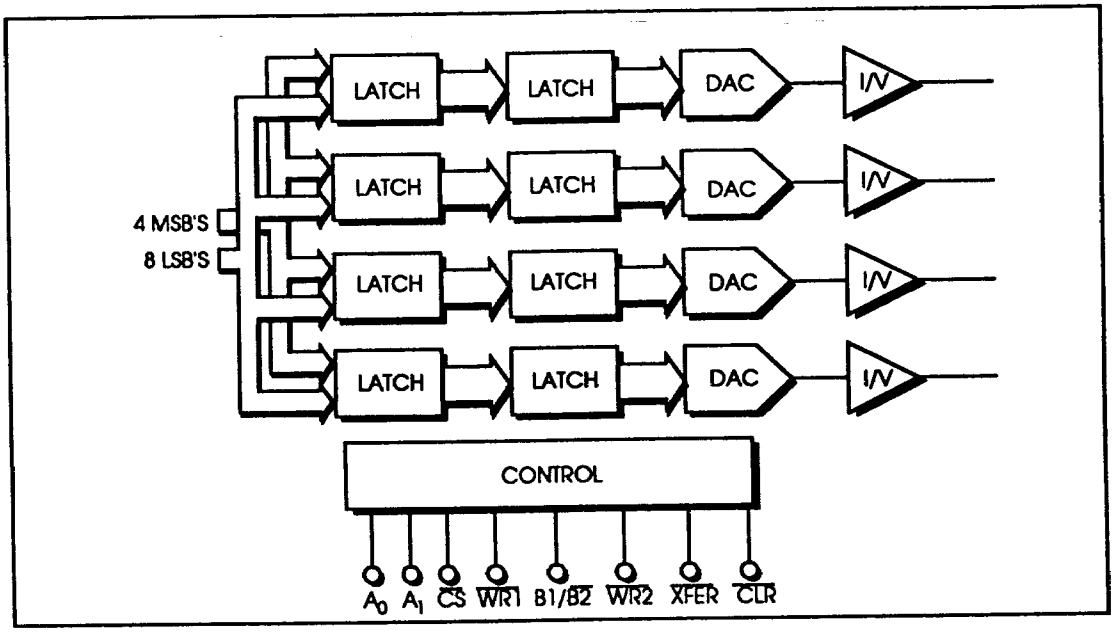

Specifications

(Typical @ 25°C and Nominal Power Supplies)

MODEL	SP9345J/S	SP9345K/T	UNITS	CONDITIONS
DIGITAL INPUTS				
Resolution	12	12	Bits	
V_{IH} Logic	2.4 min.	2.4 min.	V	
V_{IL} Logic	0.8 max.	0.8 max.	V	
4 Quad, Bipolar Coding	Compl. binary	Compl. binary		
REFERENCE INPUT				
Voltage Range	±10	±10	V	
Input Resistance	5 min.,	5 min.,	kΩ	
	10 typ.,	10 typ.,	kΩ	
	15 max.	15 max.	kΩ	
SWITCHING CHARACTERISTICS				
Strobe Width	120 min.	120 min.	ns	
Data Set-up Time	125 min.	125 min.	ns	
Data Hold Time	0 min.	0 min.	ns	
ANALOG INPUT				
Gain	±16 max.	±8 max.	LSB	
Initial Offset Bipolar	±8 max.	±4 max.	LSB	
Voltage Range Bipolar	±10	±10	V	
STATIC PERFORMANCE				
Integral Linearity	±0.5 typ.,	±0.5 typ.,	LSB	
	±1 max	±1 max.	LSB	
Differential Linearity	±0.5 typ.,	±0.5 typ.,	LSB	
	±1 max.	±1 max.	LSB	
Monotonicity (t_{min} to t_{max})	12	12	Bits	
DYNAMIC PERFORMANCE				
Settling Time				
Small Signal to 0.012%	5	5	µsec	
Full Scale to 0.012%	15	15	µsec	
Slew Rate	4 typ.	4 typ.	V/µs	
STABILITY (t_{min} to t_{max})				
Gain	15	15	ppm/°C	
Bipolar Zero	15	15	ppm/°C	
Integral Linearity	±1 max.	±1 max.	ppm/°C	
Differential Linearity	±1 max.	±1 max.	ppm/°C	
POWER REQUIREMENTS				
V_{DD}	+15, ±3%	+15, ±3%	V	
V_{EE}	-15, ±3%	-15, ±3%	V	
I_{DD}	15 typ.,	15 typ.,	mA	
	18 max.	18 max.	mA	
I_{EE}	25 typ.,	25 typ.,	mA	
	28 max.	28 max.	mA	
Power Dissipation	600 typ.,	600 typ.,	mW	
	690 max.	690 max.	mW	
Power Supply Rejection	±0.004 max.	±0.004 max.	%/%	
TEMPERATURE RANGE				
Operating — J,K	0 to +70	0 to +70	°C	
S, T	-55 to +125	-55 to +125	°C	
Storage	-60 to +150	-60 to +150	°C	

Timing Characteristics

PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT -55°C TO +125°C	UNITS	DESCRIPTION
T_{DS}	100 min	125 min	ns	Data Set Up Time (To rising edge of $\overline{WR1}$ command)
T_{DH}	0 min	0 min	ns	Data Hold Time
T_{WR}	100 min	120 min	ns	Write Pulse Width
T_{XFER}	100 min	120 min	ns	Transfer Pulse Width
T_{WC}	200 min	245 min	ns	Total Write Command

Pin Assignments (28-pin Side-brazed or CerDip)

PIN	FUNC.	DESCRIPTION
1	V_{OUT4}	Voltage Output DAC 4
2	V_{EE}	-15V Supply
3	V_{DD}	+15V Supply
4	$\overline{CLR}$	Clear DAC Output to OV
5	REF IN	Reference Input
6	GND	Ground
7	B1/$\overline{B2}$	Byte 1/Byte 2, Selects Data Input Format
8	A_0	Address for DAC Selection
9	A_1	Address for DAC Selection
10	$\overline{XFER}$	Transfer, Updates all DAC's
11	$\overline{WR2}$	Write Input, Gates XFER Function
12	$\overline{WR1}$	Write Input, Gates DAC Selection
13	$\overline{CS}$	Enables DAC Input for Writing
14	V_{OUT1}	Voltage Output DAC 1

PIN	FUNC.	DESCRIPTION
15	V_{OUT2}	Voltage Output DAC 2
16	DB 12	Data Bit 12 (MSB)
17	DB 11	Data Bit 11
18	DB 10	Data Bit 10
19	DB 9	Data Bit 9
20	DB 8	Data Bit 8
21	DB 7	Data Bit 7
22	DB 6	Data Bit 6
23	DB 5	Data Bit 5
24	DB 4	Data Bit 4
25	DB 3	Data Bit 3
26	DB 2	Data Bit 2
27	DB 1	Data Bit 1 (LSB)
28	V_{OUT3}	Voltage Output DAC 3

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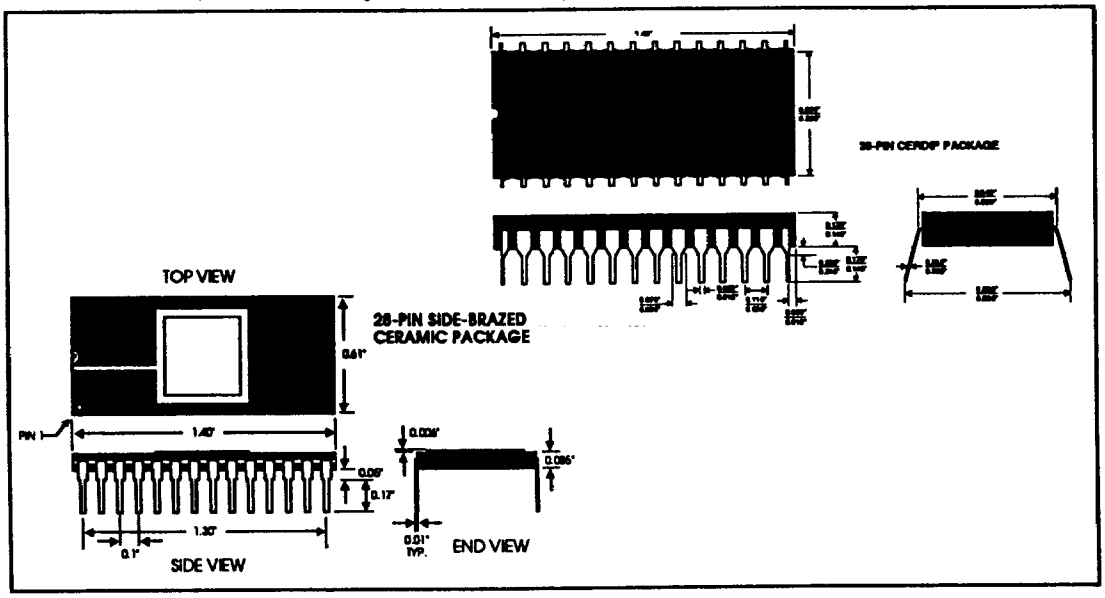
Mechanical Dimensions (28-pin Side-brazed or CerDip)

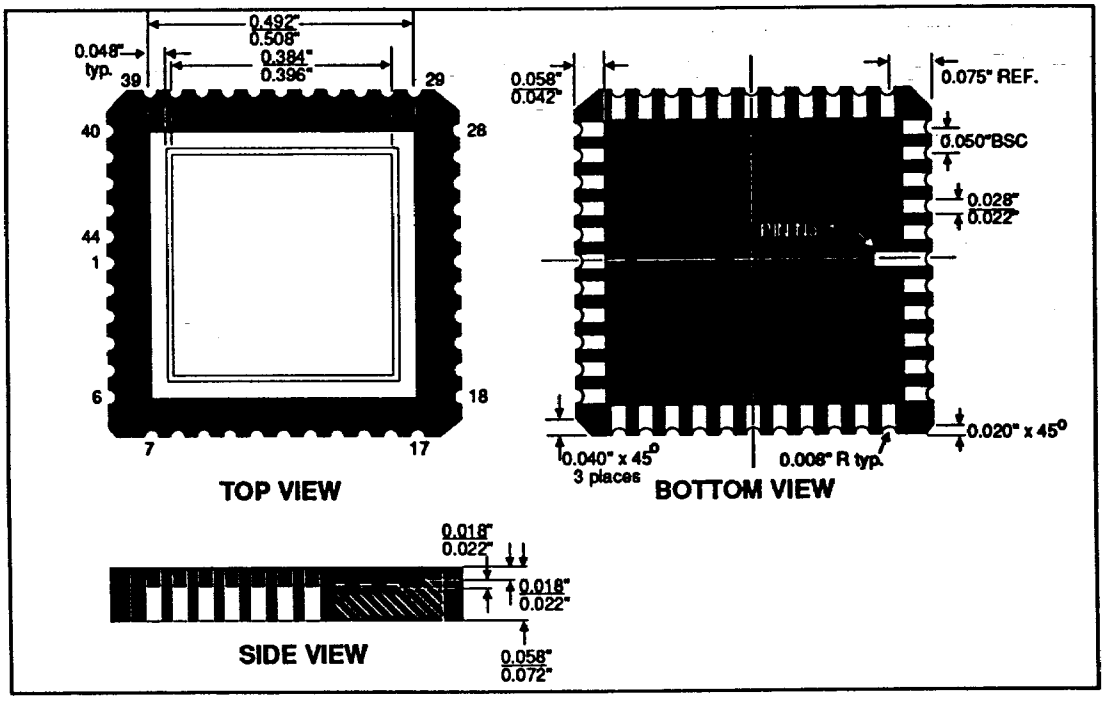


Pin Assignments (44-pin Leadless Chip Carrier)

PIN	FUNC.	DESCRIPTION
1	V_{OUT4}	Voltage Output DAC 4
2	V_{EE}	-15V Supply
3	V_{DD}	+15V Supply
4	N/C	No Connection
5	N/C	No Connection
6	N/C	No Connection
7	N/C	No Connection
8	$\overline{CLR}$	Clear DAC Output to 0V
9	REF IN	Reference Input
10	GND	Ground
11	B1/$\overline{B2}$	Byte 1/Byte 2, Selects Data Input Format
12	A_0	Address for DAC Selection
13	A_1	Address for DAC Selection
14	N/C	No Connection
15	$\overline{XFER}$	Transfer, Updates all DAC's
16	N/C	No Connection
17	N/C	No Connection
8	N/C	No Connection
19	N/C	No Connection
20	$\overline{WR2}$	Write Input, Gates XFER Function
21	$\overline{WRT}$	Write Input, Gates DAC Selection
22	$\overline{CS}$	Enables DAC Input for Writing

PIN	FUNC.	DESCRIPTION
23	V_{OUT1}	Voltage Output DAC 1
24	V_{OUT2}	Voltage Output DAC 2
25	DB 12	Data Bit 12 (MSB)
26	DB 11	Data Bit 11
27	N/C	No Connection
28	N/C	No Connection
29	N/C	No Connection
30	N/C	No Connection
31	DB 10	Data Bit 10
32	DB 9	Data Bit 9
33	DB 8	Data Bit 8
34	DB 7	Data Bit 7
35	DB 6	Data Bit 6
36	DB 5	Data Bit 5
37	DB 4	Data Bit 4
38	N/C	No Connection
39	N/C	No Connection
40	N/C	No Connection
41	DB 3	Data Bit 3
42	DB 2	Data Bit 2
43	DB 1	Data Bit 1 (LSB)
44	V_{OUT3}	Voltage Output DAC 3

Mechanical Dimensions (44-pin Leadless Chip Carrier)



Description *(continued from Page 1)*

DAC's may be simultaneously updated using a single XFER command. Featuring 15 µsec settling time and ±1/2 LSB accuracy, the **SP9345** is ideally suited for applications where multiple DAC's are required and board space is at a premium. Typical applications include ATE, process controllers, robotics, and instrumentation.

Ordering Information

Monolithic 12-Bit QUADDAC, voltage output

Model	Temperature Range	Screening	Package
SP9345JN*	0°C to +70°C	Commercial	28-pin DIP
SP9345KN*	0°C to +70°C	Commercial	28-pin DIP
SP9345JL	0°C to +70°C	Commercial	44-pin LCC
SP9345KL	0°C to +70°C	Commercial	44-pin LCC
SP9345SL/883	-55°C to +125°C	MIL-STD-883	44-pin LCC
SP9345TL/883	-55°C to +125°C	MIL-STD-883	44-pin LCC
SP9345SQ/883*	-55°C to +125°C	MIL-STD-883	28-pin DIP
SP9345TQ/883*	-55°C to +125°C	MIL-STD-883	28-pin DIP

*Sipex reserves the right to ship either Ceramic Side-Brazed or CerDip packaged product.

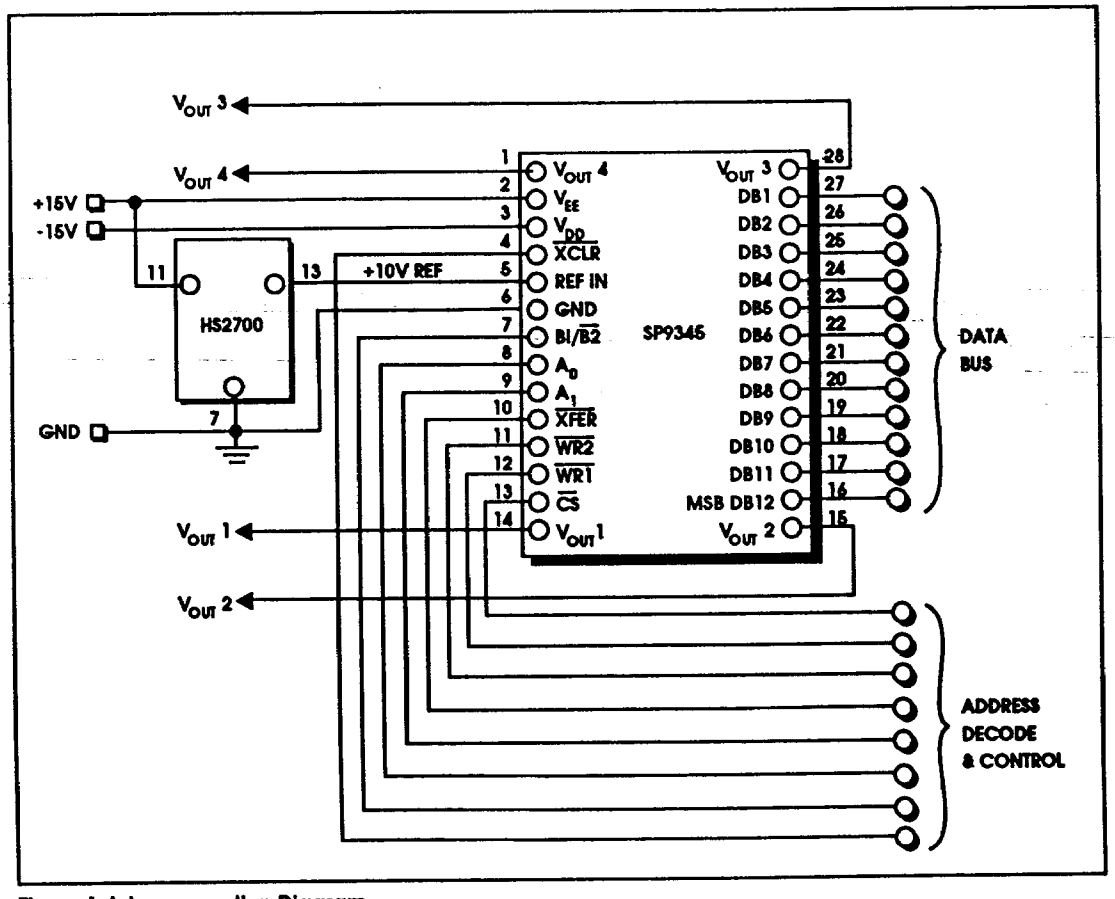


Figure 1. Interconnection Diagram

INPUT			OUTPUT
MSB		LSB	
0000	0000	0000	V_{REF}
0000	0000	0001	V_{REF} - 1 LSB
0111	1111	1111	0 - 1 LSB
1000	0000	0000	0
1000	0000	0001	0 + 1 LSB
1111	1111	1111	$-V_{REF}$ + 1 LSB
$1\ LSB = \frac{V_{REF}}{2^{12}}$			

Table 1. Complementary Binary Coding

Principles of Operation

The **SP9345** is made up of five main functional blocks — the input data multiplexer, the DAC registers, control logic, the four 12-bit D/A converters, and the bipolar output voltage converter circuits. The input data multiplexer is designed to interface to either 12- or 8-bit microprocessor data busses. The data selection (width) accepted by the **SP9345** is controlled by the B1/$\overline{B2}$ signal; a logic high on pin 7 will select the12-bit mode, while a low will select the 8-bit mode. In the 12-bit mode the data is transferred to the DAC registers without changes in its format. In the 8-bit mode the four least significant bits (LSBs) are connected to the four most significant bits (MSBs), allowing an 8-bit MSB-justified interface. All data inputs are enabled using the $\overline{CS}$ signal in both modes.

The digital inputs are designed to be both TTL and 5V CMOS compatible, despite the +15V nominal chip power supply voltage. To achieve the compatability, the digital inputs are converted into 15V logic levels with TTL level shifters using a 6.8V zener reference created on-chip.

In order to reduce the DAC full scale output sensitivity to the large weighting of the MSB's found in conventional R-2R resistor ladders, the 3 MSB's are decoded into 8 equally weighted levels. This reduces the contribution of each bit by a factor of 4, thus reducing the output sensitivity to mismatches in resistors and switches by the same amount. Linearity errors and stability are both improved for the same reasons.

Each D/A converter is separated from the data bus by two sets of registers, each consisting of level-triggered latches. The first set is the input register and is 12-bits wide. This register is selected by the address inputs, A_0 and A_1, and is enabled by the $\overline{CS}$ and $\overline{WR1}$ signals. In the 8-bit mode the enable signal to the 8 MSB's is disabled by a logic low on B1/$\overline{B2}$ to allow the 4 LSB's to be updated. The second register, which accepts the decoded 3 MSB's plus the 9 LSB's, is 16-bits wide. The four

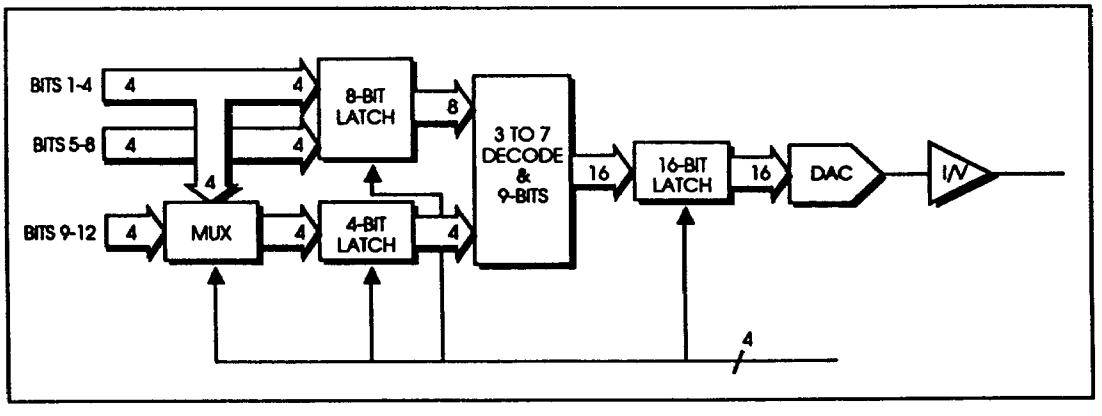


Figure 2. Detailed Block Diagram (only one DAC shown)

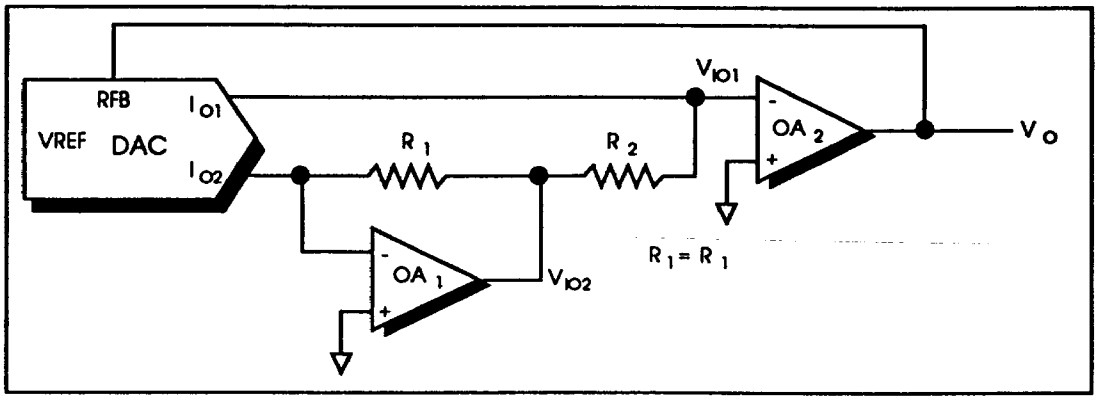


Figure 3. Current-to-Voltage Converter

secondary registers are updated simultaneously for all DAC's using the $\overline{XFER}$ and $\overline{WR2}$ signals. Using the $\overline{CLR}$ and $\overline{WR2}$ signals or the power-on-reset, (enabled when the power is switched on) the second register is set to all 0's and the DAC output will settle to 0V.

Using the control logic block inputs, the user has full control of address decoding, chip enable, data transfer and clearing of the DAC's. The logic inputs are level triggered, and like the digital code inputs, are TTL and CMOS compatable. The truth table (*Table 3*) shows the appropriate functions associated with the states of the inputs.

The DACs themselves are implemented with a precision thin film resistor network and NMOS switches. Each D/A converter is used to convert the 16-bit input from the second storage register to a precision current. The set of resistors and switches for each DAC are divided into two distinct configurations, one for the MSB inputs 1-7 and the second for inputs 8-16. The resistor network for the MSB consists of 7 parallel resistors connected to VREF and driven by switches of equal size controlled by the bit inputs. Depending on the input data, the switches connect the current derived from VREF to the I_{O1} or I_{O2} lines. The total reference input I is divided into 8 equal currents in such a way that 1/8th flows through each of the 7 parallel resistors and 1/8th flows through the rest of the resistor network connected as a conventional R-2R ladder. This again reduces the influence of the heavily weighted MSB's, thus minimizing errors.

The voltage output of the **SP9345** is created on-chip using two operational amplifiers for each DAC, providing a ±10V bipolar output range with offset

PIN	FUNCTION
A_0	Address 0 for DAC Selection
A_1	Address 1 for DAC Selection
$\overline{WR1}$	Enables A_0, A_1 (Along with $\overline{CS}$), Active Low, Gated with $\overline{CS}$
B1/$\overline{B2}$	Selects high and low bytes. In 12-bit mode, B1/$\overline{B2}$ tied high. In 8-bit mode, a 12-bit word is loaded into first register when B1/$\overline{B2}$ is high, and a 4-bit word is updated to the lower bits when B1/$\overline{B2}$ is low.
$\overline{WR2}$	Gated with $\overline{XFER}$, used to load all DAC's simultaneously (Active Low)
$\overline{XFER}$	Gated with $\overline{WR2}$, used to load all DAC's simultaneously (Active Low)
$\overline{CLR}$	Gated with $\overline{XFER}$, used to clear all DAC output voltages to OV (Active Low)

Table 2. Pin Function

A_1	A_0	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	$\overline{CLR}$	FUNCTION
0	0	0	0	1	1	X	X	Address DAC A and load input register
0	0	0	0	0	1	X	X	Address DAC A and load 4 LSBs
0	1	0	0	1	1	X	X	Address DAC B and load input register
0	1	0	0	0	1	X	X	Address DAC B and load 4 LSBs
1	0	0	0	1	1	X	X	Address DAC C and load input register
1	0	0	0	0	1	X	X	Address DAC C and load 4 LSBs
1	1	0	0	1	1	X	X	Address DAC D and load input registers
1	1	0	0	0	1	X	X	Address DAC D and load 4 LSBs
X	X	**	**	X	0	0	1	Transfer data from input register to DACs
X	X	X	X	X	0	X	0	Clears all DAC output voltages to 0V
X	X	1	X	X	X	X	X	Invalid state with any other control line active
X	X	X	1	X	X	X	X	Invalid state with any other control line active

X = Don't care; ** = Don't care, however $\overline{CS}$ and $\overline{WR1}$ =1 will inhibit changes to the input registers.

binary coding. *Figure 3* shows the configuration of the two op-amps and the D/A converter. The current at output terminal I_{O1} is fed to the current-to-voltage converter, which, in the case of a unipolar output range, provides a virtual ground. The current output at terminal I_{O2} is converted into a voltage V_{IO2} using a similar current-to-voltage converter providing a low resistance output. This voltage is summed through resistor R_2 to the summing point of amplifier OA_2 producing a voltage at the output proprtional to $V_{IO1}+V_{IO2}$.

Loading Data

The sequence necessary to load a 12-bit word on a 12-bit wide data bus is as follows:

1) Set $\overline{XFER}$=1, B1/$\overline{B2}$=1, $\overline{CLR}$=1, $\overline{WR1}$=1, $\overline{WR2}$=1, $\overline{CS}$=1.
2) Set A_0 and A_1 (the DAC address) to the desired DAC.
   0 0 = DAC_A 0 1 = DAC_B
   1 0 = DAC_C 1 1 = DAC_D
3) Set D_{11} (MSB) through D_0 (LSB) to the

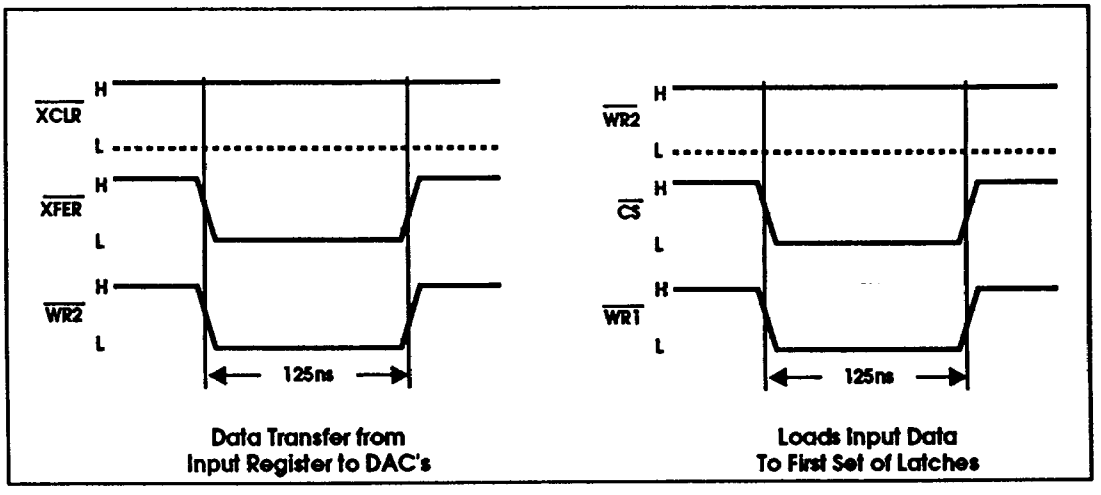


Figure 4. Timing

desired digital input code.
4) Load the word to the selected DAC by cycling $\overline{WR1}$ and $\overline{CS}$ through the following sequence:
"1"——> "0"——> "1"
5) Repeat sequence for each register.

To load a 12-bit word to the input register of each DAC, using an 8 bit data bus, the sequence is as follows:

1) Set $\overline{XFER}$=1, B1/$\overline{B2}$=1, $\overline{CLR}$=1, $\overline{WR1}$=1, $\overline{WR2}$=1, $\overline{CS}$=1.
2) Set D_{11} through D_4 to the 8 MSB's of the desired digital input code.
3) Load the 8 MSB's of the digital word to the selected input register by cycling $\overline{WR1}$ and $\overline{CS}$ through the "1"——> "0"——> "1" sequence.

4) Reset B1/$\overline{B2}$ from "0"——> "1"
5) Set D11 (MSB) through D_8 to the 4 LSB's of the digital input code.
6) Load the 4 LSB's by cycling $\overline{WR1}$ and $\overline{CS}$ through the "1"——> "0"——> "1" sequence.

To transfer the four 12-bit words in the four input registers to the DAC registers:

1) Set $\overline{CLR}$=1, $\overline{CS}$=1, $\overline{WR1}$=1
2) Cycle $\overline{WR2}$ and $\overline{XFER}$ through the "1"——> "0"——> "1" sequence.

To "zero" the outputs of the four DAC's, cycle $\overline{WR2}$ and $\overline{CLR}$ through the "1" —> "0" —> "1" sequence.

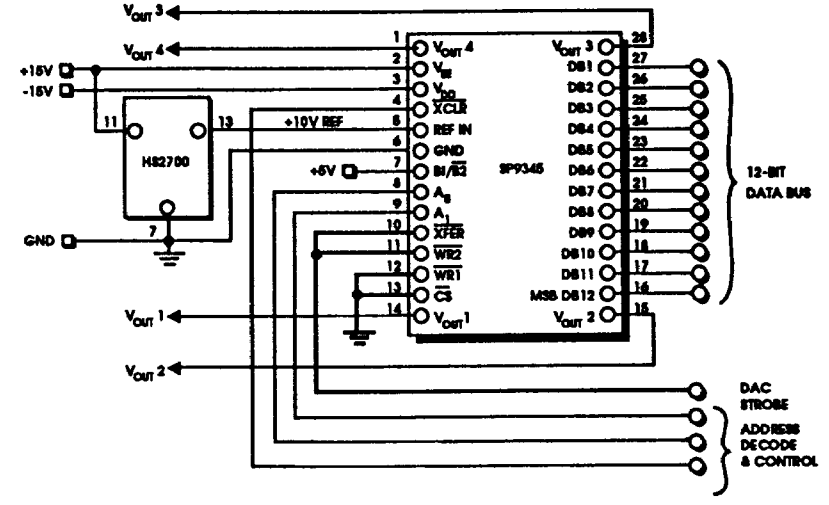
Two Latches, One Latch, or No Latches
The latches can be used in a "semi-" transparent mode, and a "fully-" transparent mode. In order to use the **SP9345** in either mode the user must be interfaced to a 12-bit bus only.

The semi-transparent mode is setup such that the first set of latches is transparent, and the second set is used to latch the incoming data. Data is latched into the second set rather than the first set, in order to minimize glitch energy induced from the data formatting. In this mode $\overline{WR1}$ and $\overline{CS}$ are tied low, and $\overline{WR2}$ and $\overline{XFER}$ are used to strobe the data to the DAC's. Each DAC is addressed using the address lines A_0 and A_1. After the appropriate DAC has been selected and the data is settled at the digital inputs, bringing $\overline{WR2}$ and $\overline{XFER}$ low will transfer the data to the DAC's. The user should be sure to bring $\overline{XFER}$ and $\overline{WR2}$ high again so that the next selected DAC will not be over-written by the last digital code. By strobing $\overline{XFER}$ and $\overline{WR2}$, all four DAC's will be updated simultaneously; however, only the DAC's with changing inputs will appear to change. This mode of operation may be useful in applications where preloading of the input registers is not necessary.

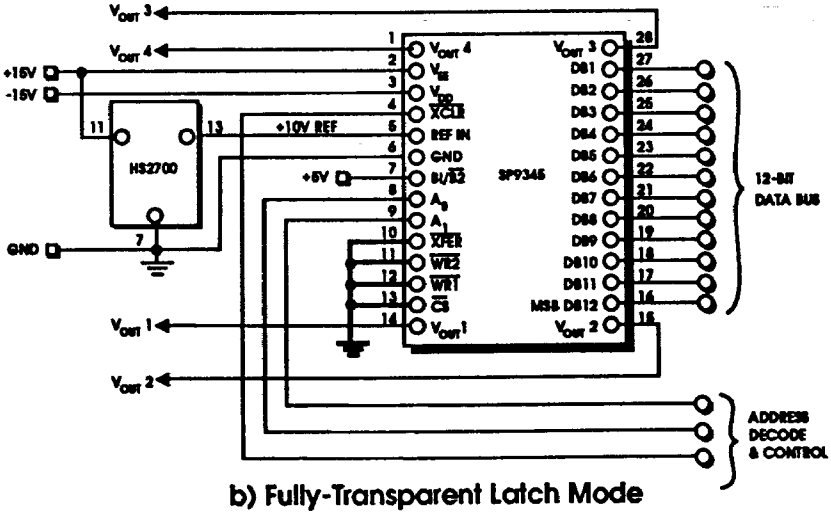
A fully transparent mode is realized by tying $\overline{WR1}$, $\overline{CS}$, $\overline{WR2}$, and $\overline{XFER}$ all low. In this mode anything that is written on the 12-bit data bus will be passed directly to the selected DAC. Since both latches are not being used, the previous digital word will be over-written by the new data as soon as the address changes and the data bus is switched to the appropriate DAC. This may be useful should the user want to calibrate a circuit, by taking full scale or zero scale readings for all four DAC's.

Zeroing DAC Outputs
The DAC outputs can be set to zero volts two different ways. The first involves the $\overline{CLR}$ and $\overline{WR2}$ pins. In normal operation the $\overline{CLR}$ pin is tied high thus disabling the clear function. When this pin is brought low with $\overline{WR2}$, a digital code of 1000 0000 0000 is written to all four DAC inputs, producing a half scale output or zero volts. When the $\overline{CLR}$ pin is brought back high the digital code at the second register will again appear at the DAC digital input, and the analog output will return to its previous corresponding value.

The power-on-reset is especially useful at a system level. Although there will be no damage to the **SP9345** when the unit is powered up while writing to the DAC's and producing an analog output, this may be a problem for other circuitry connected to the DAC outputs. The **SP9345** however can be configured such that during power-up, the second latch will be digitally "zeroed", producing a zero volt output at each of the four DAC outputs. This is achieved by powering the unit up with $\overline{XFER}$ in a high state. Thus, with no external circuitry, the **SP9345** can be powered up with the analog outputs at a known, zero volt output level.



a) Semi-Transparent Latch Mode



b) Fully-Transparent Latch Mode