

FEATURES

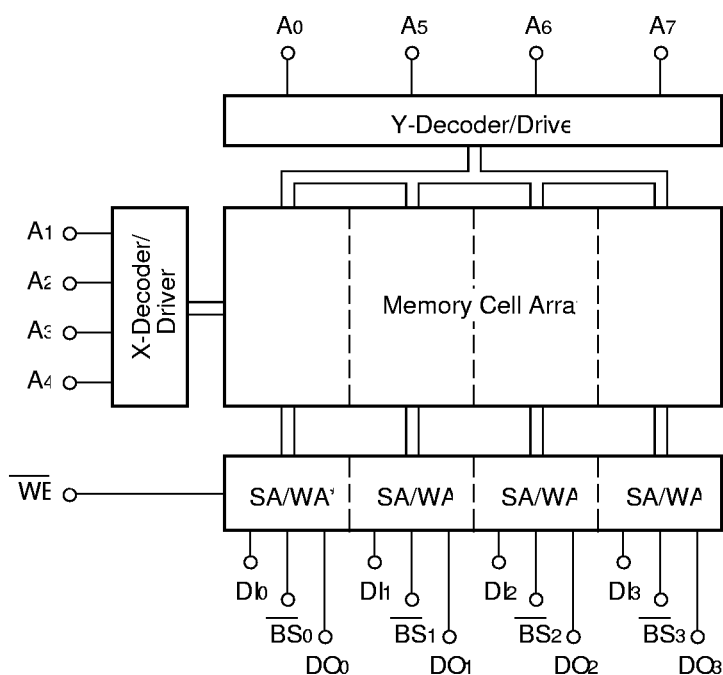
- Address access time, t_{AA} : 3/4/5/7ns max.
- Block select access time, t_{AB} : 2ns max.
- Write pulse width, t_{WW} : 3ns min.
- Edge rate, $t_{r/ff}$: 500ps typ.
- Write recovery times under 5ns
- Power supply current, I_{EE} : -250mA, -200mA for -5/7ns
- Superior immunity against alpha particles provides virtually no soft error sensitivity
- Built with advanced ASSET™ technology
- Fully compatible with industry standard 10K/100K ECL I/O levels
- Noise margins improved with on-chip voltage and temperature compensation
- Open emitter output for easy memory expansion
- Includes popular Block Select function allowing individual read/write control over blocks
- ESD protection of 2000V
- Available in 24-pin hermetic Dip, flatpack and 28-pin MLCC packages

DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 256-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100422 is also supply voltage-compatible with 100K ECL, while the SY101422 operates from 10K ECL supply voltage (-5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

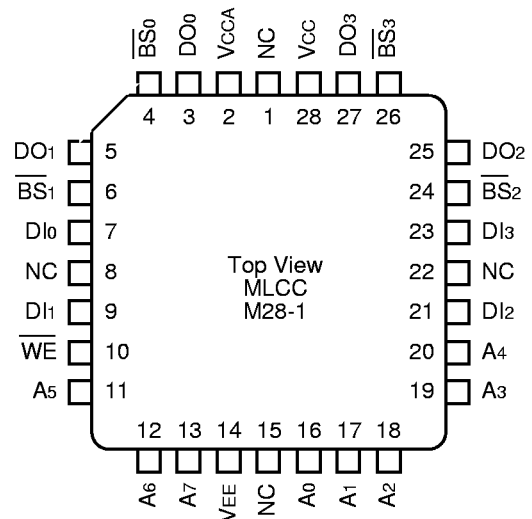
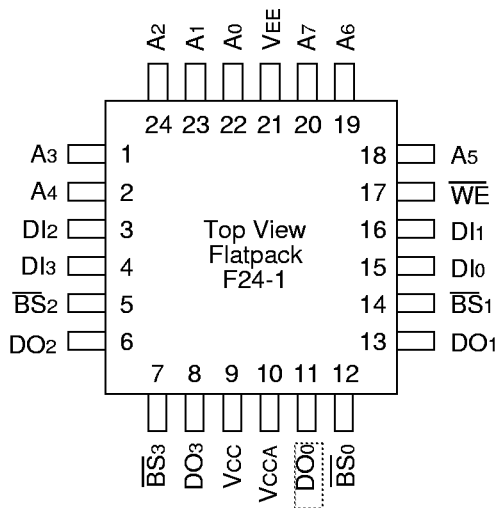
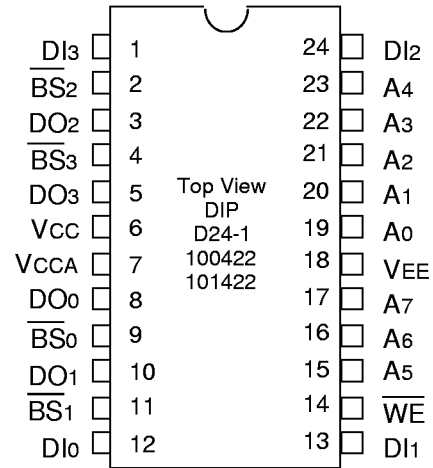
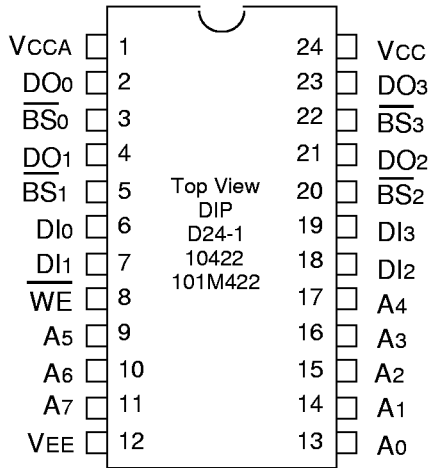
The SY10/100/101422 employ proprietary circuit design techniques and Synergy's proprietary ASSET advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

BLOCK DIAGRAM



* SA = Sense Amplifier
 WA = Write Amplifier

PIN CONFIGURATIONS



PIN NAMES

Label	Function
A ₀ - A ₇	Address Inputs
BS ₀ - BS ₃	Block Select (BS)
WE	Write Enable
DI ₀ - DI ₃	Data Input (DIN)
DO ₀ - DO ₃	Data Output (DOUT)
VCC	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage

TRUTH TABLE

Input			Output	Mode
BS	WE	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

NOTE:

H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care

FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit RAMs organized as four 256-by-1-bit blocks with each block having its own Block Select (\overline{BS}) control signal that functions essentially like a unique chip select for the Block. The four blocks and Block Selects together make the device a 256 x 4-bit RAM. Memory cell selection is achieved by using the 8 address bits designated as A0 through A7. Each of the 2⁸ possible input address combinations corresponds to a unique word location in memory. The active low Block Select (\overline{BS}) control signals are provided for memory expansion and for independent control of each of the four 256 x 1-bit blocks of memory. The active low Write Enable (\overline{WE}) controls the read and write operation on the selected block or blocks. Data resident on the DIN inputs (D0 through D3) is written into the addressed location only when \overline{WE} and the Block Select (\overline{BS}) associated with each of the DIN bits is held LOW. This allows control of the Write operation to any one,

two, three or all four of the input data bits. In order to perform a read operation, \overline{WE} is held high, the Block Select (\overline{BS}) associated with each of the four output blocks is held low, and the non-inverted output data at the addressed location is transferred to DOUT (DO0 through DO3) to be read out. This allows control of the Read operation to any one, two, three or all four of the output blocks. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to -2.0V or an equivalent circuit must be used to provide the specified output levels.

All outputs are forced to a logic LOW level when the RAM is being written into ($\overline{WE} = \text{LOW}$). The output (or outputs) associated with a block (or blocks) of memory can be forced to a logic LOW level by deselecting that block (or blocks) with its respective Block Select input ($\overline{BS}_0 - \overline{BS}_3 = \text{HIGH}$).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VEE	VEE Pin Potential to VCC Pin	+0.5 to -7.0	V
VIN	Input Voltage	+0.5 to VEE	V
IOUT	DC Output Current (Output High)	-30	mA
Tc	Temperature Under Bias	-55 to +125	°C
Tstore	Storage Temperature	-65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

RISE AND FALL TIME

Parameter	Code ⁽¹⁾	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
	S			1500		
Output Fall Time	F	tr	—	500	—	ps
	S			1500		

NOTE:

1. F = Fast Edge Rate
S = Standard Edge Rate

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Supply Voltage ⁽¹⁾	10K	VEE	-5.46	-5.2	-4.94	V
		Tc	0	—	75	°C
Supply Voltage ⁽¹⁾	100K	VEE	-4.8	-4.5	-4.2	V
		Tc	0	—	85	°C
Supply Voltage ⁽¹⁾	101K	VEE	-5.46	-5.2	-4.94	V
		Tc	0	—	85	°C

NOTE:

1. Referenced to Vcc.

CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	CIN	—	4	—	pF
Output Pin Capacitance	COUT	—	5	—	pF

10K DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V; T_c = 0°C to +75°C; V_{EE} = -5.2V; Airflow > 2.5m/s; Output Load = 50Ω to -2.0V

Symbol	Parameter	T _c	Min.	Max.	Unit	Condition
V _{OH}	Output High Voltage	0°C +25°C +75°C	-1000 -960 -900	-840 -810 -720	mV	V _{IN} = V _{IH} Max. or V _{IL} Min.
V _{OL}	Output Low Voltage	0°C +25°C +75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV	V _{IN} = V _{IH} Max. or V _{IL} Min.
V _{OHc}	Output High Voltage	0°C +25°C +75°C	-1020 -980 -920	— — —	mV	V _{IN} = V _{IH} Min. or V _{IL} Max.
V _{OLc}	Output Low Voltage	0°C +25°C +75°C	— — —	-1645 -1630 -1605	mV	V _{IN} = V _{IH} Min. or V _{IL} Max.
V _{IH}	Input High Voltage	0°C +25°C +75°C	-1145 -1105 -1045	-840 -810 -720	mV	Guaranteed Input Voltage High for All Inputs
V _{IL}	Input Low Voltage	0°C +25°C +75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV	Guaranteed Input Voltage Low for All Inputs
I _{IH}	Input High Current	0°C to +75°C	0.0	20	μA	V _{IN} = V _{IH} Max.
I _{IL}	Input Low Current	0°C to +75°C	-2	2	μA	V _{IN} = V _{IL} Min.
I _{IL}	\overline{BS} Input Low Current	0°C to +75°C	30	170	μA	V _{IN} = V _{IL} Min.
I _{IH}	\overline{BS} Input High Current	0°C to +75°C	40	220	μA	V _{IN} = V _{IH} Max.
I _{IL}	\overline{WE} Input Low Current	0°C to +75°C	-2	35	μA	V _{IN} = V _{IL} Min.
I _{IH}	\overline{WE} Input High Current	0°C to +75°C	0.0	60	μA	V _{IN} = V _{IH} Max.
I _{EE}	Power Supply Current -3ns, -4ns -5ns, -7ns	0°C to +75°C	-250 -200	— —	mA	All Inputs and Outputs Open

100K/101K DC ELECTRICAL CHARACTERISTICS

V_{CCA} = 0V
 V_{CC} = 0V

V_{EE} = -4.5V (100K)
 V_{EE} = -5.2V (101K)

T_c = 0°C to +85°C

Airflow > 2.5m/s
 Output Load = 50Ω to -2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
V _{OH}	Output High Voltage	-1025	-880	mV	V _{IN} = V _{IH} Max. or V _{IL} Min.
V _{OL}	Output Low Voltage	-1810	-1620	mV	V _{IN} = V _{IH} Max. or V _{IL} Min.
V _{OHc}	Output High Voltage	-1035	—	mV	V _{IN} = V _{IH} Min. or V _{IL} Max.
V _{OLc}	Output Low Voltage	—	-1610	mV	V _{IN} = V _{IH} Min. or V _{IL} Max.
V _{IH}	Input High Voltage	-1165	-880	mV	Guaranteed Input Voltage High for All Inputs
V _{IL}	Input Low Voltage	-1810	-1475	mV	Guaranteed Input Voltage Low for All Inputs
I _{IH}	Input High Current	0.0	20	μA	V _{IN} = V _{IH} Max.
I _{IL}	Input Low Current	-2	2	μA	V _{IN} = V _{IL} Min.
I _{IL}	\overline{BS} Input Low Current	30	170	μA	V _{IN} = V _{IL} Min.
I _{IH}	\overline{BS} Input High Current	40	220	μA	V _{IN} = V _{IH} Max.
I _{IL}	\overline{WE} Input Low Current	-2	35	μA	V _{IN} = V _{IL} Min.
I _{IH}	\overline{WE} Input High Current	0.0	60	μA	V _{IN} = V _{IH} Max.
I _{EE}	Power Supply Current -3ns, -4ns -5ns, -7ns	-250 -200	— —	mA	All Inputs and Outputs Open

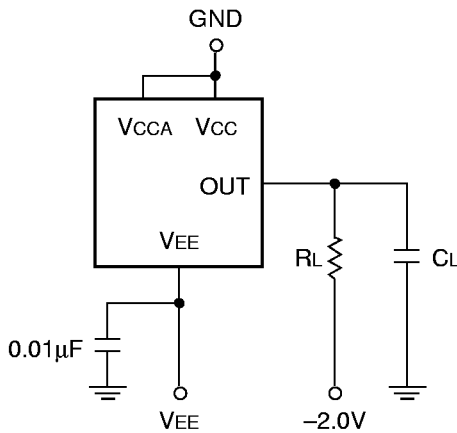
AC ELECTRICAL CHARACTERISTICS

AC TEST CONDITIONS

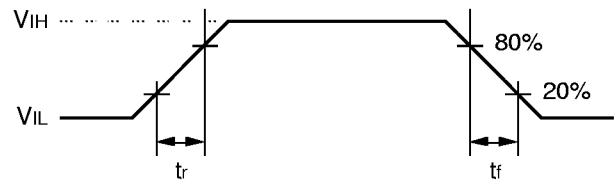
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to $-2.0V$
 $V_{EE} = -5.2V \pm 5\%(10K)$ $T_c = 0^\circ C$ to $+75^\circ C$ (10K)
 $V_{EE} = -4.5V \pm 0.3V(100K)$ $T_c = 0^\circ C$ to $+85^\circ C$ (100K/101K)
 $V_{EE} = -5.2V \pm 5\%(101K)$ Airflow > 2.5m/s

	T_c	V_{IH}	V_{IL}
10K	$0^\circ C$	$-0.933V$	$-1.733V$
	$+25^\circ C$	$-0.90V$	$-1.70V$
	$+75^\circ C$	$-0.863V$	$-1.663V$
100/101K	$0^\circ C$ to $+85^\circ C$	$-0.90V$	$-1.70V$

Loading Condition



Input Pulse



$t_r = t_f = 1.0ns$ typ.

OUTPUT LOAD: $R_L = 50\Omega$
 $C_L = 5pF^*$ (typ.)

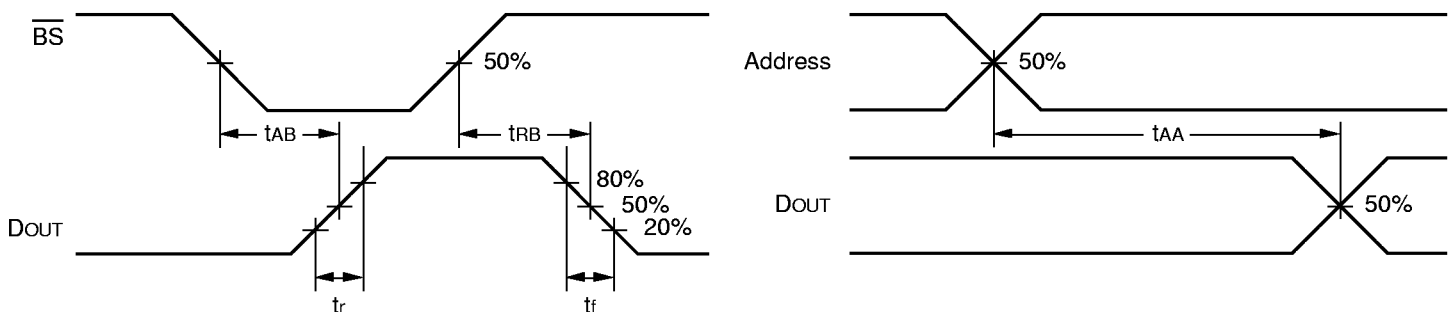
* (Modeled as 50Ω transmission line terminated to $-2V$.)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Symbol	Parameter	SY10422-3 SY100422-3 SY101422-3		SY10422-4 SY100422-4 SY101422-4		SY10422-5 SY100422-5 SY101422-5 SY101M422-5		SY10422-7 SY100422-7 SY101422-7 SY101M422-7		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	TAVQV	Address Access Time	—	3	—	4	—	5	—	7	ns
t_{AB}	TBSLQV	Block Select Access Time	—	2	—	2	—	3	—	3	ns
t_{RB}	TBSHQL	Block Select Recovery Time	—	2	—	2	—	3	—	3	ns

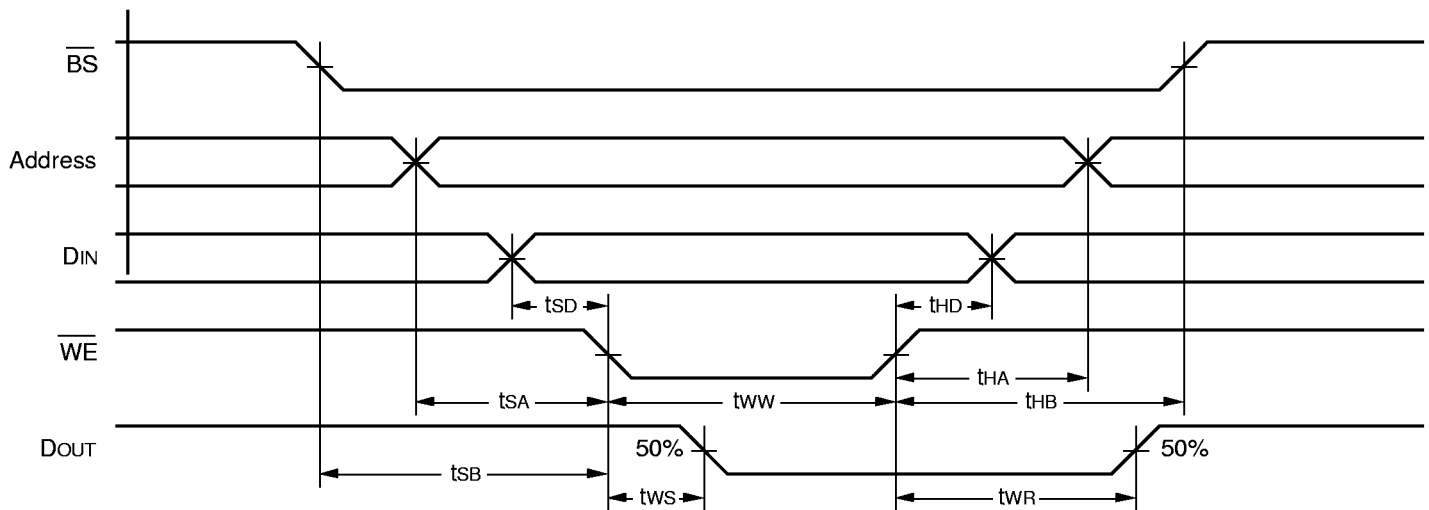
READ CYCLE TIMING DIAGRAM



READ CYCLE

Symbol		Parameter	SY10422-3 SY100422-3 SY101422-3		SY10422-4 SY100422-4 SY101422-4		SY10422-5 SY100422-5 SY101422-5 SY101M422-5		SY10422-7 SY100422-7 SY101422-7 SY101M422-7		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WW}	TWLWH	Write Pulse Width	3	—	4	—	5	—	5	—	ns
t _{WS}	TWLQL	Write Disable Time	—	3	—	4	—	4	—	4	ns
t _{WR}	TWHQV	Write Recovery Time	—	3	—	4	—	4	—	4	ns
t _{SA}	TAVWL	Address Set-Up Time	1	—	1	—	1	—	1	—	ns
t _{SB}	TBSLWL	Block Select Set-Up Time	0	—	0	—	1	—	1	—	ns
t _{SD}	TDVWL	Data Set-Up Time	0	—	0	—	1	—	1	—	ns
t _{HA}	TWHAX	Address Hold Time	1	—	1	—	1	—	1	—	ns
t _{HB}	TWHBSX	Block Select Hold Time	1	—	1	—	1	—	1	—	ns
t _{HD}	TWHDX	Data Hold Time	1	—	1	—	1	—	1	—	ns

WRITE CYCLE TIMING DIAGRAM



PRODUCT ORDERING CODE

Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
3	SY10/100/101422-3FCF	Fast	F24-1	Commercial
	SY10/100/101422-3MCF	Fast	M28-1	Commercial
4	SY10/100/101422-4FCF	Fast	F24-1	Commercial
	SY10/100/101422-4MCF	Fast	M28-1	Commercial
5	SY10/100/101422-5DCS	Standard	D24-1	Commercial
	SY10/100/101422-5FCS	Standard	F24-1	Commercial
	SY10/100/101422-5JCS	Standard	J28-1	Commercial
	SY10/100/101422-5JCSTR	Standard	J28-1	Commercial
	SY101M422-5DCS	Standard	D24-1	Commercial
7	SY10/100/101422-7DCS	Standard	D24-1	Commercial
	SY10/100/101422-7FCS	Standard	F24-1	Commercial
	SY10/100/101422-7JCS	Standard	J28-1	Commercial
	SY10/100/101422-7JCSTR	Standard	J28-1	Commercial
	SY101M422-7DCS	Standard	D24-1	Commercial

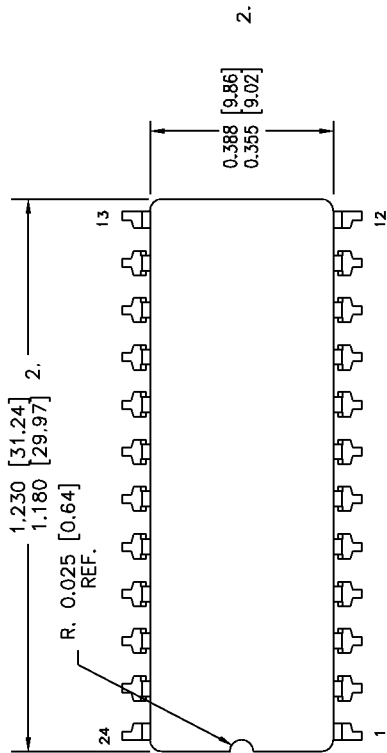
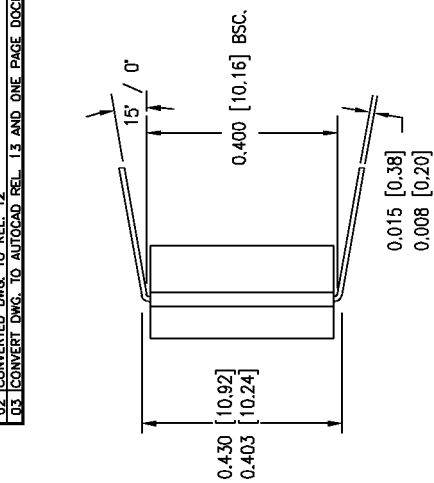
24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERT DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 13 AND ONE PAGE DOCUMENT.	10/27/98/99



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-960-9191
FAX: 408-967-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	N/A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

24 LEAD CERDIP (.400" WIDE)
PACKAGE OUTLINE

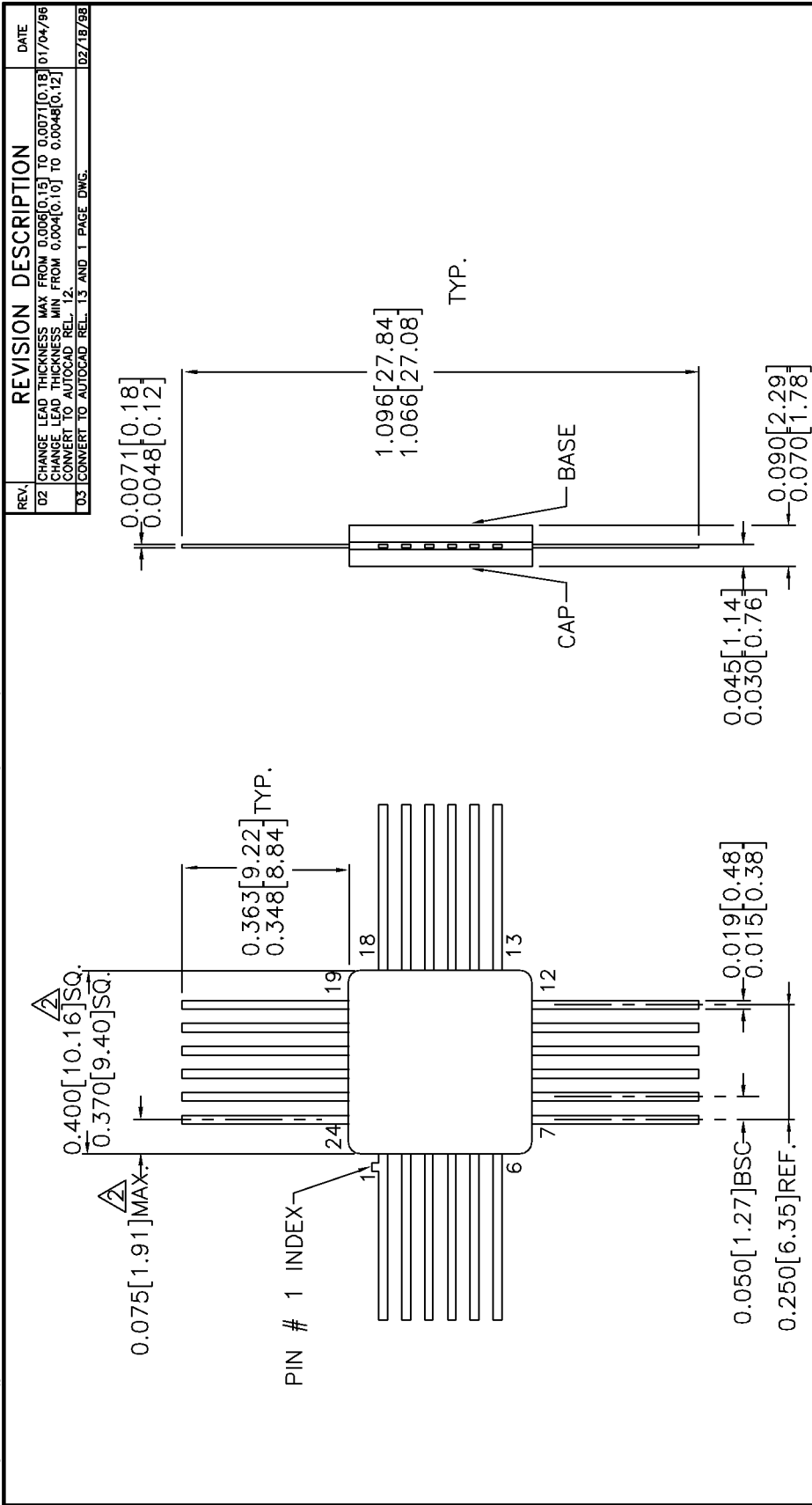
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24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.008[0.15] TO 0.0071[0.18] CHANGE LEAD THICKNESS MIN FROM 0.004[0.10] TO 0.0048[0.12] (CONVERT TO AUTOCAD REL. 12.)	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98

APPROVALS	DATE	APPROVALS	DATE	SIZE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO		

SCALE	REVISION
N/A	03

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24 LEAD CERPACK
PACKAGE OUTLINE

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RELEASE DATE:

NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

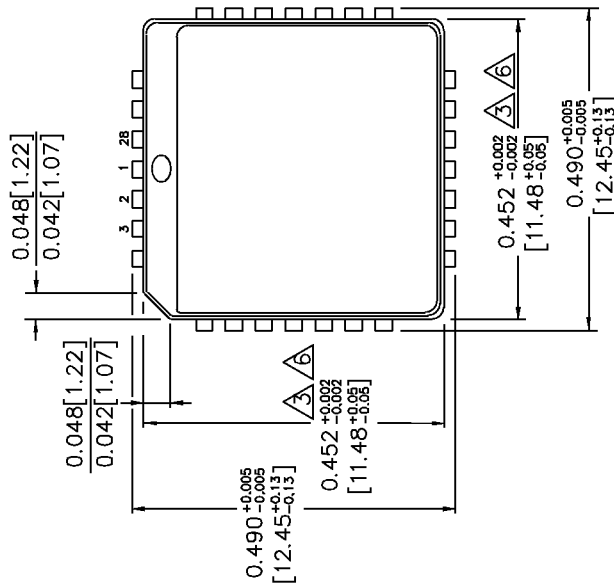
FILE/REV #: PD0008A03

PD/0008/ASCORP

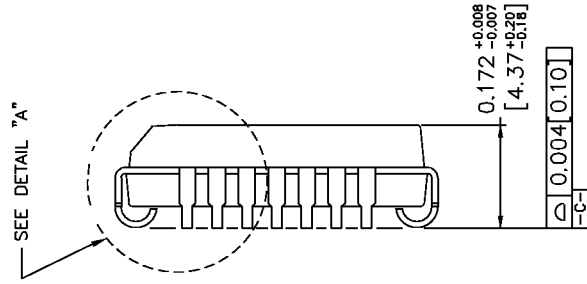
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

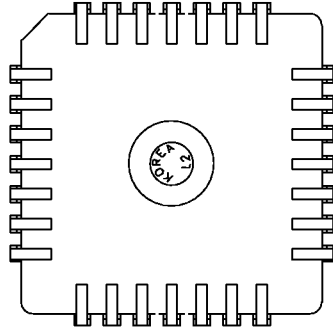
TOP VIEW



SIDE VIEW

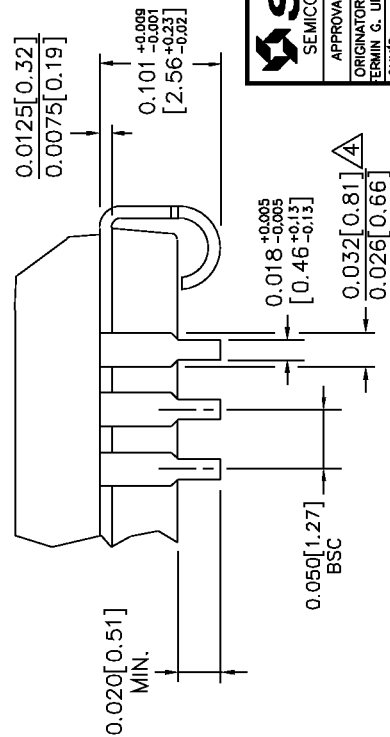


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: TERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

SCALE
 N/A
 REVISION
 03

DETAIL "A"

28 LEAD METAL QUAD PLASTIC LEADER CHIP CARRIER (M28-1)

FILE/REV #: PD0023A05

PD/0023/ASCORP

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