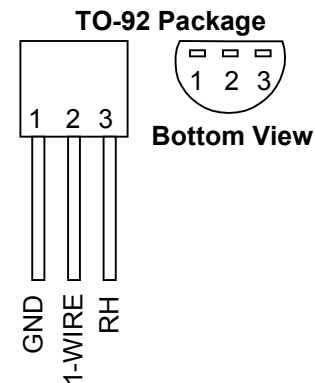
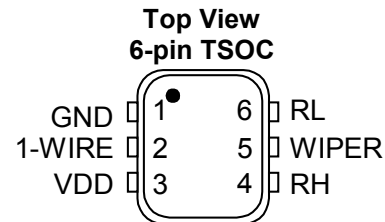


FEATURES

- Single element 256-position linear taper potentiometer
- Supports potentiometer terminal working voltages up to 11V
- Potentiometer terminal voltage independent of supply voltage
- Potentiometer wiper position controlled and read over minimal 1-Wire bus interface
- 100 kΩ resistor element value
- T0-92 package provides a 1-Wire® variable resistor configuration
- Supports Conditional Search based on power-on default wiper position
- Multiple DS2890's can be identified on a common 1-Wire bus and operated independently
- Unique factory lasered 64-bit registration number assures error free device selection and absolute part identity
- Built-in multi-drop controller ensures compatibility with other 1-Wire Network products
- Supports Overdrive mode which boosts communication speed up to 142 kbits per second
- -40°C to +85°C operating temperature range
- 2.8V – 6.0V operating voltage range

PIN ASSIGNMENT



Visit www.dalsemi.com for Flip Chip pinout and mechanical data.

ORDERING INFORMATION

PART NUMBER	RESISTANCE*	PACKAGE DESCRIPTION
DS2890-000	100 kΩ	T0-92
DS2890P-000	100 kΩ	6-pin TSOC
DS2890X-000	100 kΩ	Flip Chip Pkg., Tape & Reel
DS2890-000/T&R	100 kΩ	Tape & Reel of DS2890
DS2890P-000/T&R	100 kΩ	Tape & Reel of DS2890P

* Contact the factory for availability of alternate resistance values

1-Wire is a registered trademark of Dallas Semiconductor.

PIN DESCRIPTION

SIGNAL NAME	TYPE	FUNCTION
1-WIRE	I/O	1-Wire bus interface. Open drain, requires external pull-up resistor. Range: 2.8V – 6.0V. See HARDWARE CONFIGURATION for pull-up resistor recommendations.
RH	I/O	High end terminal of potentiometer resistor element. Range: 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
RL	I/O	Low end terminal of potentiometer resistor element. Range: 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
WIPER	I/O	Potentiometer wiper terminal. Range 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
V_{DD}	PWR	Auxiliary power supply input. Range: 2.8V – 6.0V
GND	PWR	Ground

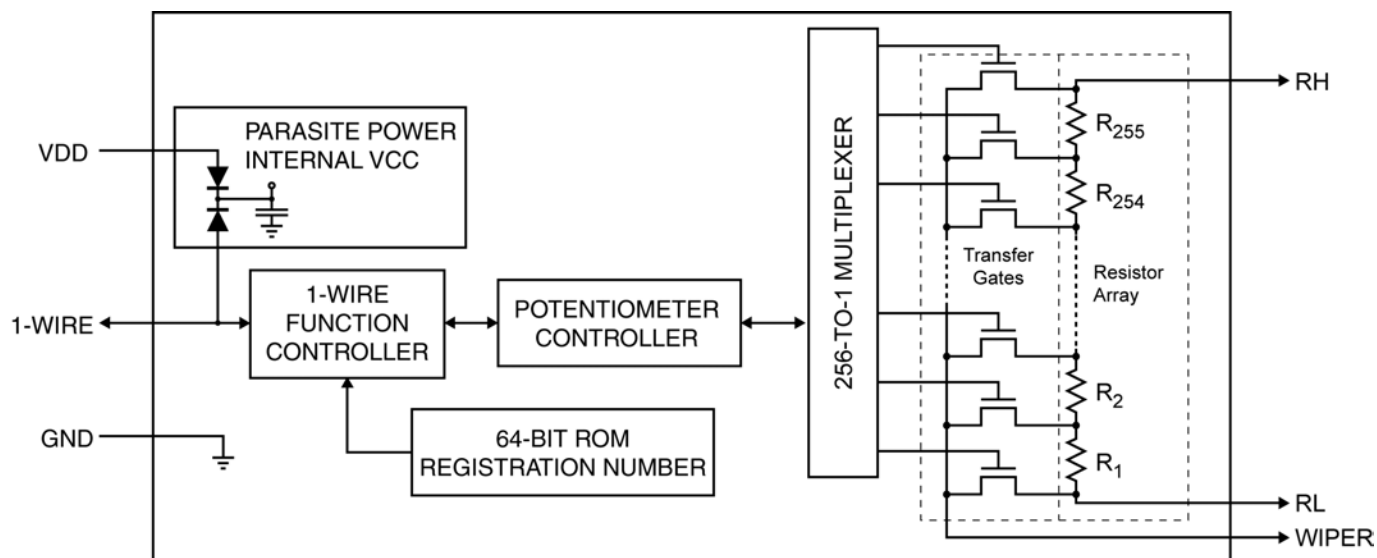
DESCRIPTION

The DS2890 is a linear taper digitally controlled potentiometer with 256 wiper positions. Device operation, including wiper position, is controlled over the single contact 1-Wire bus for the ultimate in electrical interface simplicity. With a wide 0–11 volt working voltage range for the potentiometer terminals, the DS2890 is ideal for a broad range of industrial and control applications. Potentiometer terminal voltage is independent of device supply voltage as well as the voltage applied to the other potentiometer terminals. Communication with the DS2890 follows the standard Dallas Semiconductor 1-Wire protocol and can be accomplished with minimal hardware such as a single port pin of a microcontroller. Multiple DS2890 devices can reside on a common 1-Wire bus and be operated independently of each other. Each DS2890 has its own unalterable 64-bit ROM registration number that is factory lasered into the chip. The registration number guarantees unique identification for absolute traceability and is used to address the device in a multi-drop 1-Wire Network environment. The DS2890 will respond to a 1-Wire Conditional Search command if the potentiometer wiper is set at the power-on default position. This feature enables the bus master to easily determine whether a potentiometer has gone through a power-on reset and needs to be re-configured with a required wiper position setting. The DS2890 supports two power modes: a) 1-Wire only mode in which device power is supplied parasitically from the 1-Wire and b) V_{DD} mode where power is supplied from an external supply. With a V_{DD} supply the device can support both a potentiometer and variable resistor configuration. When operating in a 1-Wire only power mode the device supports only a variable resistor configuration.

OPERATION

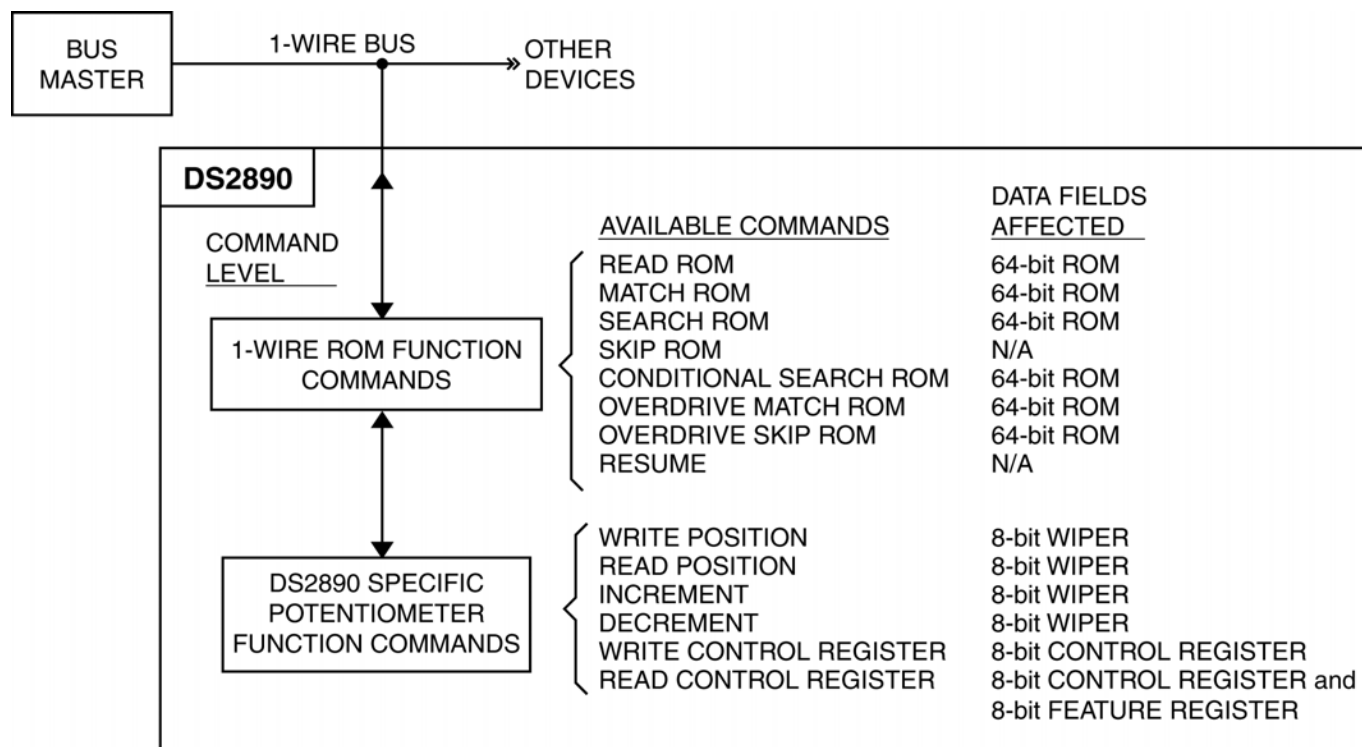
The DS2890 is a single element digital potentiometer; a block diagram of the device is shown in Figure 1. The device has a total of 256 linearly spaced tap points including the RL and RH terminals; a total of 255 resistive segments exist between the RL and RH terminals. These tap points are accessible to the WIPER terminal whose position is controlled via the 1-Wire bus interface. Wiper position and device state are maintained as long as the 1-Wire bus is active or the V_{DD} supply is applied within operating limits. Otherwise, a power-on reset will occur and the wiper position and operating state will return to power-on default conditions.

FIGURE 1. DS2890 BLOCK DIAGRAM



As shown in the figure the device has five major elements: the 1-Wire Function Controller, the Potentiometer Controller, the 64-bit ROM, the resistor array, and Parasite Power circuitry. Each of these elements is discussed in detail throughout the remainder of the data sheet. DS2890 control including device selection, positioning/reading the potentiometer wiper, and device operating state is performed over the 1-Wire bus. The hierarchical structure of the 1-Wire protocol as applicable to the DS2890 is shown in Figure 2. As shown, the control sequence starts with the 1-Wire bus master issuing one of eight ROM function commands. After a ROM function command is successfully completed potentiometer functions may be executed. The protocol for ROM and potentiometer functions are described in the “COMMAND FLOW” section. For the 3-pin TO-92 package configuration and operation see the “TO-92 PACKAGE OPERATION” section.

FIGURE 2. 1-Wire Command Hierarchical Structure



DATA I/O BIT ORDER

All data is read and written least significant bit (LSB) first.

POTENTIOMETER FEATURE REGISTER

Although the feature set of the DS2890 is primarily fixed, a mechanism to identify feature characteristics of future 1-Wire potentiometers has been developed and implemented in the DS2890. As shown in Figure 3, the feature register is an encoded read-only byte that describes the characteristics of the DS2890 and future 1-Wire potentiometers. Feature values that correspond to the DS2890 are highlighted. The feature register is read with the READ CONTROL REGISTER potentiometer function command (see "POTENTIOMETER FUNCTION COMMANDS").

FIGURE 3. 1-WIRE POTENTIOMETER FEATURE REGISTER

Feature Register Bit Encoding

b7	b6	b5	b4	b3	b2	b1	b0
PR		NWP		NP		WSV	PC

Feature Register Bit Definitions

Feature Description	Bit(s)	Definition
PC: potentiometer characteristic	b0	If 0: logarithmic potentiometer element(s) If 1: linear potentiometer element(s)
WSV: wiper setting volatility	b1	If 0: wiper setting(s) are non-volatile If 1: wiper setting(s) are volatile
NP: number of potentiometers	b3..b2	2 bit binary value representing number of potentiometers: If 00b: 1 potentiometer If 01b: 2 potentiometers If 10b: 3 potentiometers If 11b: 4 potentiometers
NWP: number of wiper positions	b5..b4	2 bit binary value representing number of wiper positions for each potentiometer: If 00b: 32 positions If 01b: 64 positions If 10b: 128 positions If 11b: 256 positions
PR: potentiometer resistance	b7..b6	2 bit binary value representing potentiometer resistance: If 00b: 5 k Ω If 01b: 10 k Ω If 10b: 50 k Ω If 11b: 100 k Ω

DS2890 feature values are highlighted: value

The DS2890 will respond with a feature register value of F3h when a READ CONTROL REGISTER command is executed, see section “POTENTIOMETER FUNCTION COMMANDS”.

POTENTIOMETER CONTROL REGISTER

The potentiometer control register is used to turn on/off the DS2890 charge pump (see section “POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS” for a discussion of the charge pump) and has control capabilities for future 1-Wire potentiometers that could contain multiple resistor elements. The format of the control register is shown in Figure 4.

FIGURE 4. POTENTIOMETER CONTROL REGISTER

Control Register Bit Encoding

b7	b6	b5	b4	b3	b2	b1	b0
X	CPC	X	X	\overline{WN}		WN	

Control Register Bit Definitions*

Description	Bit(s)	Definition
WN: wiper number to control	b1..b0	2 bit binary value representing the potentiometer wiper to control: If 00b: potentiometer 1 wiper If 01b: potentiometer 2 wiper If 10b: potentiometer 3 wiper If 11b: potentiometer 4 wiper
\overline{WN} : inverted wiper number to control	b3..b2	1's complement of potentiometer wiper to control: If 11b: potentiometer 1 wiper If 10b: potentiometer 2 wiper If 01b: potentiometer 3 wiper If 00b: potentiometer 4 wiper
CPC: charge pump control	b6	If 0: the charge pump is OFF If 1: the charge pump is ON
X: don't care.	b4,b5,b7	These bits are reserved for future use by Dallas Semiconductor. These bits should be written to a value of 0.

*Note:

Control Register power-on defaults: Charge Pump is OFF (CPC=0), Wiper Number to control is wiper #1 (WN=00b, \overline{WN} =11b).

Valid DS2890 control values are highlighted: value

Thus for the DS2890, valid control register values are:

Control Register Value	Description
00001100b	charge pump off, potentiometer #1 wiper selected
01001100b	charge pump on, potentiometer #1 wiper selected

As shown in Figure 22 and discussed in the "POTENTIOMETER FUNCTION COMMANDS" section, no change in device state will occur if an invalid control register value is sent.

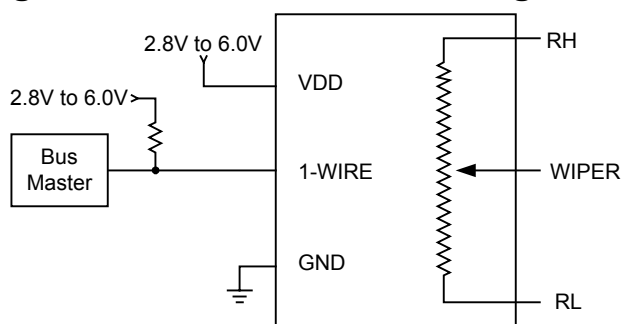
POWER and CONFIGURATION CONSIDERATIONS

1-Wire devices can typically derive operating power entirely from the 1-Wire bus by storing energy on an internal capacitor during periods of time when the 1-Wire bus is in a high state. During bus low times the device continues to operate from the energy stored on the internal capacitor; the capacitor is then recharged when the bus returns to a high state. This technique of operating entirely from the 1-Wire bus by powering from energy stored on an internal capacitor during bus low times is known as “parasite powered” operation. Special consideration is required with the DS2890 in that it supports two power configurations and two related digital resistor modes: Potentiometer Configuration and Variable Resistor Configuration. The Potentiometer Configuration requires the presence of a VDD power source to supply the power needs of the device charge pump which must be turned on to support a terminal-to-terminal wiper output range. The Variable Resistor configuration is supported with or without a VDD source or enabled charge pump although resistance range, as described below, is influenced by the charge pump state.

POTENTIOMETER CONFIGURATION

To configure and operate the DS2890 as a potentiometer as shown in Figure 5 requires the TSOC or flip chip package, a VDD power source, and the device charge pump turned on (Control Register, bit CPC=1). The charge pump **must be enabled** to support RL to RH terminal voltage swings at the WIPER output and as described previously, a VDD supply **must** be provided to support the power requirements of the charge pump.

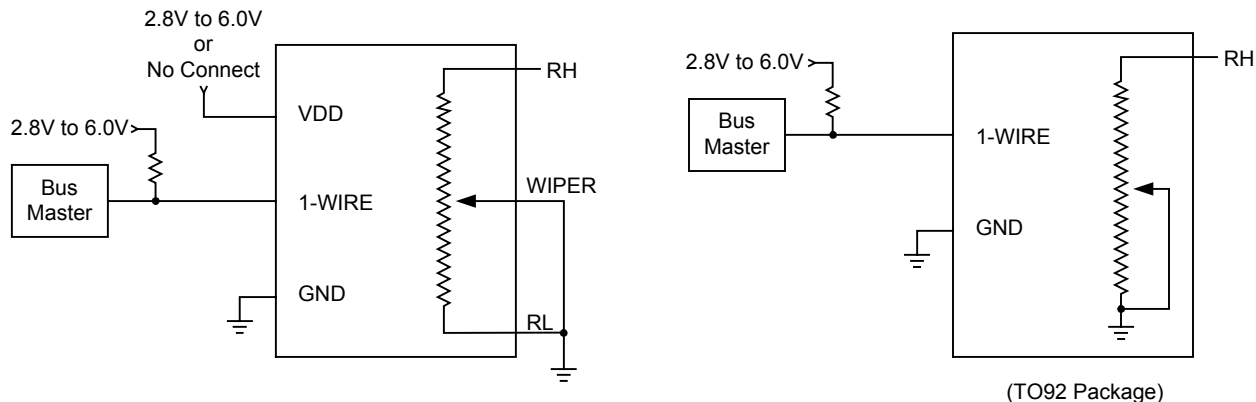
Figure 5. Potentiometer Configuration



VARIABLE RESISTOR CONFIGURATION

The Variable Resistor configuration as shown in Figure 6 is supported by all package types with or without an external VDD supply. As described previously, without a VDD source the charge pump **must** be disabled.

Figure 6. Variable Resistor Configurations



WIPER RESISTANCE CONSIDERATIONS

A simplified diagram of the DS2890 resistor array for the potentiometer configuration is shown in **FIGURE 8**. In this figure the r_{DS} resistance of the wiper transistors in Figure 1 are modeled as wiper resistance R_{WIPER} . The value of R_{WIPER} varies with device configuration, operational state, and wiper terminal voltage. Wiper resistance is significantly reduced when an external VDD supply is used and the device charge pump is enabled. A wiper resistance graph with the charge pump enabled is shown in **FIGURE 10**.

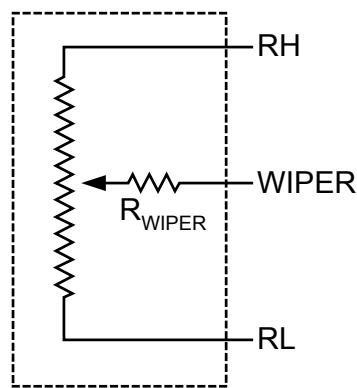
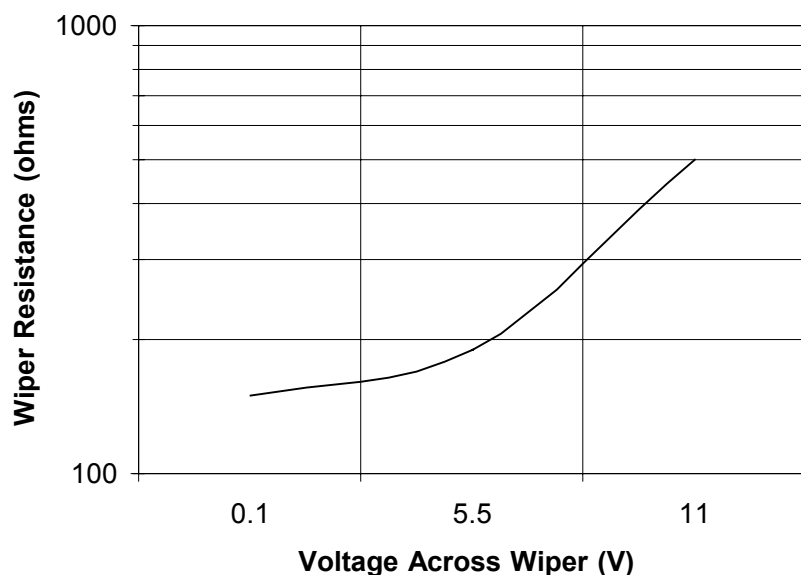


FIGURE 8. Potentiometer Resistor Model

**FIGURE 10. Typical Wiper Resistance vs Wiper Voltage at 25°C,
Charge Pump ON**



When packaged in a 3-pin TO-92 or configured as a variable resistor, the DS2890 takes on a configuration as shown in **FIGURE 11**, a simplified model is shown in Figure 12. As shown, the RL and Wiper terminals and are connected to GND and the resistance between the RH terminal and GND is varied. As described previously, the DS2890 charge pump must be turned off (default state) for operation with the TO-92 package or when VDD is not applied. Wiper resistance for a configuration with the charge pump disabled is shown in **FIGURE 13**.

FIGURE 11. DS2890 TO-92 CONFIGURATION BLOCK DIAGRAM

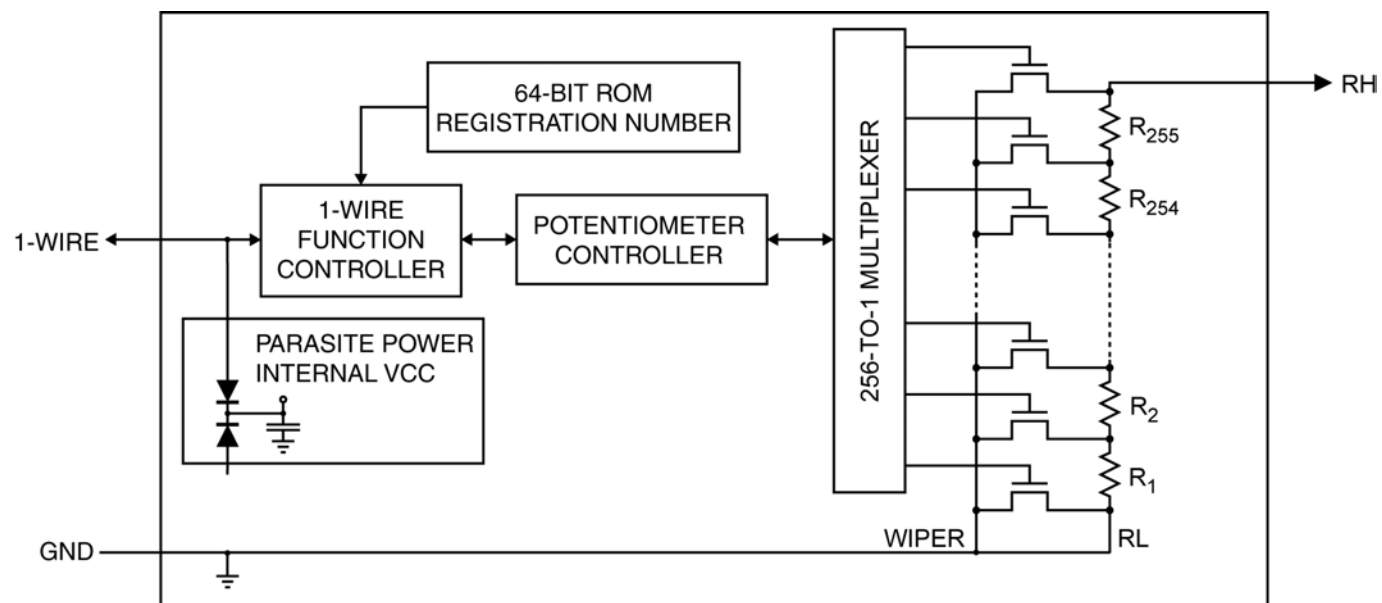
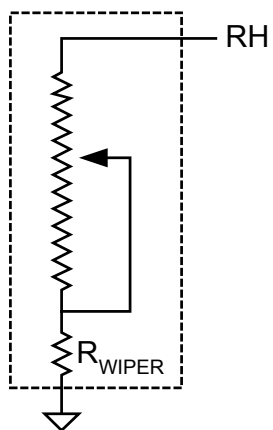
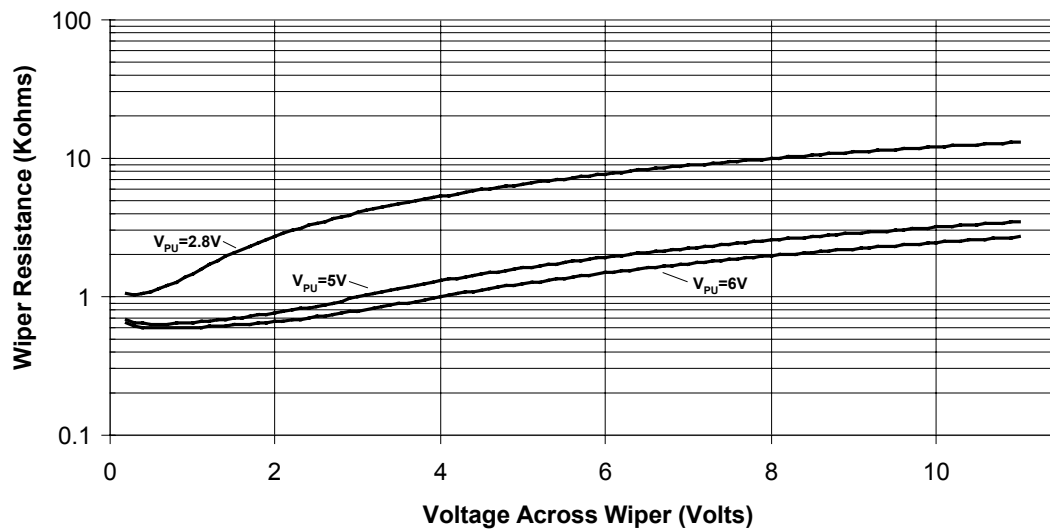


Figure 12. VARIABLE RESISTOR MODEL



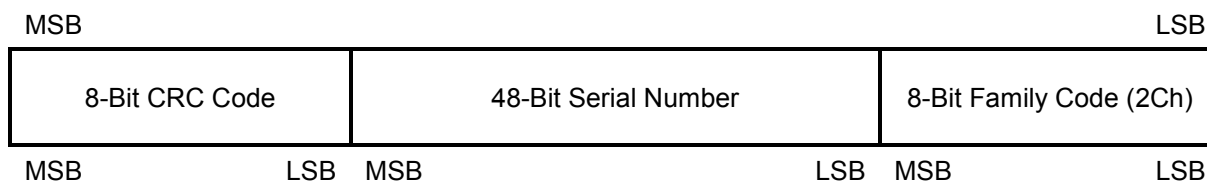
**FIGURE 13. Typical Wiper Resistance vs Wiper Voltage at 25°C,
Charge Pump OFF**



64-BIT LASERED ROM

Each DS2890 contains a unique and unalterable lasered ROM registration number that is 64 bits long; the format of this value is shown in Figure 15. The first 8 bits are a 1-Wire family code; the family code for the DS2890 and future 1-Wire Potentiometers is 2Ch. The next 48 bits are a unique serial number that is administered by Dallas Semiconductor. The last 8 bits are a CRC of the first 56 bits. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 16. Operationally, the CRC generator works as follows: The shift register bits are first initialized to zero. Then starting with the least significant bit, the 8-bit family code is shifted in. After the 8th bit of the family code has been entered, the 48-bit serial number is shifted in. After shifting in the 48th bit of the serial number the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to an all zeros value. The 64-bit ROM and the 1-Wire Function Controller portions of the DS2890 allow the device to operate as a 1-Wire device and follow the protocol detailed in the section “TRANSACTION SEQUENCE”.

FIGURE 15. 64-BIT LASERED ROM



READ CONTROL REGISTER [AAH]

The Read Control Register command is used to obtain both the Control Register and potentiometer Feature Register. Following the Read Control Register command byte, the bus master reads 16 bits to obtain first the Feature Register byte and then the Control Register byte. The DS2890 will respond with 0's to additional reads after the 8 bit of the Control Register byte. The Read Control Register command is terminated with a Reset pulse.

WRITE CONTROL REGISTER [55H]

The Write Control Register command is used to manipulate DS2890 state bits located in the Control Register. This command is used to set the potentiometer wiper address and charge pump state. The bus master follows the Write Control Register command byte with an 8-bit register value. Following the 8th bit of the register byte, the bus master reads back the 8-bit control value from the DS2890 to confirm that the device received the correct value (Note that if an invalid register value was received by the DS2890, the bus master will read all 1's (FFh) during the read back sequence.). If a value other than FFh is read, the bus master determines if the DS2890 received the correct value. If an incorrect value is read back, the bus master must issue a Reset pulse and repeat the sequence. If the value read back is correct, the bus master then sends the 8-bit release code (96h). If the DS2890 accurately receives the release code, the Control Register is updated and the device will respond with 0's to additional reads by the bus master. If an invalid release code is received, no change is made to the Control Register and the device will respond with 1's to additional reads by the bus master. The Write Control Register command is terminated with a Reset pulse.

INCREMENT [C3H]

The Increment command is used for a one step position increase of the currently addressed potentiometer wiper. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. The bus master follows the Increment command byte with an 8-bit read to which the DS2890 will respond with the new 8-bit wiper position set point. No position change is made if the DS2890 wiper is at the maximum position (FFh) and an Increment command is received. One difference between the Increment/Decrement commands and other potentiometer functions is that upon completion of either of these commands, 1-Wire command processing remains at the potentiometer function level. As shown in Figure 21, additional potentiometer commands may be sent without going through the ROM function flow.

DECREMENT [99H]

The Decrement command is used for a one step position decrease of the currently addressed potentiometer wiper. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. The bus master follows the Decrement command byte with an 8-bit read to which the DS2890 will respond with the new 8-bit wiper position set point. No position change is made if the DS2890 wiper is at the minimum position (00h) and a Decrement command is received. One difference between the Increment/Decrement commands and other potentiometer functions is that upon completion of either of these commands, 1-Wire command processing remains at the potentiometer function level. As shown in Figure 21, additional potentiometer commands may be sent without going through the ROM function flow.

1-WIRE BUS SYSTEM

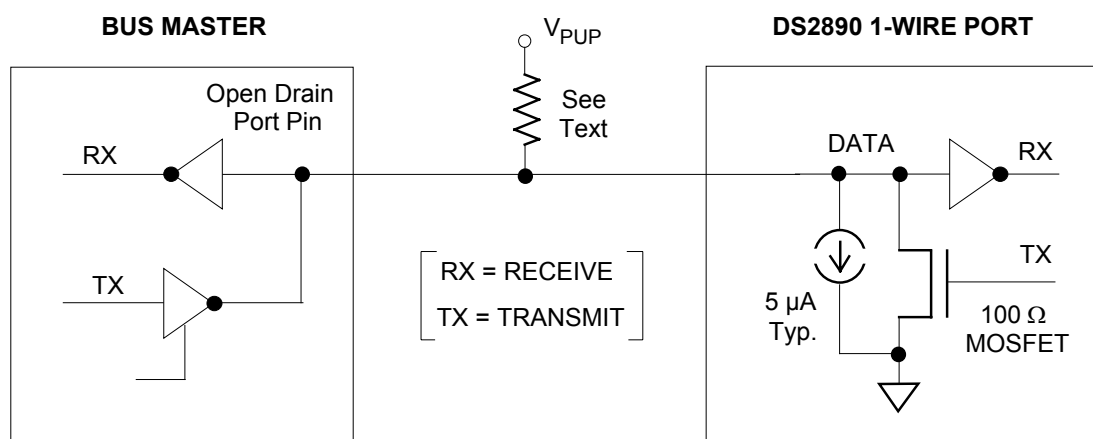
The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the DS2890 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2890 is open drain with an internal circuit equivalent to that shown in Figure 9. A multi-drop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive Mode. For a discrete bus master interface as in Figure 17, the 1-Wire bus requires a pull-up resistor with a minimum value of 2.2 k Ω . Depending on 1-Wire communication speed, regular or overdrive, and bus load characteristics, the optimal pull-up resistor value will be in the 1.5 k Ω to 5 k Ω range. Figure 18 shows a DS2480B bus master configuration with an interface to the host CPU serial port. Among many features, the DS2480B simplifies the 1-Wire interface design, generates slew-rate controlled 1-Wire waveforms, and off-loads 1-Wire timing generation overhead required in a discrete solution.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 μ s (Overdrive Speed) or more than 120 μ s (regular speed), one or more devices on the bus may be reset.

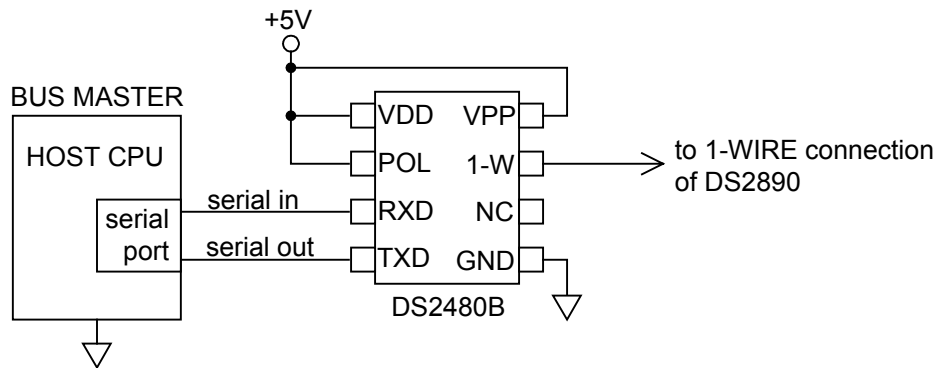
FIGURE 17. HARDWARE CONFIGURATION



NOTE:

Depending on 1-Wire communication speed, regular or overdrive, and bus load characteristics, the optimal pull-up resistor value will be in the 1.5 k Ω to 5 k Ω range.

FIGURE 18. BUS MASTER WITH DS2480B DRIVER



TRANSACTION SEQUENCE

The protocol for accessing the DS2890 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Potentiometer Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2890 is on the bus and is ready to operate. For more details, see the “1-WIRE SIGNALING” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS2890 supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to Figure 23 and Figure 24 flowcharts):

READ ROM [33H]

This command allows the bus master to read the DS2890’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number read by the master will be invalid.

MATCH ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2890 on a multi-drop bus. Only the DS2890 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0H]

When a multi-drop system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the 64-bit ROM code of one device. Additional passes will identify the ROM codes of the remaining devices.

CONDITIONAL SEARCH ROM [ECH]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified search condition will participate in the search. The device condition that will cause individual DS2890s to participate in a Conditional Search is a wiper position located at the power-on default setting (00h). This feature enables the bus master to easily determine whether a potentiometer has gone through a power-on reset and needs to be re-configured with a required wiper position setting.

SKIP ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access potentiometer functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wired-AND result).

OVERDRIVE SKIP ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2890 in the Overdrive Mode. All communication following this command code has to occur at Overdrive Speed until a reset pulse of minimum 480 μ s duration resets all devices on the bus to regular speed.

When issued on a multi-drop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the search process. If more than one Overdrive-supporting slave is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

OVERDRIVE MATCH ROM [69H]

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS2890 on a multi-drop bus and to simultaneously set it in Overdrive Mode. Only the DS2890 that exactly matches the 64-bit ROM sequence will respond to the subsequent potentiometer function command. Slaves already in Overdrive mode from a previous Overdrive Skip or a successful Overdrive Match command will remain in Overdrive mode. All Overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480 μ s duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

RESUME COMMAND [A5H]

In a typical application the DS2890 may be accessed several times to complete a control adjustment. In a multi-drop environment this means that the 64-bit ROM sequence of a Match ROM command has to be repeated for every access. To maximize the data throughput in a multi-drop environment the Resume Command function was implemented. As shown in Figure 24, this function checks the status of the RC flag and, if it is set, directly transfers control to the potentiometer functions, similar to a Skip ROM command. The only way to set the RC flag is through successfully executing the Match ROM, Search ROM, Conditional Search ROM, or Overdrive Match ROM command. Once the RC flag is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus will clear the RC flag, preventing two or more devices from simultaneously responding to the Resume Command function.

POTENTIOMETER FUNCTION EXAMPLE

At regular speed with an auxiliary supply (V_{DD} within range): turn on the charge pump, set the wiper position to mid-point, increment the wiper twice, and decrement the wiper once.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset Pulse (480 - 960 μ s)
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command
TX	55h	Issue Write Control Register Command
TX	4Ch	Issue Control Register value for WN=0, CPC=1
RX	<data byte>	Read back Control Register value (4Ch) and verify
TX	96h	Issue Release Code to update Control Register
RX	<data bits>	If 0's are read, update was successful; if 1's are read, the update failed
TX	Reset	Reset Pulse (480 - 960 μ s)
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command
TX	0Fh	Issue Write Position Command
TX	7Fh	Write Wiper Position value
RX	<data byte>	Read back Wiper Position byte and verify
TX	96h	Issue Release Code to update Wiper Position
RX	<data bits>	If 0's are read, update was successful; if 1's are read, the update failed
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	C3h	Issue Wiper Increment Command
RX	<data byte>	Read new wiper position
TX	C3h	Issue Wiper Increment Command
RX	<data byte>	Read new wiper position
TX	99h	Issue Wiper Decrement Command
RX	<data byte>	Read new wiper position
TX	Reset	Reset Pulse

1-WIRE SIGNALING

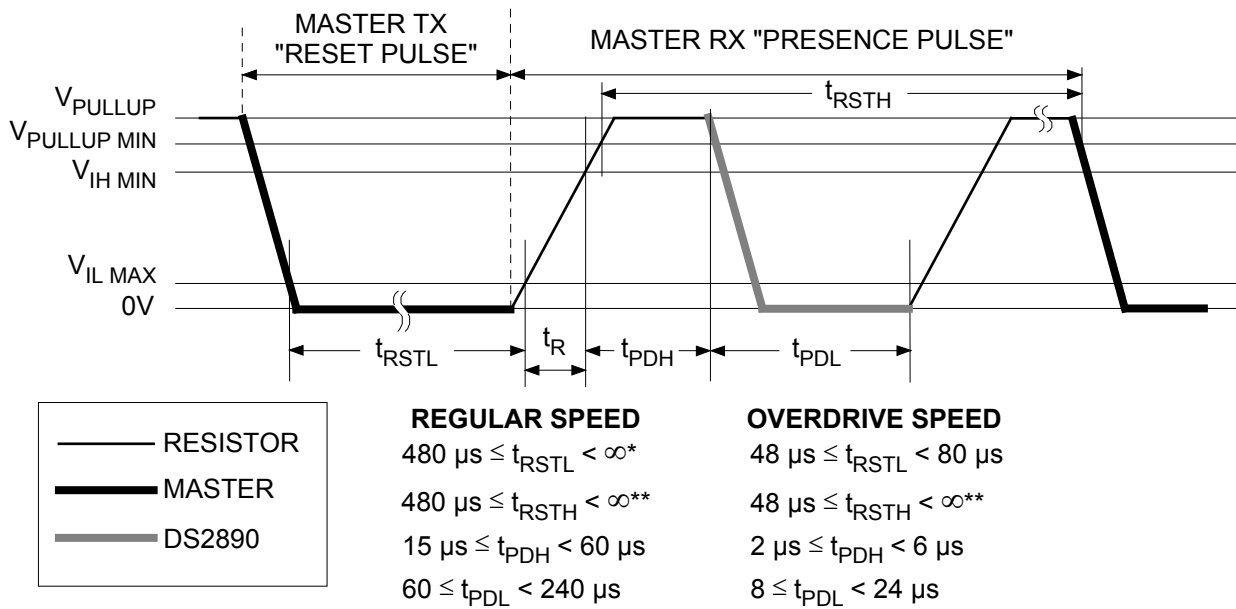
The DS2890 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. Except for the presence pulse the bus master initiates all these signals. The DS2890 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS2890 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all waveforms.

The initialization sequence required to begin any communication with the DS2890 is shown in Figure 19. A Reset Pulse followed by a Presence Pulse indicates the DS2890 is ready to send or receive data. The bus master transmits (TX) a reset pulse (t_{RSTL} , minimum 480 μ s at regular speed, 48 μ s at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pull-up resistor. After detecting the rising edge on the data contact, the DS2890 waits (t_{PDH} , 15-60 μ s at regular speed, 2-6 μ s at Overdrive speed) and then transmits the Presence Pulse (t_{PDL} , 60-240 μ s at regular speed, 8-24 μ s at Overdrive Speed). A Reset Pulse of 480 μ s or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2890 is in Overdrive Mode and the Reset Pulse is no longer than 80 μ s the device will remain in Overdrive Mode.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 20 (a-c). The master initiates all time slots by driving the data line low. The falling edge of the data line synchronizes the DS2890 to the master by triggering an internal timing circuit. During write time slots, the timing circuit determines when the DS2890 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the timing circuit determines how long the DS2890 will hold the data line low. If the data bit is a “1”, the DS2890 will not hold the data line low at all.

FIGURE 19. INITIALIZATION PROCEDURE “RESET AND PRESENCE PULSES”

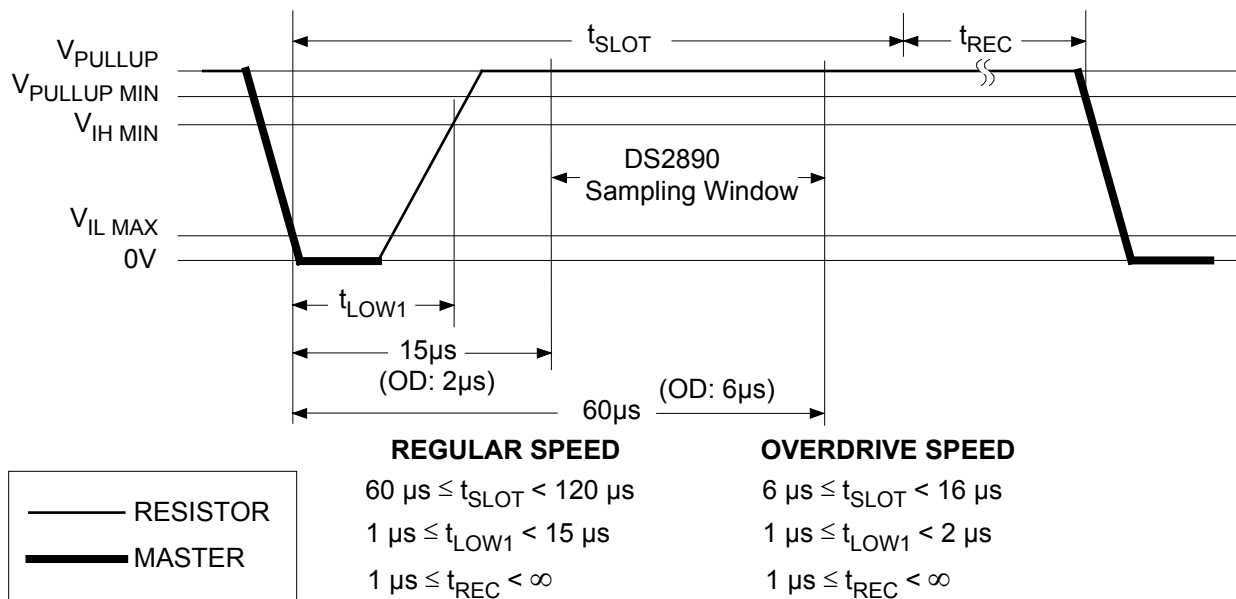


* In order not to mask interrupt signaling by other devices on the 1-Wire bus and to prevent a power-on reset of the parasite powered circuit, $t_{RSTL} + t_R$ should always be less than 960 μs .

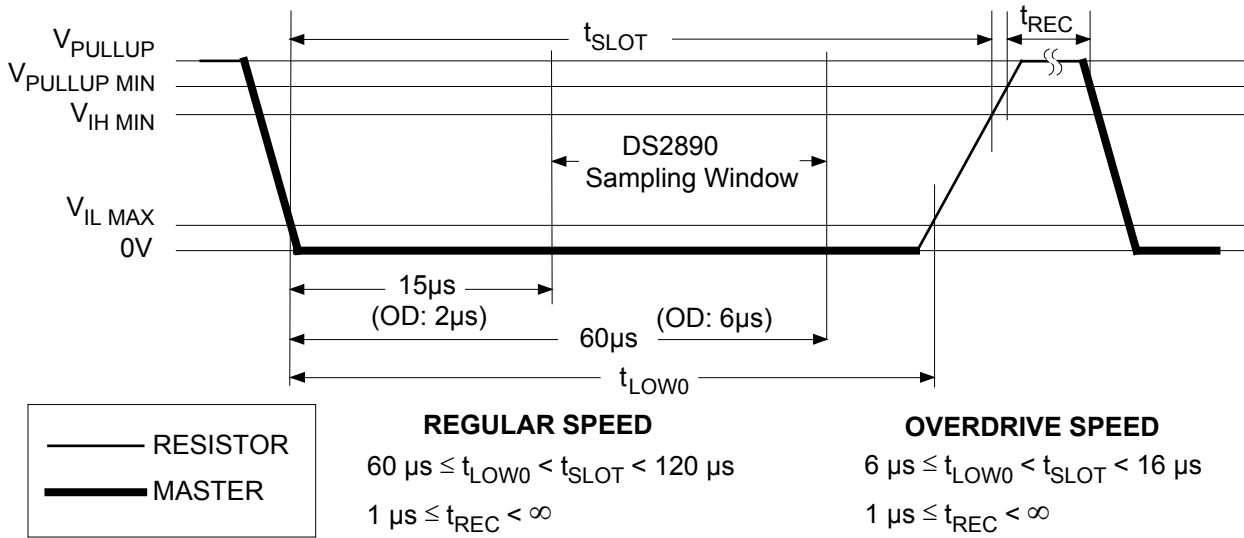
** Includes recovery time.

FIGURE 20. READ/WRITE TIMING DIAGRAMS

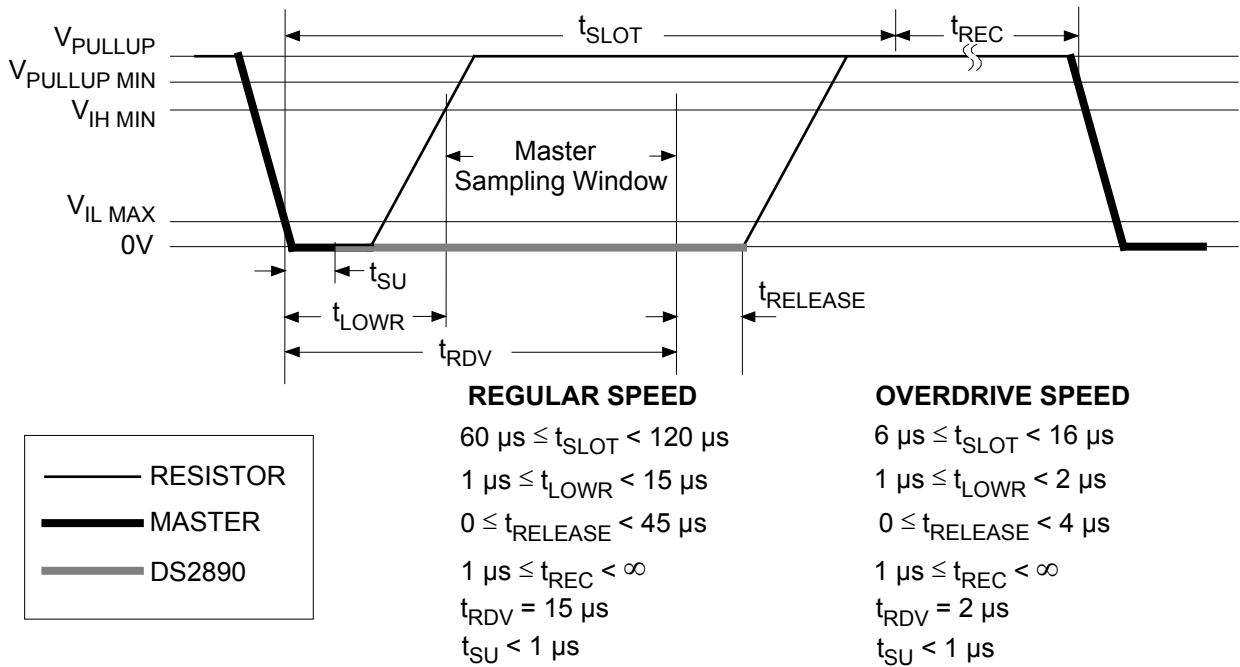
a) Write-one Time Slot



b) Write-zero Time Slot



c) Read-data Time Slot



*The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV} . For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).

FIGURE 21. POTENTIOMETER FUNCTION COMMAND FLOW

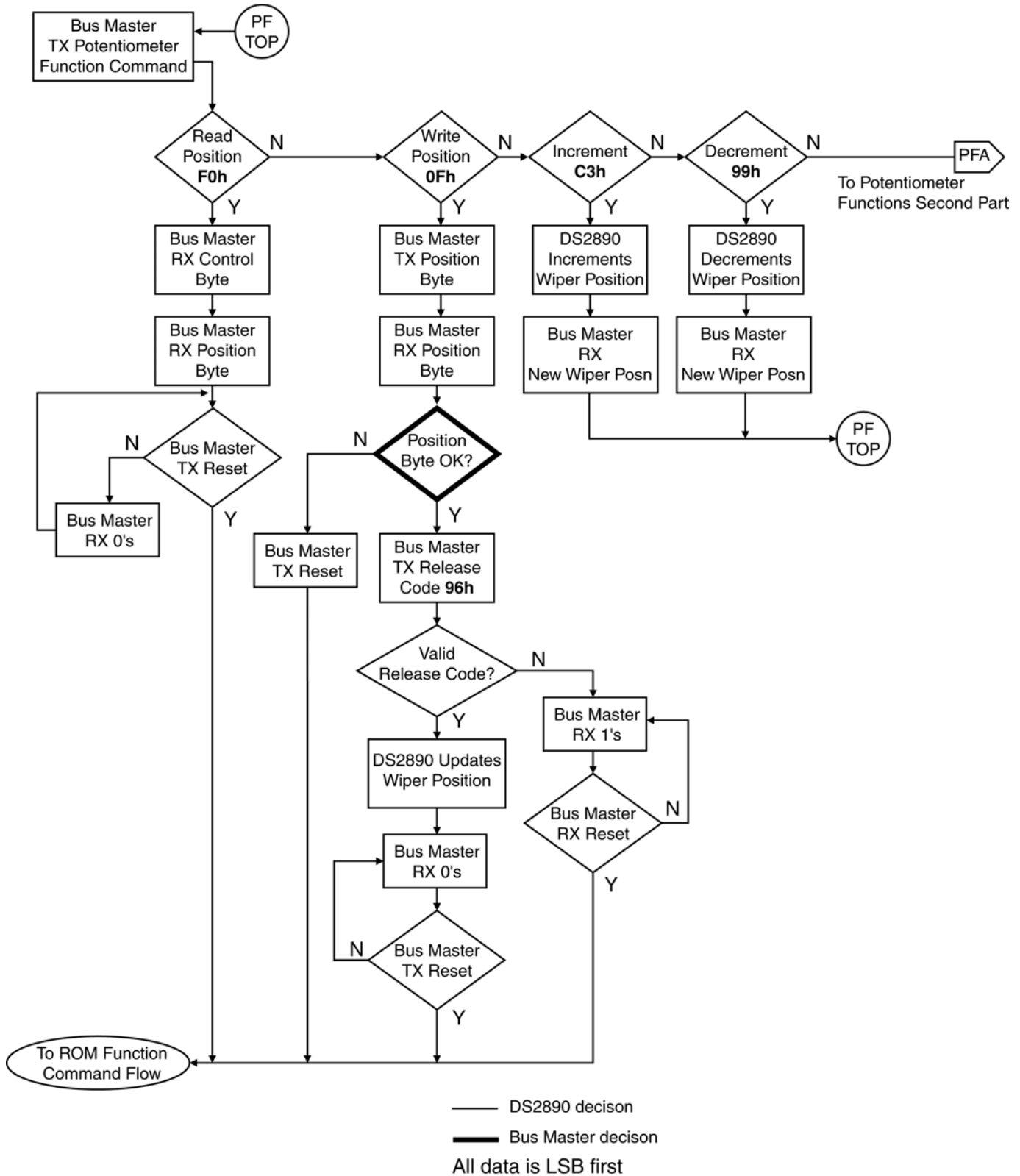


FIGURE 23. ROM FUNCTION COMMAND FLOW

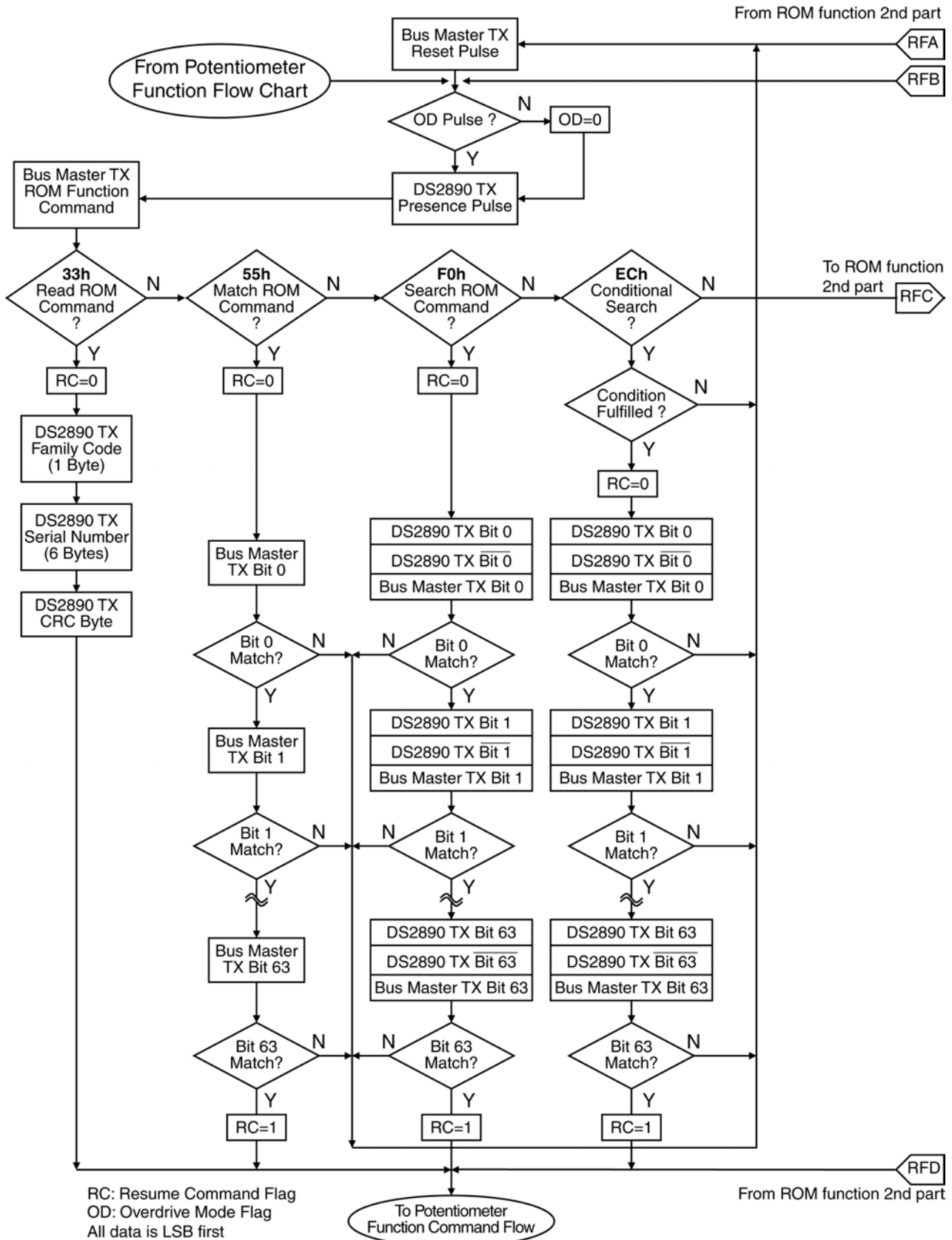
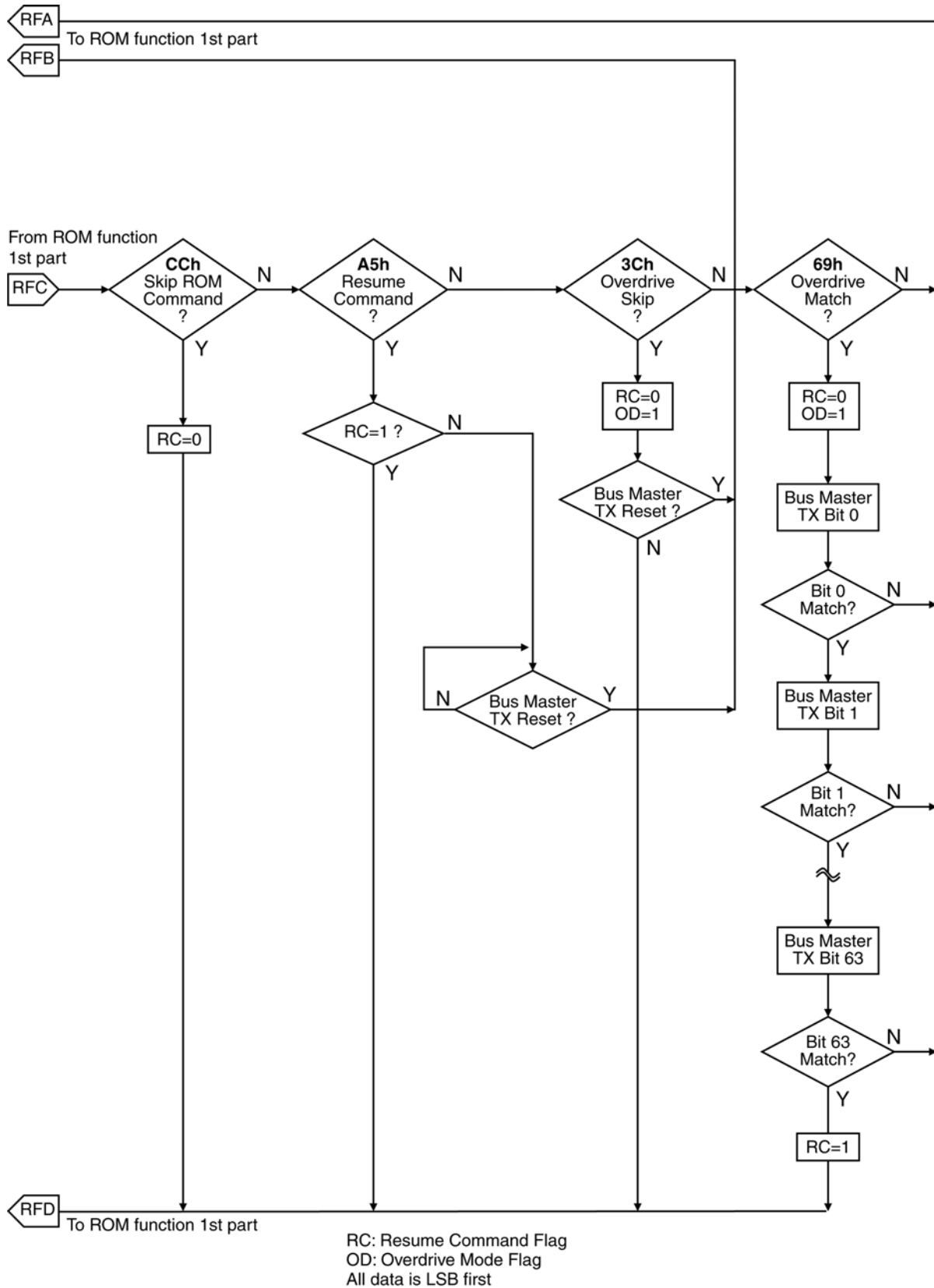


FIGURE 24. ROM FUNCTION COMMAND FLOW (CONTINUED)



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on RH, RL, WIPER Relative to Ground	-0.5V to +11.0V
Voltage on Other Pins Relative to Ground	-0.5V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS -40°C ≤ T_A ≤ +85°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pull-Up Voltage	V _{PUP}	2.8		6.0	V	1
Auxiliary Supply Voltage	V _{DD}	2.8		6.0	V	1,2
		-0.3		0.8	V	1,3

Notes:

1. Voltages are referenced to ground
2. Range applicable when an auxiliary V_{DD} supply is used
3. Range applicable when an auxiliary V_{DD} supply is not used

POTENTIOMETER CHARACTERISTIC

$$2.8V \leq V_{PUP} \leq 6.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Resistor Terminal Voltage		-0.3		11.0	V	1
End-to-End Total Resistance			100		kΩ	
End-to-End Resistance Tolerance		-25		25	%	2
Wiper Resistance:	R _{WIPER}					3
Absolute Linearity			±0.6		LSB	4
Relative Linearity			±0.25		LSB	5
-3 dB cutoff frequency	f _{CUTOFF}	100			kHz	
Temperature Coefficient			800		ppm/°C	

Notes:

1. Voltage is referenced to ground.
2. Valid at 25°C only.
3. Wiper resistance is a function of operating characteristics. See section “POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS” for R_{WIPER} characteristics.
4. Absolute linearity is a measure of wiper output voltage versus expected wiper voltage as determined by wiper position.
5. Relative linearity is a measure of the output deviation between successive potentiometer tap points.

DC ELECTRICAL CHARACTERISTICS

$$2.8V \leq V_{PUP} \leq 6.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Input High	V_{IH}	2.2			V	1
1-Wire Input Low	V_{IL}	-0.3		0.8	V	1,2
1-Wire Output High	V_{OH}		V_{PUP}	6.0	V	1,3
1-Wire Output Low @ 4 mA	V_{OL}			0.4	V	1
1-Wire Input Leakage Current	I_L		5		μA	4
V_{DD} Input Current, Charge Pump OFF	I_{DD}			4.0	μA	5
V_{DD} Input Current, charge Pump ON	I_{DD}			2.0	mA	6

Notes:

1. Voltages are referenced to ground.
2. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.
3. V_{PUP} is the external 1-Wire pull-up voltage.
4. Input load is to ground.
5. Input current when an auxiliary V_{DD} supply is used and the charge pump is turned OFF.
6. Input current when an auxiliary V_{DD} supply is used and the charge pump is turned ON.

AC ELECTRICAL CHARACTERISTICS - REGULAR 1-WIRE SPEED

$$2.8V \leq V_{PUP} \leq 6.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW1}	1		15	μs	
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Low Time	t_{LOWR}	1		15	μs	
Read Data Valid	t_{RDV}		15		μs	1
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	2
Recovery Time	t_{REC}	1			μs	
Reset High Time	t_{RSTH}	480			μs	3
Reset Low Time	t_{RSTL}	480			μs	4
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	

Notes:

1. The optimal sampling point for the master is as close as possible to the end time of the 15 μs t_{RDV} period without exceeding t_{RDV} . For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).
2. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 μs of this falling edge.
3. An additional reset or communication sequence cannot begin until the reset high time (t_{RSTH}) has expired.
4. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 μs , to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

AC ELECTRICAL CHARACTERISTICS - OVERDRIVE 1-WIRE SPEED

$$2.8V \leq V_{PUP} \leq 6.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	μs	
Write 1 Low Time	t_{LOW1}	1		2	μs	
Write 0 Low Time	t_{LOW0}	6		16	μs	
Read Low Time	t_{LOWR}	1		2	μs	
Read Data Valid	t_{RDV}		2		μs	1
Release Time	$t_{RELEASE}$	0	1.5	4	μs	
Read Data Setup	t_{SU}			1	μs	4

AC ELECTRICAL CHARACTERISTICS - OVERDRIVE 1-WIRE SPEED

$$2.8V \leq V_{PUP} \leq 6.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time	t_{REC}	1			μs	
Reset High Time	t_{RSTH}	48			μs	
Reset Low Time	t_{RSTL}	48		80	μs	
Presence Detect High	t_{PDH}	2		6	μs	
Presence Detect Low	t_{PDL}	8		24	μs	

Notes:

1. The optimal sampling point for the master is as close as possible to the end time of the $2 \mu s$ t_{RDV} period without exceeding t_{RDV} . For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).
2. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within $1 \mu s$ of this falling edge.
3. An additional reset or communication sequence cannot begin until the reset high time (t_{RSTH}) has expired.
4. The reset low time (t_{RSTL}) should be restricted to a maximum of $960 \mu s$, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

CAPACITANCE

$$T_A = 25^{\circ}C$$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pin				800	pF	1
V_{DD} Pin			10		pF	
Resistor Terminals				10	pF	

NOTE:

1. Capacitance on the 1-Wire pin could be 800 pF when power is first applied. If a $5 \text{ k}\Omega$ is used to pull up the 1-Wire line to V_{PUP} , the capacitance will not affect communications after a $5 \mu s$ charge time.