

1-Watt Power Amplifier

14.0- 14.5 GHz

Preliminary

V1P.0

MAAPSM0012

MAAPSM0012

Features

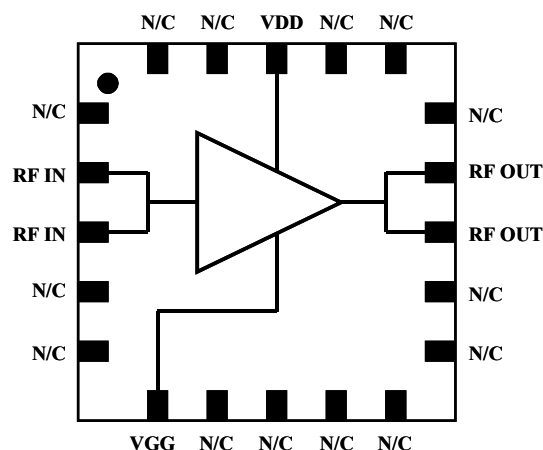
- Heat Sink on Base
- High Saturated Output Power: +30.5 dBm Typical
- 50 Ohm Input / Output Broadband Matched
- 5 mm FQFP-N 20-Lead Package

Description

The MAAPSM0012 is a four stage MMIC power amplifier mounted in a standard outline, 20-pin, 5-mm FQFP-N plastic package, designed ideally for Ku-Band VSAT applications. The MAAPSS0012 has fully matched 50-ohm input and output, eliminating the need for external RF tuning components. This product can be used as either a driver or an output stage amplifier.

M/A-COM fabricates the MAAPSS0012 using a self-aligned MSAG® MESFET process to realize high power efficiency and small size. The process features full passivation for high performance and reliability.

Functional Schematic



Ordering Information

Part Number	Package
MAAPSM0012	5 mm FQFP-N 20 Lead
MAAPSM0012TR	7-inch, 1000-piece reel
MAAPSM0012SMB	Sample Test Board (Includes 5 Samples)

Electrical Specifications: $T_C = 35^\circ\text{C}$, $V_{DD} = 8.0\text{ V}$, $I_{DQ} = 0.350\text{ A}$ (unless otherwise specified)

Parameter	Units	Min.	Typ.	Max.
Frequency	GHz	14.0		14.5
Input VSWR			1.7:1	
Output VSWR			1.4:1	
Linear Gain	dB		25.5	
Gain Flatness	dB		0.7	
Saturated Power, $P_{in} = 9\text{ dBm}$	dBm		30.5	
P_{1dB} , $P_{in} = 4\text{ dBm}$	dBm		29.5	
IP3 (Note 1)	dBm		38	
Drain Current @ P_{SAT}	A		0.550	
Gate Current @ P_{SAT}	mA		3	
Gate Voltage @ I_{DQ}	V		-2.1	
Thermal Resistance	$^\circ\text{C/W}$		19	

1. IP3 is measured with two +19 dBm output tones @ 10 MHz spacing.

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Pin Configuration

PIN No.	PIN Name	Description
1	N/C	No Connect
2	RF IN	RF Input
3	RF IN	RF Input
4	N/C	No Connect
5	N/C	No Connect
6	VGG	Gate Supply
7	N/C	No Connect
8	N/C	No Connect
9	N/C	No Connect
10	N/C	No Connect
11	N/C	No Connect
12	N/C	No Connect
13	RF OUT	RF Output
14	RF OUT	RF Output
15	N/C	No Connect
16	N/C	No Connect
17	N/C	No Connect
18	VDD	Drain Supply
19	N/C	No Connect
20	N/C	No Connect
Base	GND	Package Ground

Handling Procedures

Please observe the following precautions to avoid damage to the MAAPSM0012:

Static Sensitivity

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Use proper ESD precautions when handling these devices.

Absolute Maximum Ratings²

Parameter	Absolute Maximum
DC Drain Supply Voltage	+10 volts
DC Gate Supply Voltage	-3 volts
Case Temperature (See Page 3, Note 8)	-40 °C to +85 °C
Channel Temperature	+150 °C
Storage Temperature	-40 °C to +150 °C
Input Power	15 dBm

2. Exceeding any one or combination of these limits may cause permanent damage.

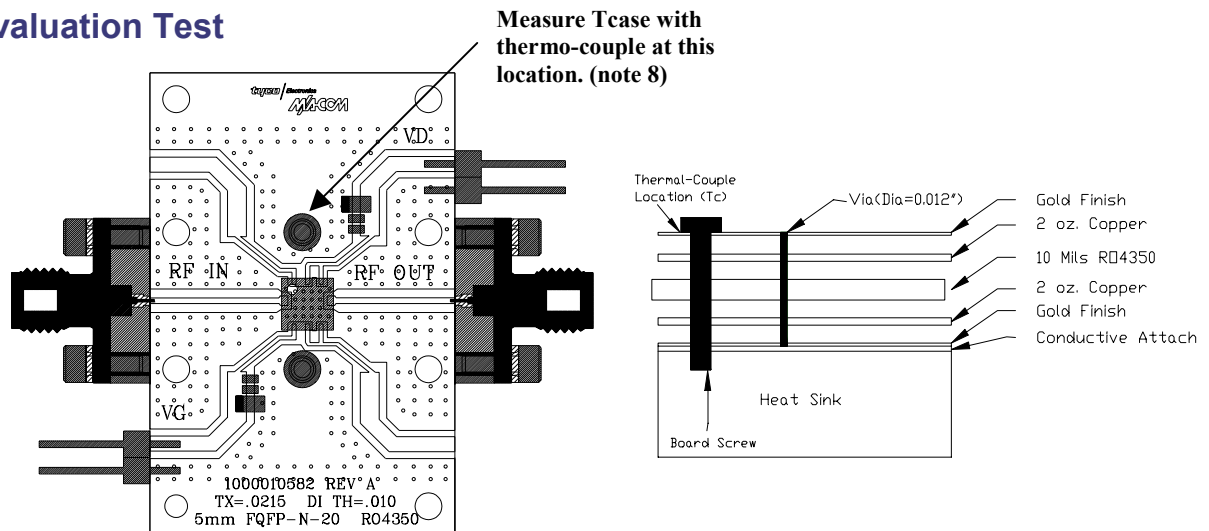
Operating The MAAPSM0012

The MAAPSM0012 is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply -2.5 Volts to V_{GG} .
2. Ramp V_{DD} to +8V.
3. Adjust V_{GG} to set typical drain current (0.350A).
4. Apply RF.
5. Power down sequence in reverse. Turn gate voltage off last.

Application Information

Evaluation Test



Notes on board design:

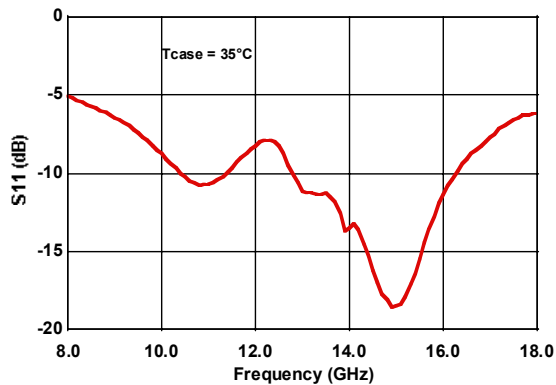
1. A low loss dielectric material such as Rogers 4350, $\epsilon_r = 3.48$, is recommended for this application.
2. A substrate thickness of 10 mils (0.254 mm) maximum is recommended to minimize thermal resistance and ground impedances.
3. RF transmission line impedance must be 50 ohms ($w = 21.5$ mils (0.546 mm) for $t = 10$ mils (0.254 mm), Rogers 4350).
4. The board must provide low thermal resistance from package base to heat sink to accommodate the 3 W typical power dissipation.
5. Metal foil thickness is critical to thermal resistance. The recommended metalization is 2 oz (70 mm minimum thickness).
6. The application board is configured with 16 vias, each 12 mil (0.3048 mm) in diameter beneath the package base. Conductive via fill material is recommended to minimize thermal resistance and to prevent solder from wicking into vias.
7. The exposed package pad must be soldered to the board.
8. Case temperature is measured near the amplifier, on the top circuit board metal, at the location of the board screw.
9. Placement of by-pass capacitors is not critical. The application board is provided with one 10-microfarad Tantalum capacitor, a 0.1- and 0.047- microfarad multi-layer ceramic chip capacitor on each drain/gate bias line.

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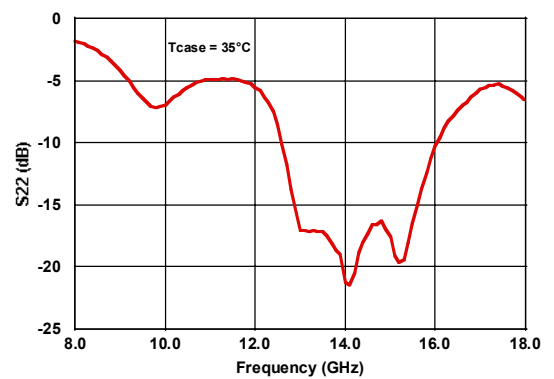
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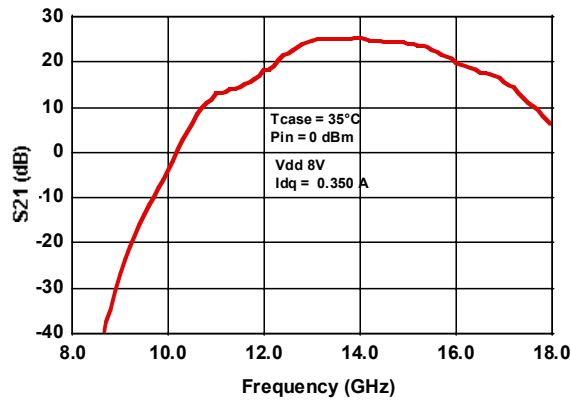
S11 vs. Frequency



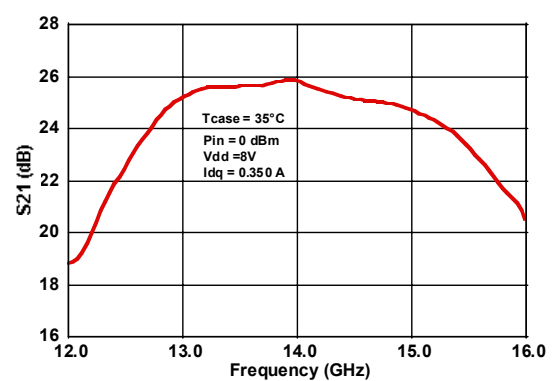
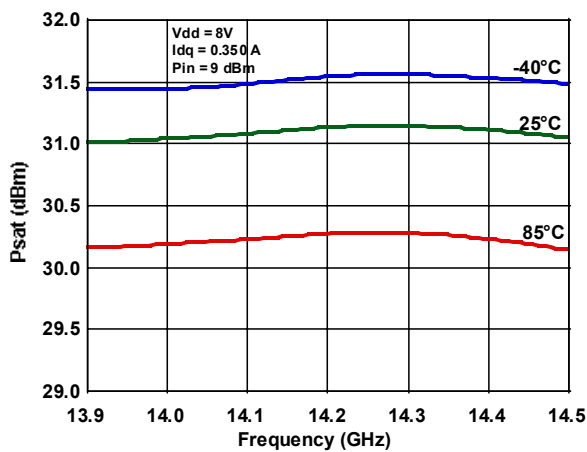
S22 vs. Frequency



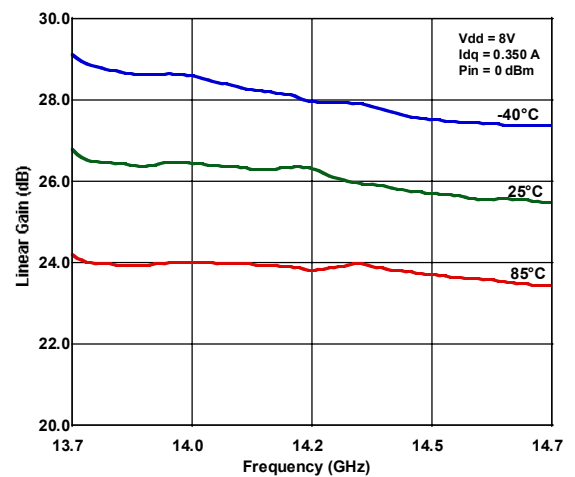
S21 vs. Frequency



S21 vs. Frequency, 12 to 16


P_{SAT} vs. Frequency


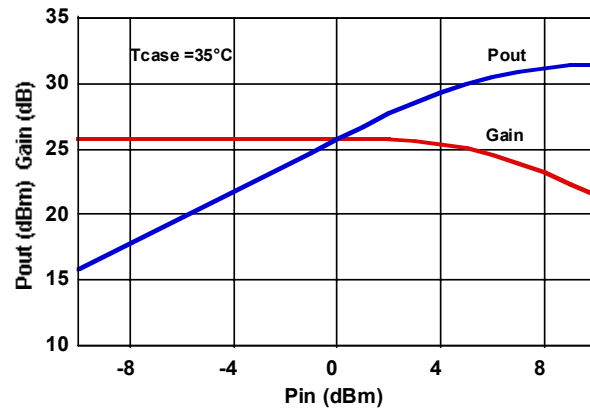
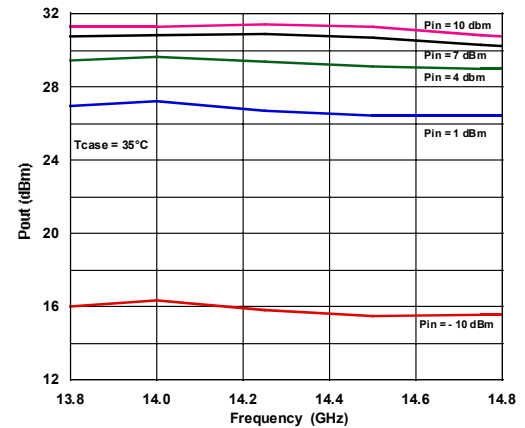
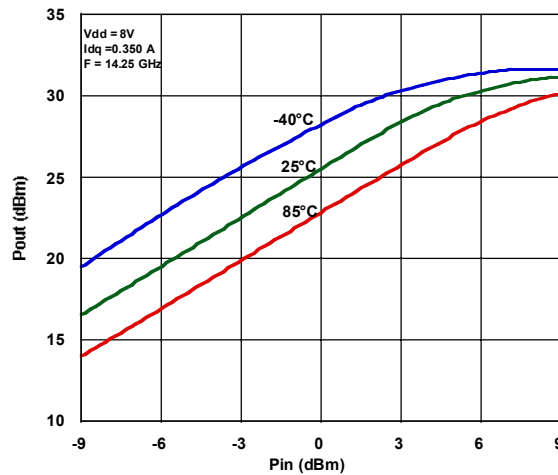
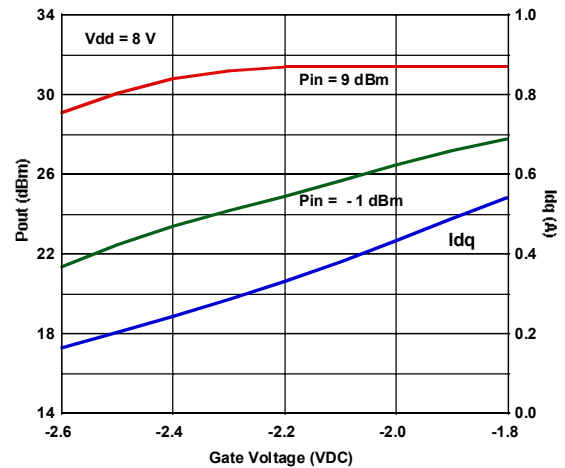
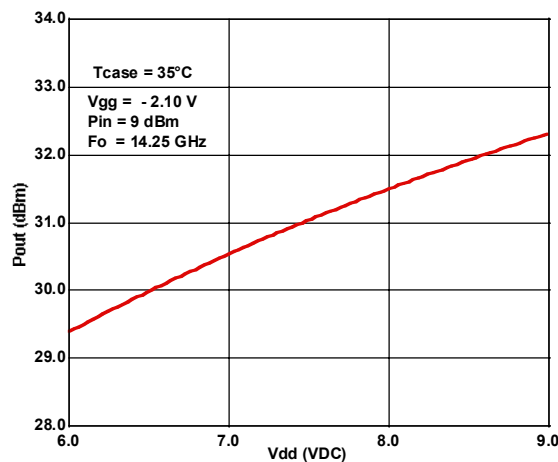
Linear Gain vs. Frequency



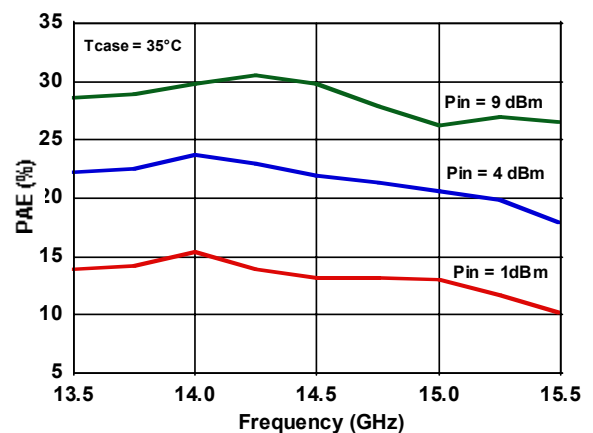
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P_{OUT} , Gain vs. P_{IN} @ 14.25 GHz

 P_{OUT} vs. Frequency vs. P_{IN}

 P_{OUT} vs. P_{IN} vs. Temperature

 P_{OUT} , I_{dQ} vs. V_{gate} @ 14.25 GHz

 P_{OUT} vs. V_{DD}


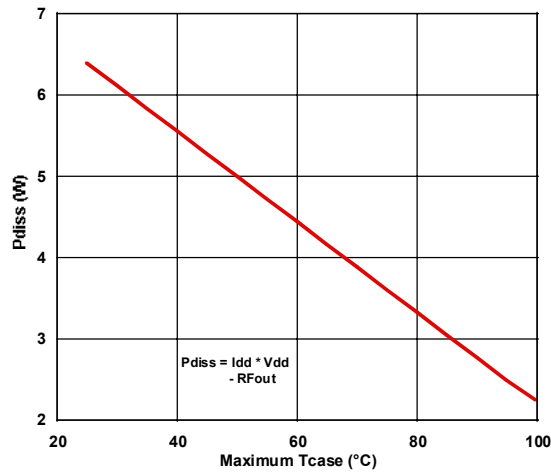
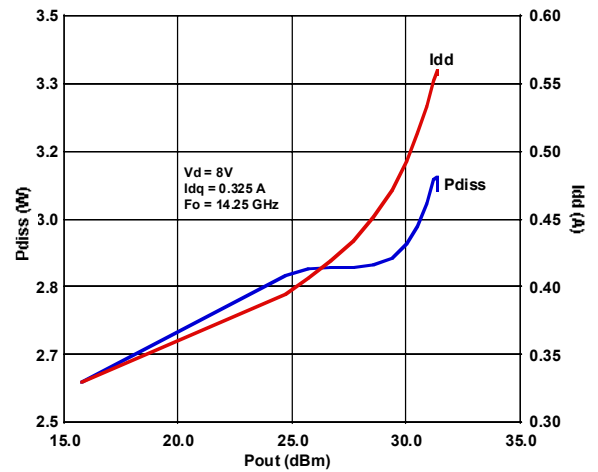
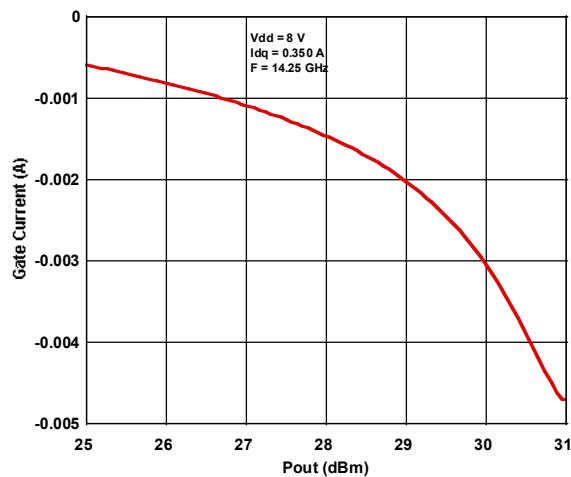
PAE vs. Frequency



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Dissipated Power vs. Max Case Temp.

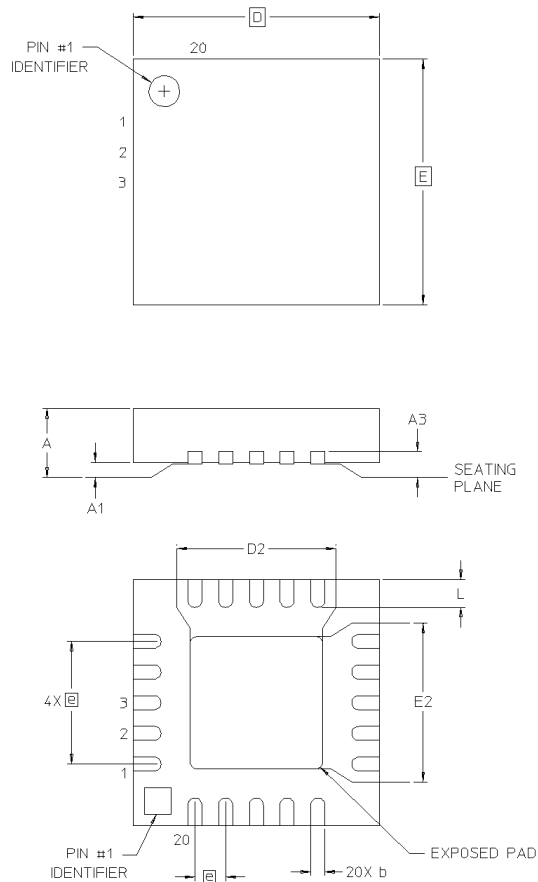
Drain Current & Dissipated Power vs. P_{OUT}Gate Current vs. P_{OUT}

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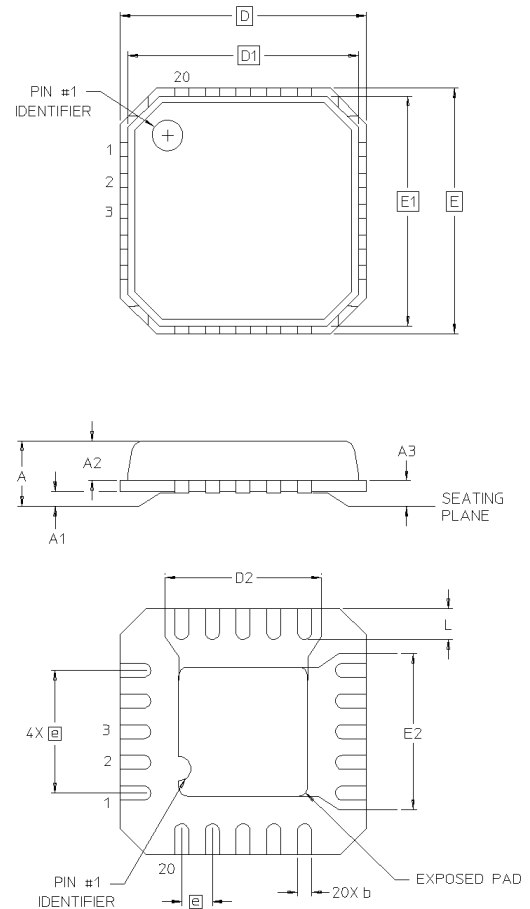
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5 mm FQFP-N 20 Lead Saw Singulated



5 mm FQFP-N 20 Lead Anvil Singulated



DIMENSION SYMBOL	MEASUREMENT (mm)			DIMENSION SYMBOL	MEASUREMENT (mm)		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.80	0.90	1.00	A	0.80	0.90	1.00
A1	0	0.02	0.05	A1	0	0.02	0.05
A3	0.25 REF			A2	0	0.65	1.00
b	0.23	0.30	0.38	A3	0.25 REF		
D		5.00 BSC		b	0.23	0.30	0.38
D2	1.25	2.70	3.25	D		5.00 BSC	
e		0.65 BSC		D1		4.75 BSC	
E		5.00 BSC		D2	1.25	2.70	3.25
E2	1.25	2.70	3.25	e		0.65 BSC	
L	0.35	0.55	0.75	E		5.00 BSC	
				E1		4.75 BSC	
				E2	1.25	2.70	3.25
				L	0.35	0.55	0.75

NOTES: 1. REFERENCE JEDEC MO-220, VAR. VHHC (ISSUE C) FOR ADDITIONAL DIMENSIONAL AND TOLERANCE INFORMATION.
2. REFERENCE S2083 APPLICATION NOTE FOR PCB FOOTPRINT INFORMATION.

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