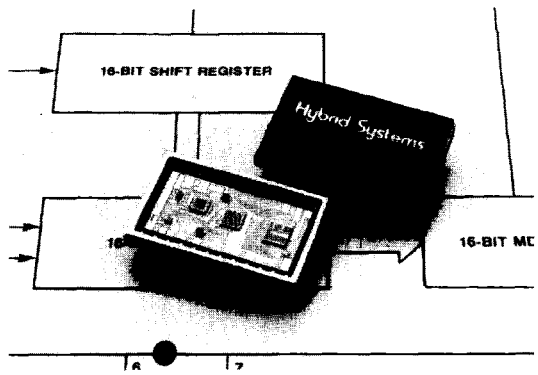
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9372

SERIAL INPUT, 16-BIT DAC

FEATURES

- Serial input
- Monotonic to 16-bits
- Asynchronous clear input
- Low power



DESCRIPTION

The HS9372 is a serial input, 16-bit, current output multiplying D/A converter with 16-bit monotonicity guaranteed over the commercial and military temperature ranges. A proprietary semi-custom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

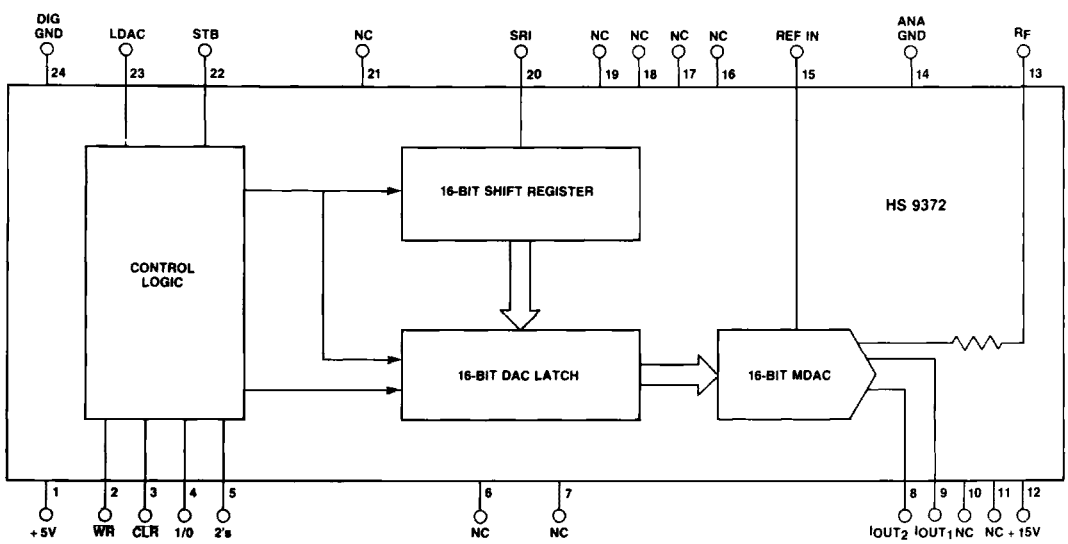
The data is clocked in serially (MSB first) to a shift register and then the 16-bit digital word is loaded into the DAC latch for conversion to analog out. Both unipolar and bipolar operation can be configured; in bipolar mode the input can be either offset binary coding or 2's complement coding.

A CLEAR input is provided for the asynchronous setting of the DAC latch to either all "0's" or "1" (MSB) and all "0's" depending on the user's choice.

The HS9372 is available for either commercial (0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883 Rev. C, Levels B or S is available.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

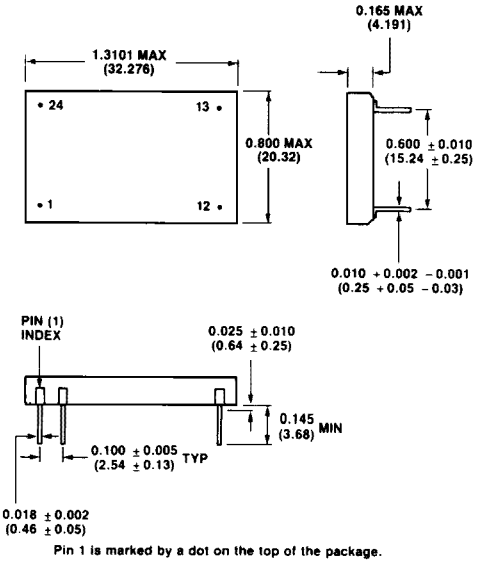
(Typical @ +25°C unless otherwise specified)

MODEL	HS 9372K	HS 9372J	HS 9372TB	HS 9372SB
DIGITAL INPUT				
Resolution	16-bits, Serial MSB first	*	*	*
Coding	Straight/Offset Binary/ 2's Complement[1]	*	*	*
Logic Compatibility	TTL, LSTTL, CMOS			
V_{IL} (max)[2]	0.8V	*	*	*
V_{IH} (min)[2]	2.4V	*	*	*
Input Current	10 μA max	*	*	*
SWITCHING CHARACTERISTICS[3]				
t_{WR} ($\overline{WR}$ pulse width)	120 nsec min	*	*	*
t_{AW} (STB and LDAC valid to end of $\overline{WR}$)	120 nsec min	*	*	*
t_{DW} (DATA valid to end of $\overline{WR}$)	120 nsec min	*	*	*
t_{DH} (DATA hold time)	0 nsec min	*	*	*
t_{AH} (STB and LDAC hold time)	0 nsec min	*	*	*
t_{WCL} ($\overline{CLR}$ pulse width)	200 nsec min	*	*	*
ANALOG OUTPUT				
Gain Accuracy	±0.1% F.S.R. typ, ±0.2% max[4]	*	*	*
Initial Offset Error	50 μV max[4,5]	*	*	*
Current Range				
Unipolar	0 to +2 mA	*	*	*
Bipolar	±1 mA	*	*	*
Noise p-p noise (0.1 Hz to 100 Hz)	50 μV p-p	*	*	*
Output Capacitance	80 pF	*	*	*
REFERENCE INPUT				
Input Impedance	5KΩ	*	*	*
STATIC PERFORMANCE				
Integral Linearity Error[6]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Differential Linearity Error	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Monotonicity Guaranteed to: (over temperature)	16-bits	15-bits	16-bits	15-bits
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.0015% F.S.R.	1 μsec[7]	*	*	*
Full Scale Transition Settling to 0.0015% F.S.R.	5 μsec[7]	*	*	*
Reference Feedthrough Attenuation[8]	100 dB @ 100 Hz sine wave	*	*	*
	80 dB @ 1 kHz sine wave	*	*	*
Glitch Energy[8]	3 nV-sec	*	*	*
STABILITY				
Gain Drift	8 ppm/°C max	*	*	*
Offset Drift				
Unipolar	1 ppm/°C max	*	*	*
Bipolar	2 ppm/°C max	*	*	*
Linearity Drift	1 ppm/°C max	*	*	*
POWER SUPPLY				
Current				
+15V	1 mA max	*	*	*
+5V				
Static Consumption	50 μA max	*	*	*
Dynamic Consumption[9]	7 mA max	*	*	*
Power Dissipation				
Static	15.25 mW max	*	*	*
Dynamic	50 mW max	*	*	*
PSRR	±0.0006% FS/% typ ±0.002% FS/% max			
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	*
Storage	−25°C to +85°C	*	−65°C to +150°C	*
PACKAGE				
24-pin, double DIP				

NOTES:

1. The coding is determined by the logic level on the 2's pin (see further).
2. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
3. −55°C to +125°C.
4. Adjustable to zero.
5. Using the internal R_F with nulled external amplifier in a constant 25°C ambient.
6. Integral Linearity is measured per best straight line method.
7. 50 Ω load.
8. Lid of Case B units should be grounded to analog ground for optimum performance.
9. Conditions: $\overline{WR}$ =

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	24	DIGITAL GND
2	$\overline{WR}$	23	LDAC
3	$\overline{CLR}$	22	STB
4	1/0	21	NC
5	2's	20	SRI
6	NC	19	NC
7	NC	18	NC
8	I OUT 2	17	NC
9	I OUT 1	16	NC
10	NC	15	REF IN
11	NC	14	ANALOG GND
12	+15V	13	RF

NC — No internal connection.

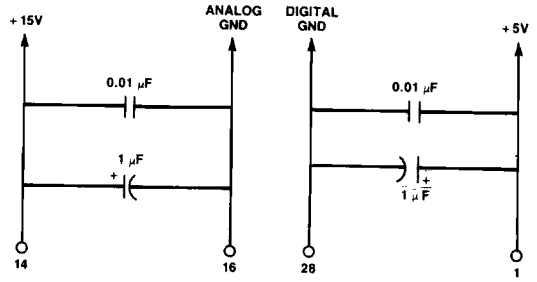
ABSOLUTE MAXIMUM RATINGS (HS 9372)

+15V Supply (+V_{DD}) to Analog GND . . . +17V
+5V Supply (−V_{CC}) to Digital GND . . . . +7V
Analog GND to Digital GND . . . . . ±0.5V
Digital Input Voltage to Digital GND . . . . . +V_{CC} + 0.3V max
Digital GND −0.3V min
$V_{REF\ IN}$ to Analog GND . . . . . ±25V
Output Voltage (Pins 8,9) . . . . . Analog GND ±0.1V
Power Dissipation of Package
(Case A) . . . . . 1.4W @ +85°C
(Case B) . . . . . 1.5W @ +125°C
Lead Temperature, Soldering
(Case A) . . . . . 300°C, 5 sec
(Case B) . . . . . 300°C, 10 sec

7

APPLICATION INFORMATION

RECOMMENDED BYPASS CIRCUIT



THEORY OF OPERATION

If the HS 9372 is to operate in unipolar mode or in bipolar mode with OFFSET BINARY coding, the 2's pin must be connected to 0 Volts. In bipolar mode with 2's COMPLEMENT coding, the 2's pin must be tied to +5 Volts.

The STB and LDAC pins address the shift register and the DAC latch respectively. When the shift register is addressed (LDAC = "0", STB = "1"), serial data appearing at the SRI pin will be clocked in on the falling edge of $\overline{WR}$. When the shift register is full, the DAC latch is addressed (STB = "0", LDAC = "1") and data will be transferred in by bringing $\overline{WR}$ momentarily low.

Using 1/0 pin in conjunction with the $\overline{CLR}$ pin, the DAC output can be set asynchronously to 0 Volts in both unipolar and bipolar mode (offset binary or 2's complement code). This occurs by bringing $\overline{CLR}$ low. Table 1 indicates how to connect 1/0 pin in the different cases.

MODE	CODING	1/0 PIN
Unipolar	Straight Binary (2's = "0")	"0"
Bipolar	Offset Binary (2's = "0")	"1"
Bipolar	2's Complement (2's = "1")	"0"

Table 1

This feature allows an easy system initialization and simplifies the DAC calibration (see "Unipolar Operation" and "Bipolar Operation" paragraphs).

Table 2 is a truth table for the logic control inputs.

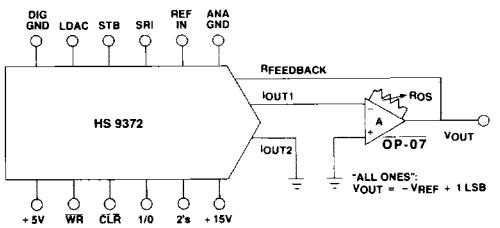
CONTROL INPUTS				OPERATION
$\overline{CLR}$	$\overline{WR}$	STB	LDAC	
0	X	X	X	Clear DAC latch to 00...00 if 1/0 is Dig Gnd 10...00 if 1/0 is +5V (asynchronous operation)
1	1	X	X	Device not selected, output
1	X	0	0	reflects previously loaded data
1	⌐↓	1	0	Strobe data into the shift register
1	⌐‾	0	1	Load data into the DAC latch[2]
1	⌐‾	1	1	Invalid address

Table 2. Truth Table — Control Inputs

NOTES:

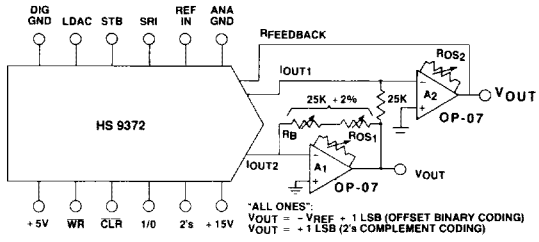
1. ⌐↓ = edge sensitive (falling edge)
   ⌐‾ = level sensitive (low)
2. If 2's = "1", data is loaded in 2's complement coding for the bipolar mode. If 2's = "0", data is loaded in offset binary coding for the bipolar mode and in direct binary coding for the unipolar mode.

UNIPOLAR OPERATION *(2's = "0")*



NOTE: To maintain specified HS 9372 linearity, the external amplifier (A) must be zeroed. This operation is easily performed without having to serially load an "all 0's" code: set $\overline{CLR}$ and 1/0 to logic level "0" and adjust R_{OS} for $V_{OUT} = 0 \pm 1$ mV.

BIPOLAR OPERATION *(4-Quadrant Multiplication)*



NOTE: To maintain specified HS 9372 linearity, external amplifiers (A_1 and A_2) must be zeroed. For offset binary coding (2's = "0"), set $\overline{CLR}$ = "0" and 1/0 = "1" and then follow steps A & B below. For two's complement coding (2's = "1"), set $\overline{CLR}$ and 1/0 = "0" and then follow steps A & B below.

a) With REF IN = 0, set R_{OS1} for $V_{01} = 0 \pm 1$ mV and R_{OS2} for $V_{OUT} = 0 \pm 1$ mV.

b) Set REF IN to +10V and adjust R_B for V_{OUT} to be 0 volts.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. − 1 LSB
1 0 0...0 0 0	+F.S./2
0 1 1...1 1 1	+F.S./2 − 1 LSB
0 0 0...0 0 0	0V

BIPOLAR OPERATION

OFFSET BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. − 1 LSB
1 0 0...0 0 0	0V
0 1 1...1 1 1	− 1 LSB
0 0 0...0 0 0	−F.S.

BIPOLAR OPERATION

2's COMPLEMENT INPUT	ANALOG OUTPUT
0 1 1...1 1 1	+F.S. − 1 LSB
0 0 0...0 0 0	0V
1 1 1...1 1 1	− 1 LSB
1 0 0...0 0 0	−FS

TIMING INFORMATION

Figure 1 is the timing diagram for loading the shift register. Figure 2 is the timing diagram for loading the DAC latch. Figure 3 is a global timing diagram for the complete operation of the HS 9372.

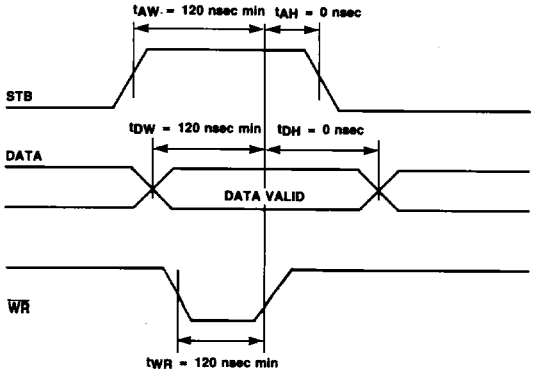


Figure 1. Loading the Shift Register (LDAC = "0") through the SRI Pin. Write Cycle #1 to 16.

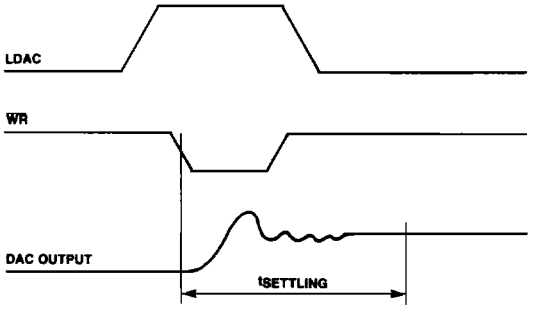


Figure 2. Loading the DAC Latch (STB = "0") from the Shift Register. Write Cycle #17.

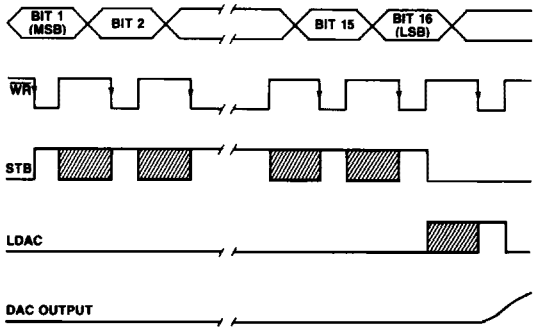


Figure 3. Global Timing for Complete Operation of the HS 9372.

MICROPROCESSOR INTERFACE

The timing information described earlier is fully compatible with the timing of several microprocessors (Intel, Zilog, etc.) without the addition of any external components. Figure 4 is a general example of interfacing the HS 9372 to an 8-bit μP. It is followed by a routine example.

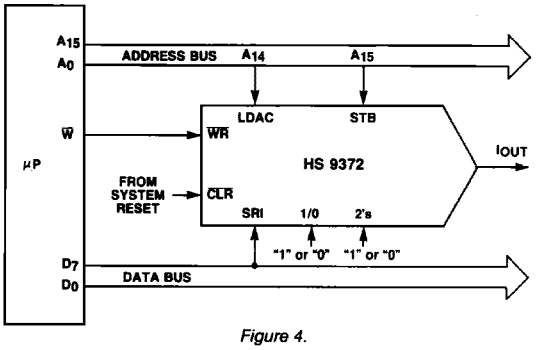


Figure 4.

ROUTINE SOFTWARE PROGRAM

Assumptions:

1. The first byte of data is at memory address 0000.
2. The second byte of data is a memory address 0001.
3. A = accumulator of the μP.
4. B = general register of the μP.
5. 4000 is the address of the DAC latch ($A_{14} = 1$; $A_{15} = 0$)
6. 8000 is the address of the shift register ($A_{14} = 0$; $A_{15} = 1$)

```
      LOAD the value 8 in register B.
      LOAD in the accumulator A of the μP the
      content of memory address 0000.
      JUMP to SHIFT (SHIFT is the subroutine which
      allows the loading of data in the input register).
      LOAD the value 8 in register B.
      LOAD in A the second byte of data which is at
      memory address 0001.
      JUMP to SHIFT.
      WRITE at the address 4000 (a memory write in
      struction at the address 4000 loads the data in
      the DAC latch).
      END.

SHIFT WRITE at the address 8000 (a memory write
      instruction at the address 8000 loads the data
      bit by bit in the shift register).
      ROTATE LEFT the content of A.
      DECREMENT B.
      If B ≠ 0, GOTO SHIFT.
      RETURN from subroutine.
```

7

POWER SUPPLY CONSIDERATIONS

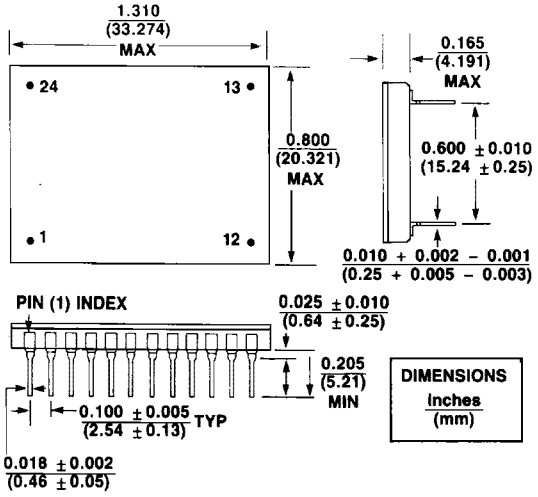
Power supplies used for the HS 9372 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 0.03 μA is 1 LSB for a 2 mA output. This translates to 156 μV for a 10 volt output range when converting to voltage.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

LAYOUT CONSIDERATIONS

Due to the small bit weight (0.03 μA for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 14 of the HS 9372. All digital lines should run on the soldering side of the PC-board.

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package.



LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 μV for the first 1000 hrs; and 100 μV per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE	SCREENING
HS 9372K	16 bits min	0°C to +70°C	—
HS 9372J	15 bits min	0°C to +70°C	—
HS 9372TB	16 bits min	−55°C to +125°C	MIL-STD-883C
HS 9372SB	15 bits min	−55°C to +125°C	MIL-STD-883C