

PRELIMINARY

MB81416-10/MB81416-12/MB81416-15

Note: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CAPACITANCE ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 - A_7$,	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}, \overline{CAS}, \overline{W}, \overline{G}$	C_{IN2}	—	8	pF
Output Capacitance $DQ_1 - DQ_4$	C_D	—	7	pF

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature 0°C to +70°C
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	-2.0	—	0.8	V	
Input Low Voltage, DQ	V_{ILD}^*	-1.0	—	0.8	V	

*The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}, \overline{CAS}$ cycling; $t_{RC} = \text{min}$)	I_{CC1}		55	mA
			50	
			45	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}		4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}, \overline{RAS}$ cycling; $t_{RC} = \text{min}$)	I_{CC3}		38	mA
			35	
			32	
PAGE MODE CURRENT Average power supply current ($\overline{RAS} = V_{IL}, \overline{CAS}$ cycling; $t_{PC} = \text{min}$)	I_{CC4}		38	mA
			35	
			32	
REFRESH CURRENT 2* Average power supply current (\overline{RAS} cycling, \overline{CAS} before \overline{RAS})	I_{CC5}		42	mA
			38	
			35	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V, V_{CC} = 5.5V, V_{SS} = 0V$, all other pins not under test = 0V)	I_{IL}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
OUTPUT LEVELS Output high voltage ($I_{OH} = -5\text{mA}$) Output low voltage ($I_{OL} = 4.2\text{mA}$)	V_{OH}	2.4	0.4	V
	V_{OL}			

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
 I_{CC} is dependent on input low voltage level $V_{ILD}, V_{ILD} > -0.5V$.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

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Parameter	Notes	Symbol		MB81416-10		MB81416-12		MB81416-15		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		t _{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t _{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t _{RWC}	TRELREL	290	—	330	—	375	—	ns
Access Time from $\overline{\text{RAS}}$	(4), (6)	t _{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{\text{CAS}}$	(5), (6)	t _{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t _{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t _T	TT	3	50	3	50	3	50	ns
RAS Precharge Time		t _{RP}	TREHREL	90	—	100	—	100	—	ns
RAS Pulse Width		t _{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
RAS Hold Time		t _{RSH}	TCELREH	50	—	60	—	75	—	ns
CAS Precharge Time (Page Mode only)		t _{CP}	TCEHCEL	45	—	50	—	60	—	ns
CAS Precharge Time (All cycles except page mode)		t _{CPN}	TCEHCEL	40	—	45	—	55	—	ns
CAS Pulse Width		t _{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
CAS Hold Time		t _{CSH}	TRELCEH	100	—	120	—	150	—	ns
RAS to CAS Delay Time	(4), (7)	t _{RCD}	TRELCEL	20	50	20	60	25	75	ns
CAS to RAS Set Up Time		t _{CRS}	TCEHREL	20	—	25	—	30	—	ns
Row Address Set Up Time		t _{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t _{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t _{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t _{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t _{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to RAS	(9)	t _{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to CAS	(9)	t _{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t _{WCS}	TWLCEL	-5	—	-5	—	-5	—	ns
Write Command Hold Time		t _{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t _{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to RAS Lead Time		t _{RWL}	TWLREH	45	—	50	—	60	—	ns
Write Command to CAS Lead Time		t _{CWL}	TWLCEH	45	—	50	—	60	—	ns
Data In Set Up Time		t _{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t _{DH}	TCELDX	20	—	25	—	30	—	ns
CAS to W Delay	(8)	t _{CWD}	TCELWL	85	—	100	—	120	—	ns
RAS to W Delay	(8)	t _{RWD}	TRELWL	135	—	160	—	195	—	ns
Access Time from $\overline{\text{G}}$		t _{QEA}	TGLQV	—	25	—	30	—	40	ns
$\overline{\text{G}}$ to Data in Delay Time		t _{QED}	TGHQV	30	—	35	—	40	—	ns
$\overline{\text{G}}$ Hold Time Referenced to $\overline{\text{W}}$		t _{QEH}	TWLGL	0	—	0	—	0	—	ns
Output Buffer Turn Off Delay from $\overline{\text{G}}$		t _{QEZ}	TGHQZ	0	30	0	35	0	40	ns
Page Mode Cycle Time		t _{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t _{PRWC}	TCEHCEH	180	—	205	—	240	—	ns
CAS Set Up Time Referenced to RAS (CAS before RAS Refresh)		t _{FCS}	TCELREL	20	—	25	—	30	—	ns
CAS Hold Time Referenced to RAS (CAS before RAS Refresh)		t _{FCH}	TRELCEH	20	—	25	—	30	—	ns
RAS Precharge to CAS Active Time		t _{RPC}	TREHCEL	20	—	20	—	20	—	ns
Refresh Counter Test RAS Pulse Width (10)		t _{TRAS}	TRELREH	280	—	325	—	390	—	ns
Refresh Counter Test Cycle Time (10)		t _{RTC}	TRELREL	380	—	435	—	500	—	ns
$\overline{\text{G}}$ to RAS Inactive Setup Time		t _{OES}	TGLREH	0	—	0	—	0	—	ns
Data in to CAS Delay Time (11)		t _{DZC}	TDXCEL	0	—	0	—	0	—	ns
Data in to $\overline{\text{G}}$ Delay Time (11)		t _{DZO}	TDXGL	0	—	0	—	0	—	ns
CAS Precharge Time (CAS before RAS cycle)		t _{CPR}	TCEHCEL	25	—	30	—	30	—	ns

Notes: See notes on next page

* These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor Memory.

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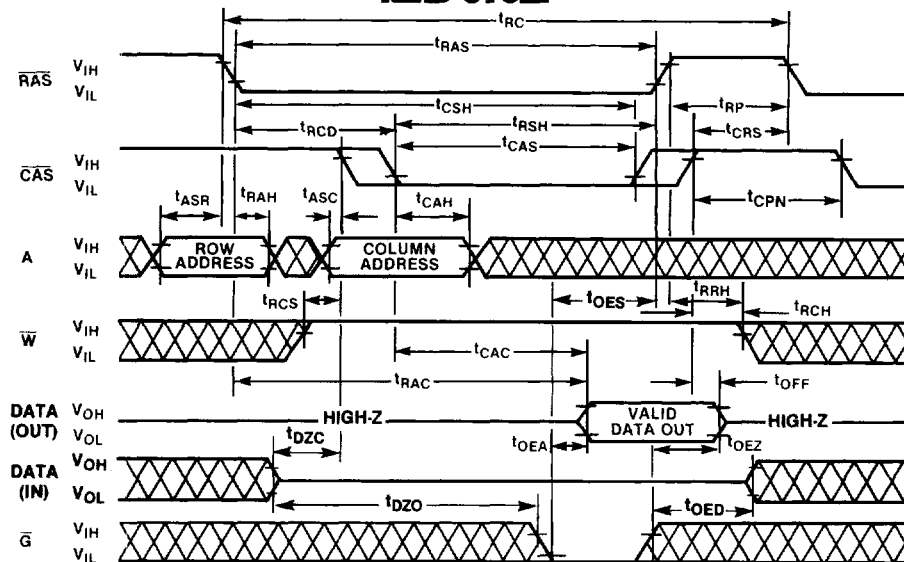
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Notes:

1. An initial pause of 200 μ s is required after power up, followed by any 8 RAS cycles, before proper operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
2. AC measurements assume $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

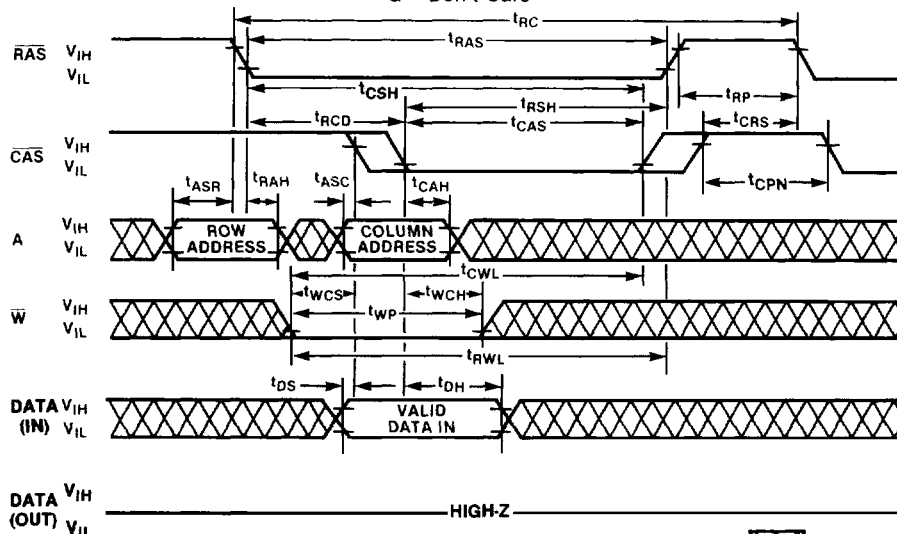
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.); $t_T = 5$ ns.
8. t_{WCS} , t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.
11. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

READ CYCLE



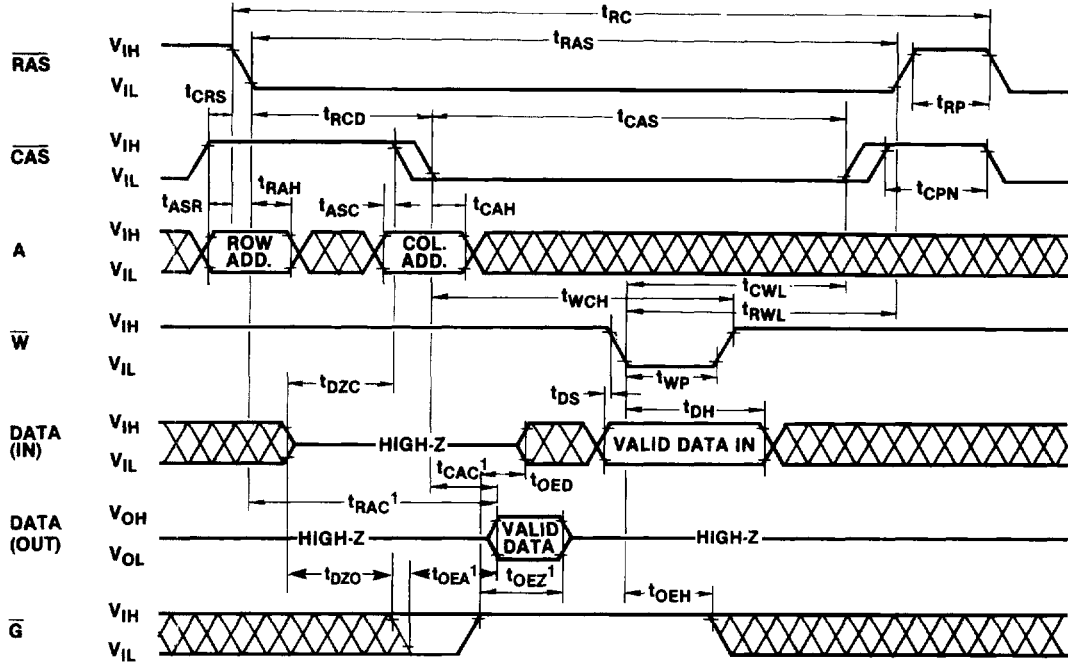
WRITE CYCLE (Early Write)

\bar{G} = Don't Care



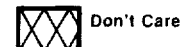
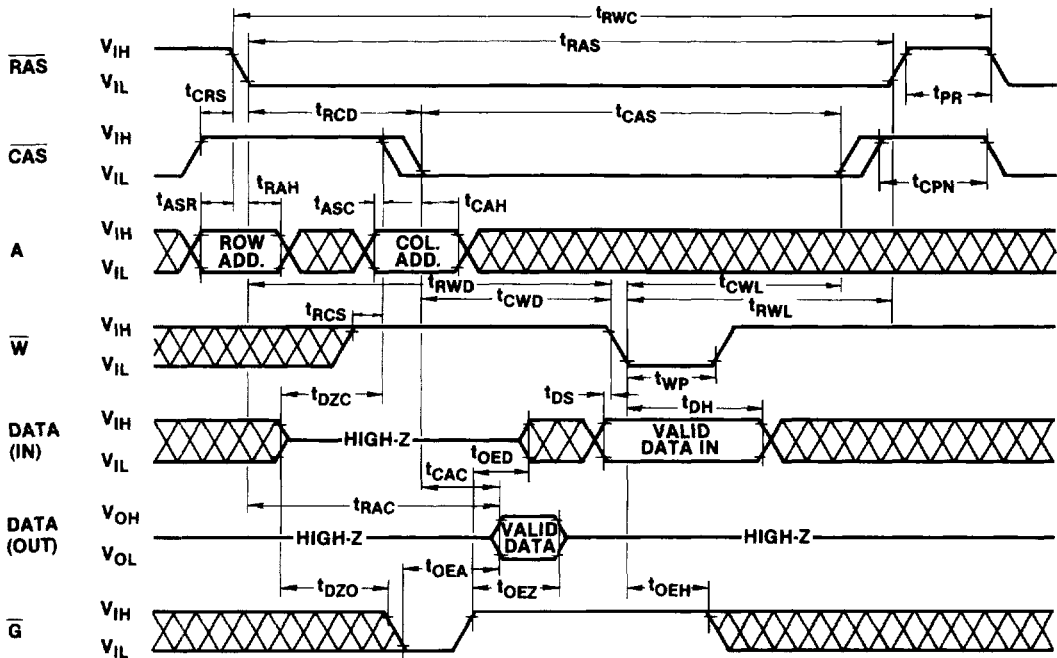
 Don't Care

WRITE CYCLE
(Output Enable Controlled)

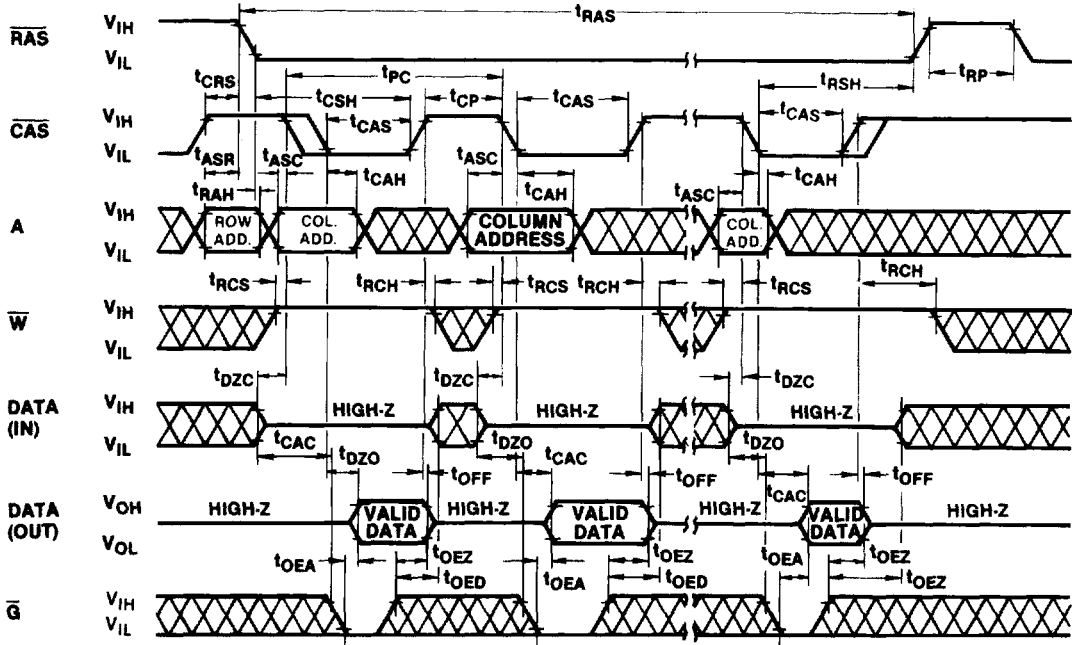


Note 1: When t_{CWD} is satisfied and \bar{G} is low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

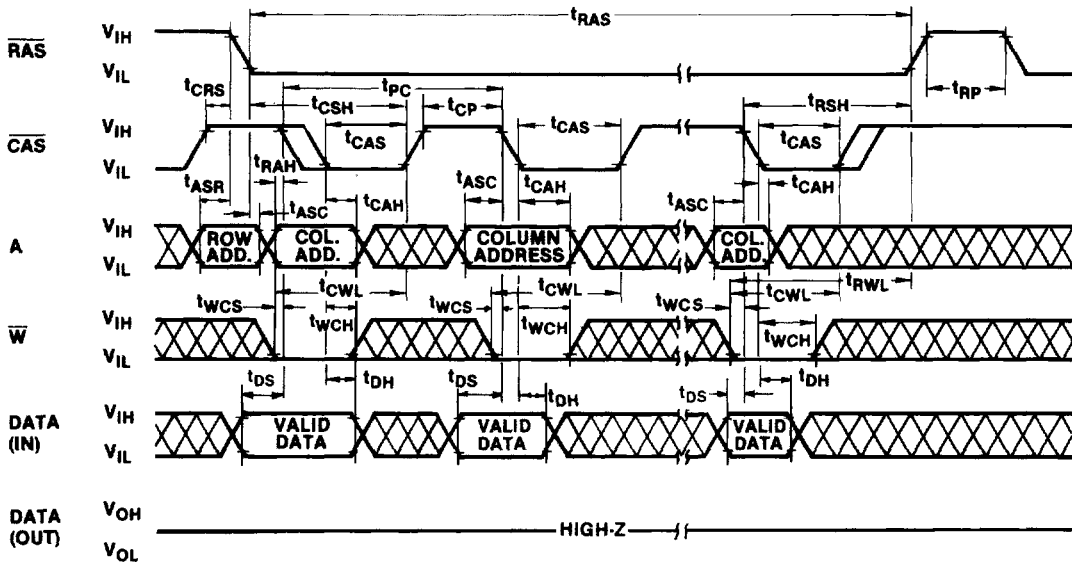
READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE



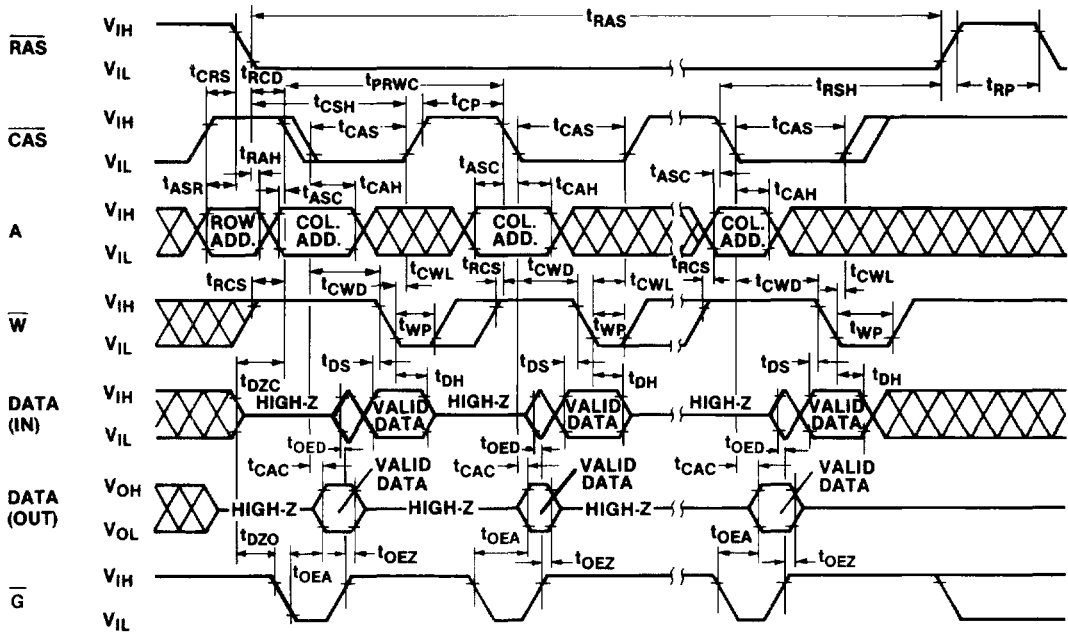
PAGE MODE WRITE CYCLE
(G = Don't Care)



 Don't Care

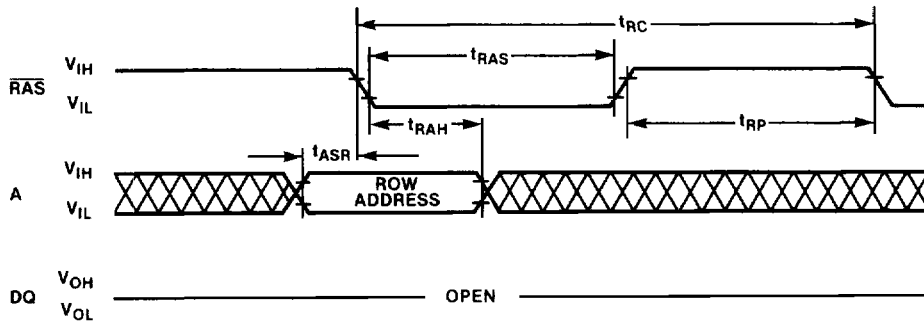
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PAGE MODE READ-WRITE CYCLE



$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

NOTE: $\overline{\text{CAS}} = V_{IH}$; A₇, $\overline{\text{W}}$, $\overline{\text{G}}$, = Don't Care



 Don't Care

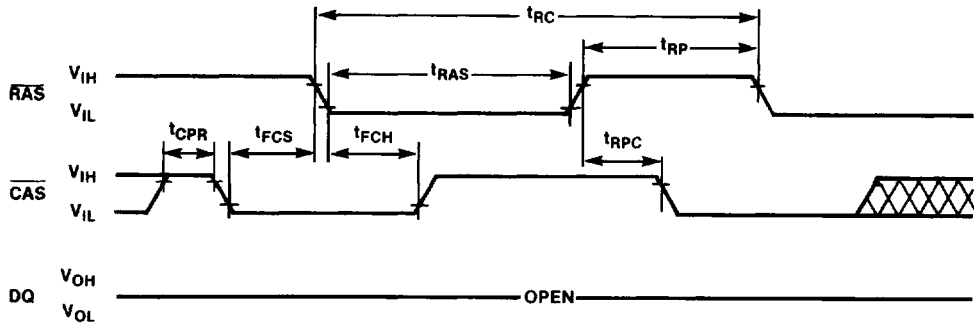
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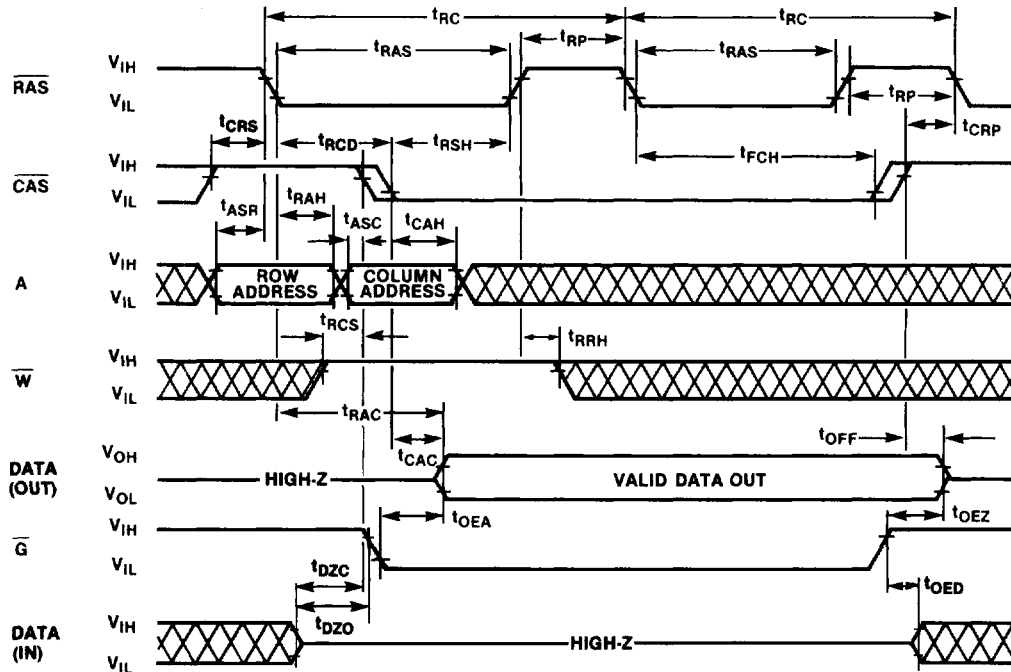
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CAS-BEFORE-RAS REFRESH CYCLE

NOTE: A, \bar{W} , \bar{G} = Don't Care



HIDDEN REFRESH CYCLE



 Don't Care

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DESCRIPTION

Address Inputs

A total of 14 binary input address bits are needed to decode any one of 16,384 nibble wide words from the MB81416's 65,536 memory cells. Addressing a Random 4-bit word is initiated by establishing 8 row address bits on the address input pins, (A_0 through A_7), and after they are stable, latching these address bits with the falling edge of the Row Address Strobe (\overline{RAS}). Then 6 column address bits are established on the address input pins A_1 through A_6 . After the addresses are stable, they are latched with the falling edge of the Column Address Strobe (\overline{CAS}). Address timing is made non-critical by the MB81416's "gated \overline{CAS} " circuitry which automatically inhibits \overline{CAS} until the Row Address Hold time (t_{RAH}) has been satisfied and the address inputs have changed from row to column addresses.

Data Input/Output

The MB81416 has 4 common I/O pins (DQ_1 , DQ_2 , DQ_3 , and DQ_4). Read or write modes are selected with the write enable pin (\overline{W}). An output high on \overline{W} controls the state of the output buffers making delayed write and read-modify-write cycles possible. The DQ pins provide TTL compatible inputs and three-state TTL compatible outputs with a fan-out of two standard TTL loads. Data-out has the same polarity as data-in.

Write Enable

The read mode or write modes are determined by the state of the write enable pin (\overline{W}). A logic high on \overline{W} selects the read mode and a logic low on \overline{W} selects the write mode. When \overline{W} is high (read mode), the data inputs are disabled. If \overline{W} goes low and satisfies the write command set-up time (t_{WCS}) before \overline{CAS} goes low, the data outputs will remain in the high-impedance state for the duration of the cycle. This allows a write cycle to occur regardless of the state of the output enable (\overline{G}).

Output Enable

The output buffers are controlled by both \overline{CAS} and output enable (\overline{G}). If either \overline{CAS} or \overline{G} are high the output buffers are in the high impedance state. During a read or read-modify-write cycle if both \overline{CAS} and \overline{G} are low, the output buffers are enabled. During an early write cycle \overline{G} has no effect on the output buffers.

Data Inputs

Data may be written into the MB81416 during a write or read-modify-write cycle. The last falling edge of \overline{CAS} or \overline{W} , strobes the data into the 4 on-chip data latches. In an early-write cycle, \overline{W} is brought low prior to \overline{CAS} , and the data is strobed in by \overline{CAS} with both the set-up time (t_{DS}) and hold time (t_{DH}) referenced to the falling edge of \overline{CAS} . The outputs are in the high impedance state regardless of \overline{G} 's state. In a delayed write or a read-modify-write cycle, \overline{W} is brought low after \overline{CAS} , data is strobed-in by \overline{W} , and set-up and hold times are referenced to \overline{W} . To avoid buss contention on I/O pins, it is necessary during a delayed write or a read-modify-write cycle for \overline{G} to be high prior to data input so that the output buffers are in the high impedance state when data is being written.

Data Outputs

Data can be read from the MB81416 with either a read or a read-modify-write cycle. These cycles begin with the outputs in the high impedance state. The outputs contain active, valid data only after both \overline{CAS} and \overline{G} have been brought low and have satisfied the minimum access time from \overline{RAS} (t_{RAC}) and the minimum access time from the output enable t_{OED} . Outputs contain valid data as long as both \overline{CAS} and \overline{G} are held low. They return to the high impedance state when either \overline{CAS} or \overline{G} go high.

\overline{RAS} -Only Refresh

The MB81416's dynamic memory cells may be refreshed by performing any memory cycle at each of the 128 row addresses (A_0 through A_6) at least

every 2 milliseconds. When a row is accessed all bits in the row are refreshed. During refresh, A_7 (Pin 10) is not used and either V_{IH} or V_{IL} may be applied to this pin.

\overline{RAS} -only Refresh is a simplified cycle that consists of strobing a row address with \overline{RAS} while \overline{CAS} remains high. During a \overline{RAS} -only Refresh cycle, \overline{CAS} is high and the output buffers are in the high impedance state. Strobing each of the 128 row addresses (A_0 through A_6) with \overline{RAS} will refresh all 65,536 memory cells in the MB81416. \overline{RAS} -only Refresh results in a substantial reduction in power dissipation compared to a full $\overline{RAS}/\overline{CAS}$ memory cycle.

\overline{CAS} Before \overline{RAS} Refresh

\overline{CAS} before \overline{RAS} refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If \overline{CAS} is held low for the specified set-up time (t_{FCS}) before \overline{RAS} goes low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next \overline{CAS} before \overline{RAS} refresh operation.

Hidden \overline{CAS} Before \overline{RAS} Refresh

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the \overline{CAS} active time and cycling \overline{RAS} . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have \overline{CAS} before \overline{RAS} refresh capability.

\overline{CAS} Before \overline{RAS} Refresh Counter Test Cycle

A special timing sequence using the \overline{CAS} before \overline{RAS} Refresh Counter Test Cycle provides a convenient way to verify the functionality of the \overline{CAS} before \overline{RAS} refresh circuitry. The cycle

*Note: \overline{CAS} Before \overline{RAS} Refresh available on request.

begins with a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ operation. Then $\overline{\text{CAS}}$ is cycled "high" and then "low". This enables a read, write, or read-modify-write operation to occur. Four memory cells are accessed with the location defined as follows:

Row Address — Bits A_0 through A_6 are supplied by the on-chip refresh counter. Bit A_7 is set low internally.

Column Address — Bits A_1 through A_6 are strobed-in by the falling edge of $\overline{\text{CAS}}$ as in a normal memory cycle.

Suggested $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Procedure

The $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Counter Test Cycle timing is used in each of

the following steps:

1. Initialized the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into each set of 4 memory cells at a single column address and 128 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 128 times so that "highs" are written into the 128 sets of 4 memory cells.
4. Read the highs written during step 3.
5. Compliment the test pattern and repeat steps 2, 3, and 4.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to read, write, or read-modify-write. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{\text{RAS}}$ is kept low to maintain the row address, $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to setup and strobe sequential row addresses for the same page. Up to 64 nibble wide words may be accessed with the same row address.