MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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by DRAMCARDFAM/D

MCM16100R8
MCM16200R8
MCM18100R8
MCM18200R8
MCM32100R8
MCM32200R8
MCM36100R8
MCM36200R8

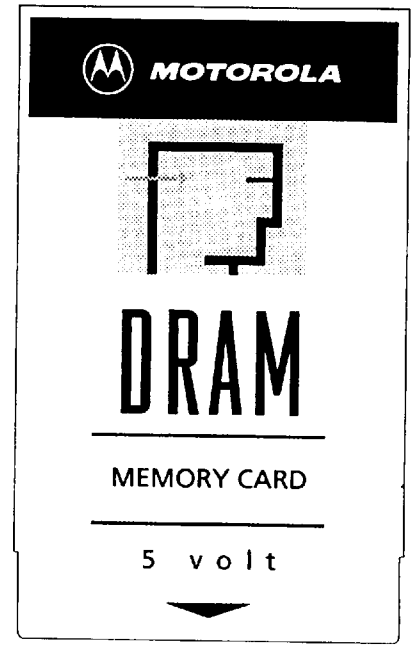
Product Preview

DRAM Memory Card Family

The Motorola 5 V DRAM memory card family products are organized in either one or two memory banks of 1,048,576 x 16, 18, 32, or 36 bits. The x32 and x36 products are fully compliant to the JEIDA standard Type 1, 88-pin card. All cards conform to the JEDEC standard Type 1, 88-pin card consisting of low power MCM5L4400A DRAMs mounted on a thin substrate along with 1M x 1 TSOP parity DRAMs (where required), decoupling capacitors, and input buffers. The final assembly is enclosed in an 88-pin Type 1 PC Card frame. All inputs with the exception of $\overline{RAS}$ are buffered for reduced reflections and compatibility with the JEDEC industry standard. The MCM5L4400A is a low power, 0.7µ CMOS, high speed, dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Ideal for Portable System Applications
- Designed for Industry Standard 5 V Operation
- PC Card Interface Provides for Simple Installation
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast-Page Mode Capability
- TTL-Compatible
- Battery Backup Mode for Low Power Applications
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh = 128 ms
- Consists of:
  - **1M x 16 Card:** Four 1M x 4 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **2M x 16 Card:** Eight 1M x 4 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **1M x 18 Card:** Four 1M x 4 DRAMs, Two 1M x 1 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **2M x 18 Card:** Eight 1M x 4 DRAMs, Four 1M x 1 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **1M x 32 Card:** Eight 1M x 4 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **2M x 32 Card:** Sixteen 1M x 4 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **1M x 36 Card:** Eight 1M x 4 DRAMs, Four 1M x 1 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
  - **2M x 36 Card:** Sixteen 1M x 4 DRAMs, Eight 1M x 1 DRAMs, 0.22 µF Decoupling Capacitors, and Input Buffers
- Fast Access Time (t_{RAC}): 60 ns, 70 ns for Each Product
- Low Active Power Dissipation: MCM36200R8-60 = 7.6 W (Abs. Max for All Cards)
  MCM36200R8-70 = 6.48 W (Abs. Max for All Cards)
- Low Standby Power Dissipation: TTL Levels = 337 mW (Abs. Max)
  CMOS Levels = 26 mW (Abs. Max)

R PACKAGE
88-PIN MEMORY CARD
CASE 1102A-01



PIN NAMES			
$\overline{A0}$ – $\overline{A9}$	Address Inputs	DQ0 – DQ35	Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe	PD1 – PD8	Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$	Row Address Strobe	$\overline{W}$	Read/Write Input
V_{CC}	Power (+ 5 V)	V_{SS}	Ground
NC	No Connection		

All power supply and ground pins must be connected for proper operation of the device.

PRESENCE DETECT PIN OUT		
Pin Name	**60 ns**	**70 ns**
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	V_{SS}	V_{SS}
PD4	V_{SS}	V_{SS}
PD5 (All 1M)	NC	NC
PD5 (All 2M	V_{SS}	V_{SS}
PD6	NC	V_{SS}
PD7	NC	NC
PD8	NC	NC

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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CARD PIN OUT

1M x 16 and 2M x 16			
Bottom		Top	
Pin	Name	Pin	Name
45	V_{SS}	1	V_{SS}
46	NC	2	DQ0
47	NC	3	DQ1
48	NC	4	DQ2
49	NC	5	DQ3
50	NC	6	DQ4
51	NC	7	DQ5
52	NC	8	DQ6
53	NC	9	V_{CC}
54	NC	10	DQ7
55	NC	11	NC
56	V_{SS}	12	NC
57	A1	13	A0
58	A3	14	A2
59	A5	15	V_{CC}
60	A7	16	A4
61	A9	17	NC
62	NC	18	A6
63	V_{SS}	19	A8
64	NC	20	NC
65	*	21	NC
66	NC	22	$\overline{RAS0}$
67	V_{SS}	23	$\overline{CAS0}$
68	NC	24	$\overline{CAS1}$
69	NC	25	NC
70	$\overline{W}$	26	NC
71	PD1	27	V_{CC}
72	PD3	28	PD2
73	V_{SS}	29	PD4
74	PD5	30	PD6
75	PD7	31	NC
76	PD8	32	NC
77	NC	33	NC
78	NC	34	DQ8
79	NC	35	NC
80	NC	36	DQ9
81	NC	37	V_{CC}
82	NC	38	DQ10
83	NC	39	DQ11
84	NC	40	DQ12
85	NC	41	DQ13
86	NC	42	DQ14
87	NC	43	DQ15
88	V_{SS}	44	V_{SS}

CARD PIN OUT KEY

Pin	MCM16100R8 MCM18100R8	MCM16200R8 MCM18200R8
65	NC	$\overline{RAS1}$

CARD PIN OUT

1M x 18 and 2M x 18			
Bottom		Top	
Pin	Name	Pin	Name
45	V_{SS}	1	V_{SS}
46	NC	2	DQ0
47	NC	3	DQ1
48	NC	4	DQ2
49	NC	5	DQ3
50	NC	6	DQ4
51	NC	7	DQ5
52	NC	8	DQ6
53	NC	9	V_{CC}
54	NC	10	DQ7
55	NC	11	NC
56	V_{SS}	12	DQ8
57	A1	13	A0
58	A3	14	A2
59	A5	15	V_{CC}
60	A7	16	A4
61	A9	17	NC
62	NC	18	A6
63	V_{SS}	19	A8
64	NC	20	NC
65	*	21	NC
66	NC	22	$\overline{RAS0}$
67	V_{SS}	23	$\overline{CAS0}$
68	NC	24	$\overline{CAS1}$
69	NC	25	NC
70	$\overline{W}$	26	NC
71	PD1	27	V_{CC}
72	PD3	28	PD2
73	V_{SS}	29	PD4
74	PD5	30	PD6
75	PD7	31	NC
76	PD8	32	NC
77	NC	33	DQ17
78	NC	34	DQ9
79	NC	35	NC
80	NC	36	DQ10
81	NC	37	V_{CC}
82	NC	38	DQ11
83	NC	39	DQ12
84	NC	40	DQ13
85	NC	41	DQ14
86	NC	42	DQ15
87	NC	43	DQ16
88	V_{SS}	44	V_{SS}

CARD PIN OUT

1M x 32 and 2M x 32			
Bottom		Top	
Pin	Name	Pin	Name
45	V_{SS}	1	V_{SS}
46	DQ16	2	DQ0
47	DQ17	3	DQ1
48	DQ18	4	DQ2
49	DQ19	5	DQ3
50	DQ20	6	DQ4
51	DQ21	7	DQ5
52	DQ22	8	DQ6
53	DQ23	9	V_{CC}
54	NC	10	DQ7
55	NC	11	NC
56	V_{SS}	12	NC
57	A1	13	A0
58	A3	14	A2
59	A5	15	V_{CC}
60	A7	16	A4
61	A9	17	NC
62	NC	18	A6
63	V_{SS}	19	A8
64	NC	20	NC
65	*	21	NC
66	$\overline{CAS2}$	22	$\overline{RAS0}$
67	V_{SS}	23	$\overline{CAS0}$
68	$\overline{CAS3}$	24	$\overline{CAS1}$
69	*	25	NC
70	$\overline{W}$	26	$\overline{RAS2}$
71	PD1	27	V_{CC}
72	PD3	28	PD2
73	V_{SS}	29	PD4
74	PD5	30	PD6
75	PD7	31	NC
76	PD8	32	NC
77	NC	33	NC
78	NC	34	DQ8
79	NC	35	NC
80	DQ24	36	DQ9
81	DQ25	37	V_{CC}
82	DQ26	38	DQ10
83	DQ27	39	DQ11
84	DQ28	40	DQ12
85	DQ29	41	DQ13
86	DQ30	42	DQ14
87	DQ31	43	DQ15
88	V_{SS}	44	V_{SS}

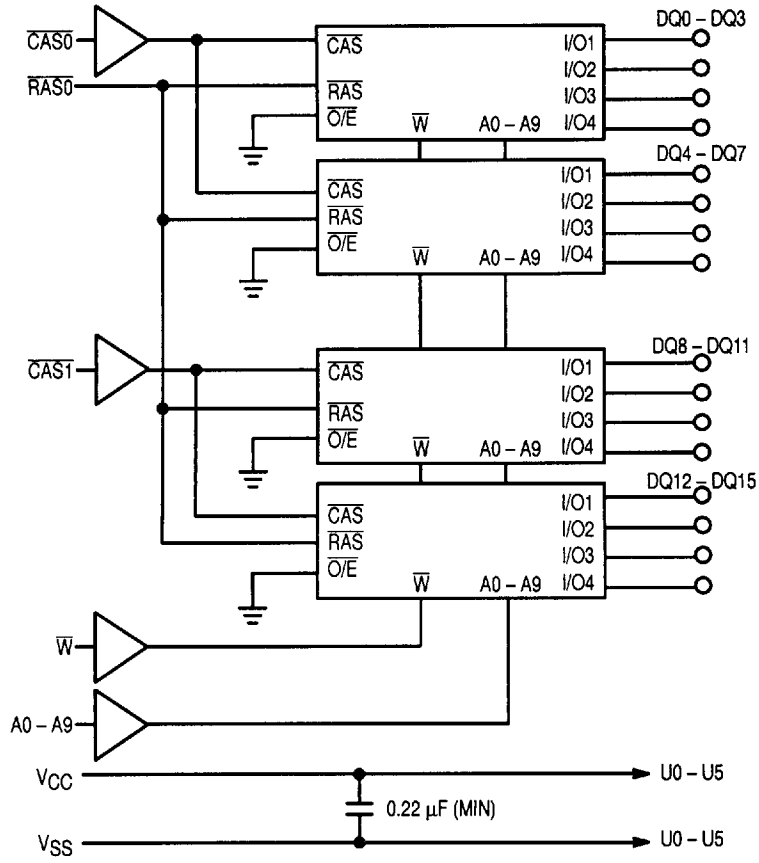
CARD PIN OUT KEY

Pin	MCM32100R8 MCM36100R8	MCM32200R8 MCM36200R8
65	NC	$\overline{RAS1}$
69	NC	$\overline{RAS3}$

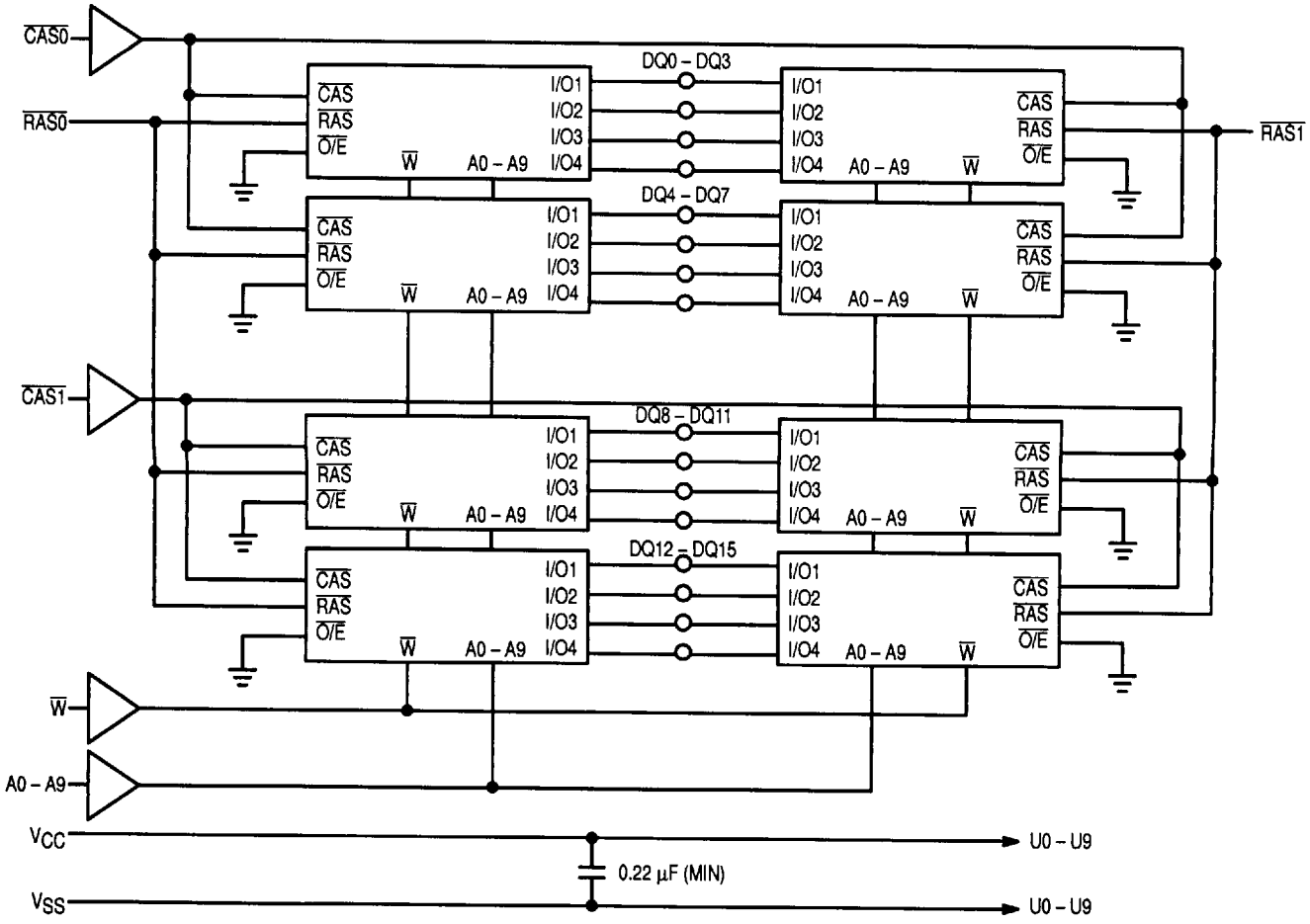
CARD PIN OUT

1M x 36 and 2M x 36			
Bottom		Top	
Pin	Name	Pin	Name
45	V_{SS}	1	V_{SS}
46	DQ18	2	DQ0
47	DQ19	3	DQ1
48	DQ20	4	DQ2
49	DQ21	5	DQ3
50	DQ22	6	DQ4
51	DQ23	7	DQ5
52	DQ24	8	DQ6
53	DQ25	9	V_{CC}
54	DQ26	10	DQ7
55	NC	11	NC
56	V_{SS}	12	DQ8
57	A1	13	A0
58	A3	14	A2
59	A5	15	V_{CC}
60	A7	16	A4
61	A9	17	NC
62	NC	18	A6
63	V_{SS}	19	A8
64	NC	20	NC
65	*	21	NC
66	$\overline{CAS2}$	22	$\overline{RAS0}$
67	V_{SS}	23	$\overline{CAS0}$
68	$\overline{CAS3}$	24	$\overline{CAS1}$
69	*	25	NC
70	$\overline{W}$	26	$\overline{RAS2}$
71	PD1	27	V_{CC}
72	PD3	28	PD2
73	V_{SS}	29	PD4
74	PD5	30	PD6
75	PD7	31	NC
76	PD8	32	NC
77	NC	33	DQ17
78	NC	34	DQ9
79	DQ35	35	NC
80	DQ27	36	DQ10
81	DQ28	37	V_{CC}
82	DQ29	38	DQ11
83	DQ30	39	DQ12
84	DQ31	40	DQ13
85	DQ32	41	DQ14
86	DQ33	42	DQ15
87	DQ34	43	DQ16
88	V_{SS}	44	V_{SS}

MCM16100R8 BLOCK DIAGRAM



MCM16200R8 BLOCK DIAGRAM



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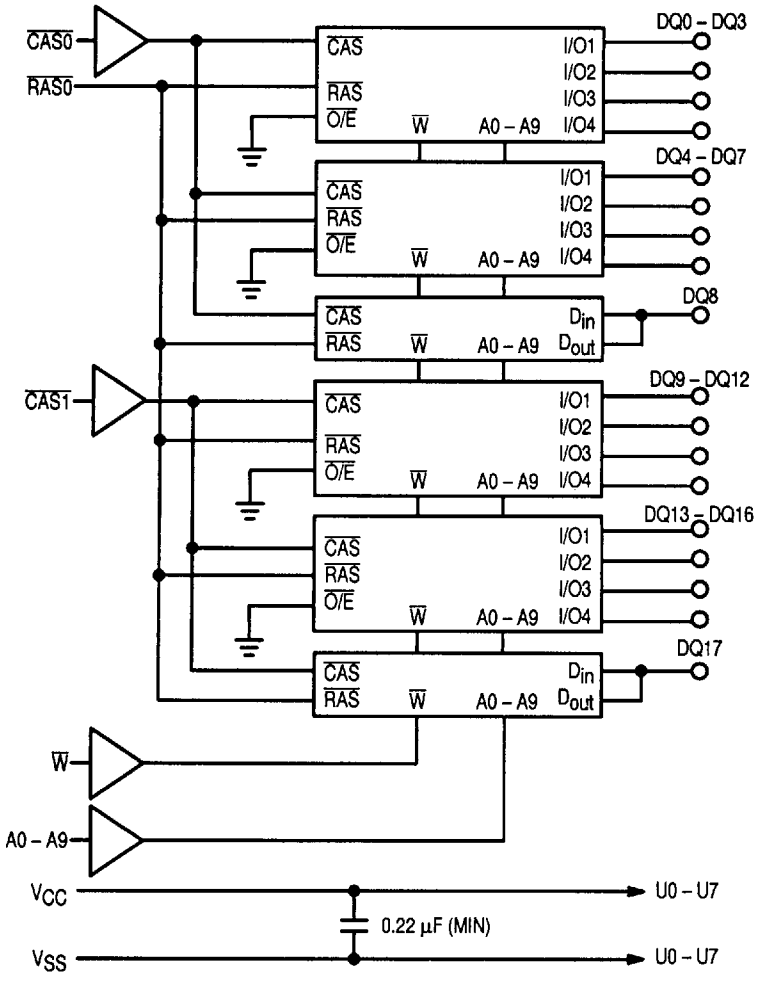

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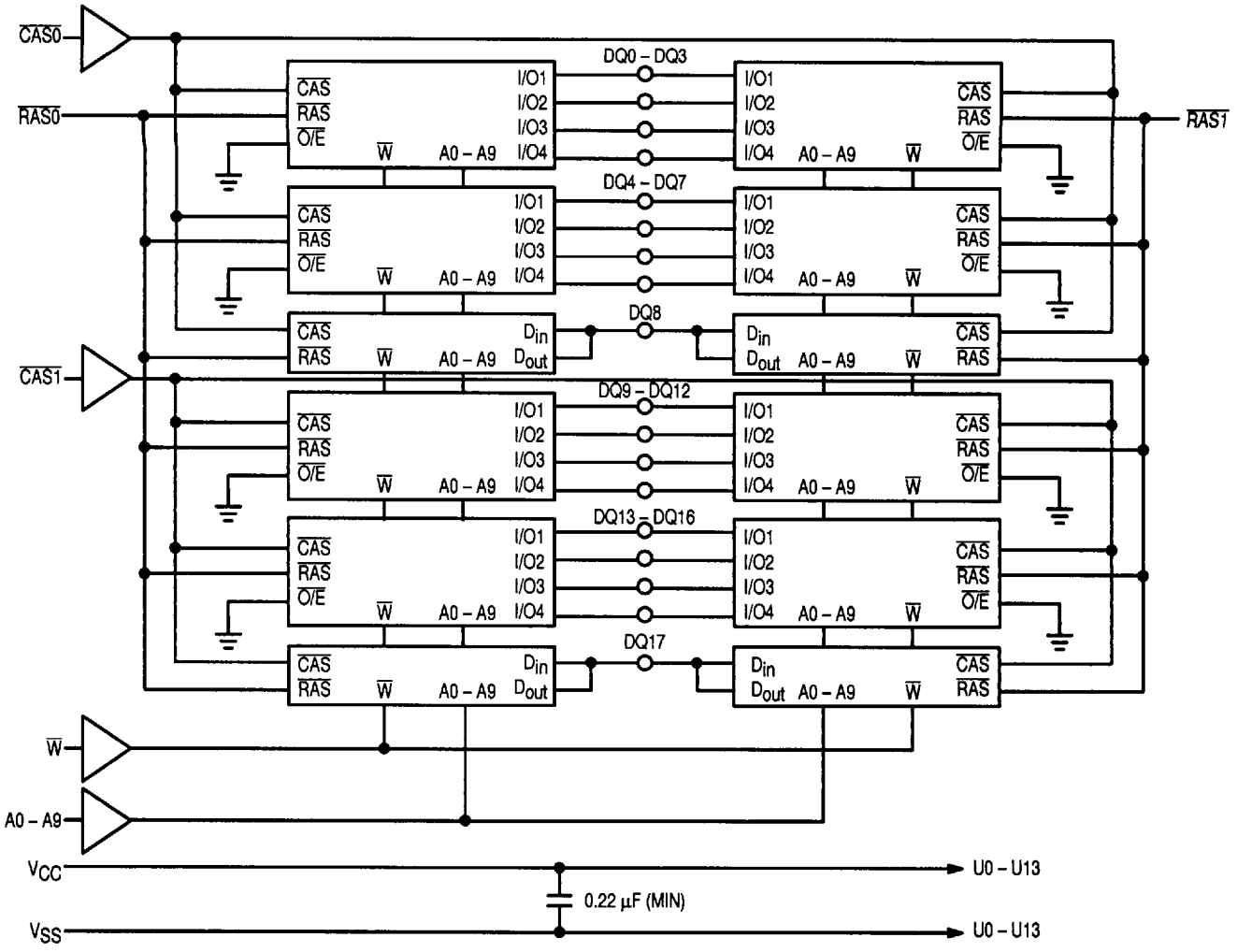

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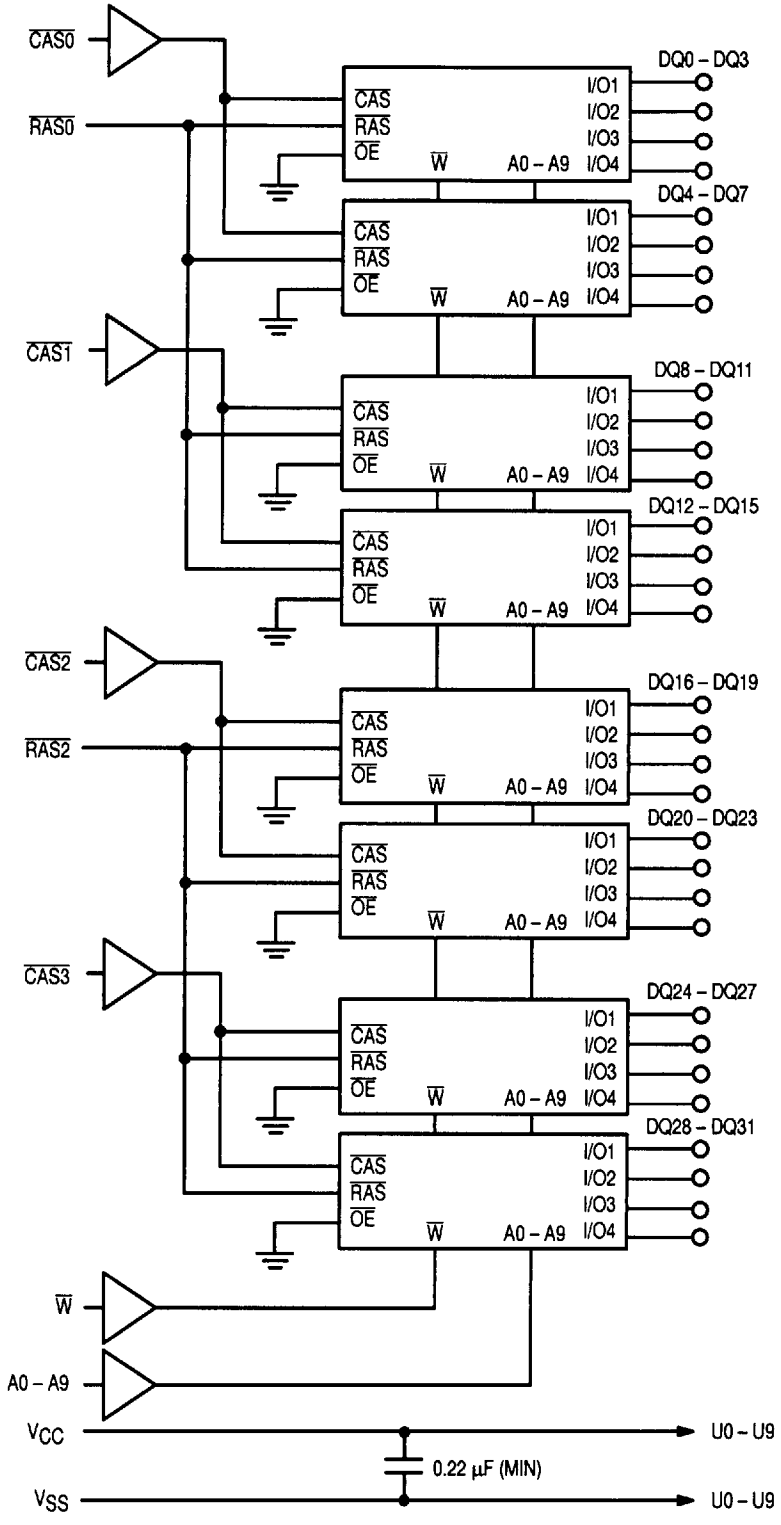

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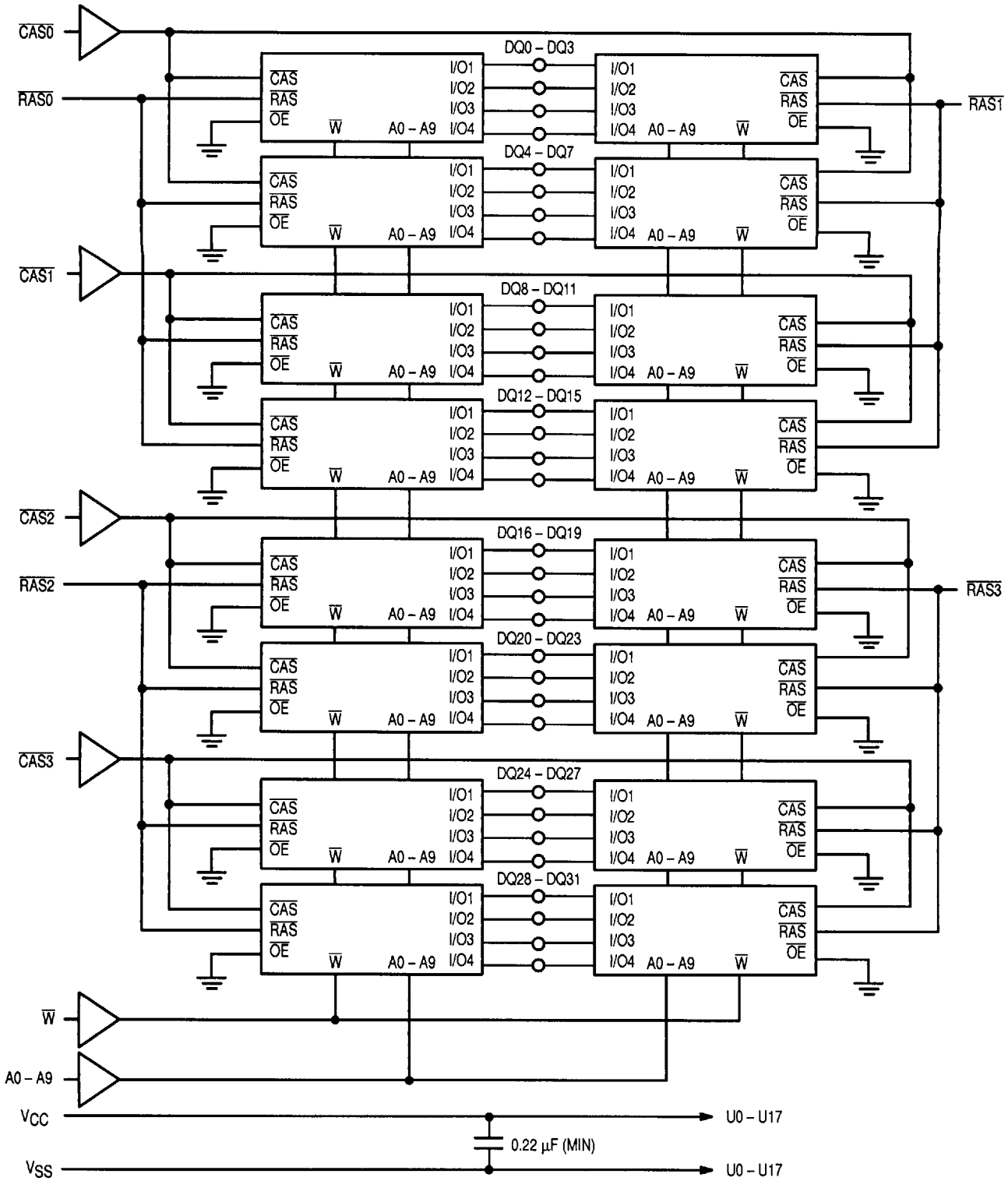
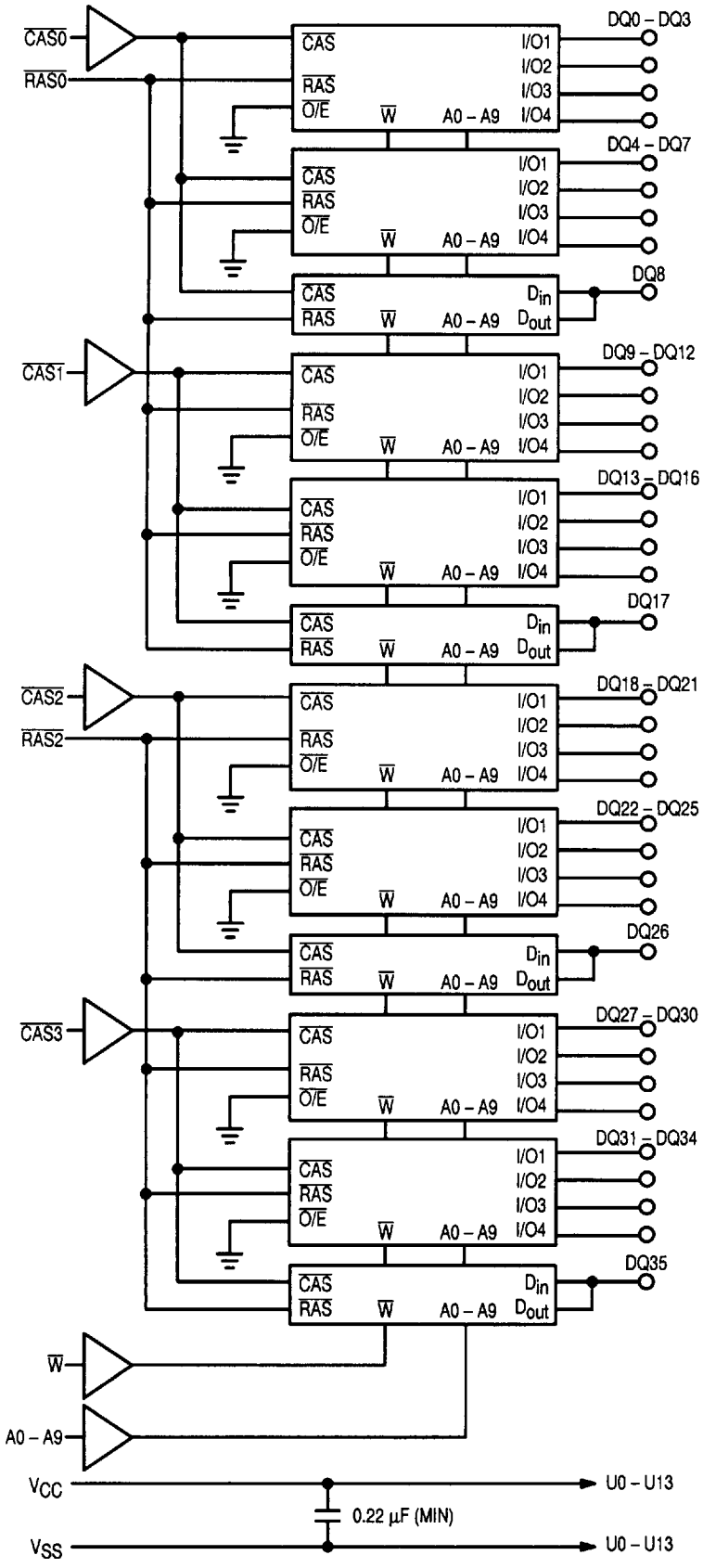
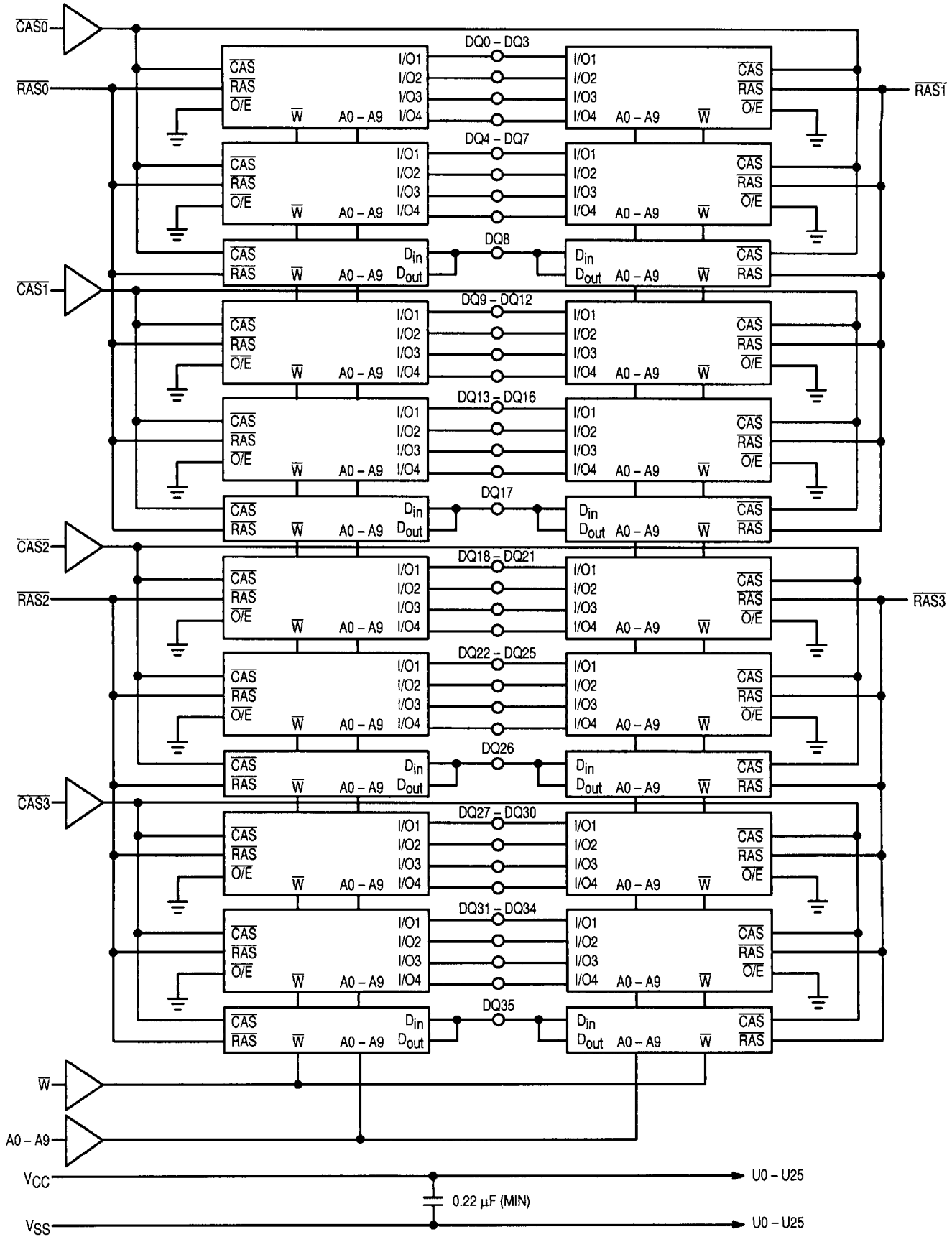


MCM36100R8 BLOCK DIAGRAM



MCM36200R8 BLOCK DIAGRAM



LOW ACTIVE POWER DISSIPATION

	60 ns	70 ns	Units
MCM16100R8	2.77	2.32	W
MCM16200R8	2.86	2.41	W
MCM18100R8	3.74	3.19	W
MCM18200R8	3.89	3.32	W
MCM32100R8	5.58	4.67	W
MCM32200R8	5.67	4.76	W
MCM36100R8	7.30	6.21	W
MCM36200R8	7.60	6.48	W

LOW STANDBY POWER DISSIPATION

	TTL Levels	CMOS Levels	Units
MCM16100R8	127	5	mW
MCM16200R8	169	9	mW
MCM18100R8	148	7	mW
MCM18200R8	210	13	mW
MCM32100R8	169	9	mW
MCM32200R8	253	18	mW
MCM36100R8	211	13	mW
MCM36200R8	337	26	mW

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	8	W
Operating Temperature Range	T_A	0 to + 55	°C
Storage Temperature Range	T_{stg}	– 20 to + 65	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to 55°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.25	5.0	5.25	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	MCM16100R8		MCM16200R8		MCM18100R8		MCM18200R8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC} Power Supply Current	I_{CC1}									mA	1
t_{RC} = 110 ns		—	528	—	744	—	715	—	744		
t_{RC} = 130 ns		—	444	—	635	—	609	—	635		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	24	—	40	—	28	—	40	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles	I_{CC3}									mA	1
t_{RC} = 110 ns		—	528	—	744	—	715	—	744		
t_{RC} = 130 ns		—	444	—	635	—	609	—	635		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}									mA	1
t_{PC} = 35 ns		—	353	—	526	—	920	—	526		
t_{PC} = 40 ns		—	346	—	514	—	907	—	514		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1	—	2.6	—	1.4	—	2.6	mA	3
V_{CC} Power Supply Current During $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	I_{CC6}									mA	1
t_{RC} = 110 ns		—	528	—	744	—	715	—	744		
t_{RC} = 130 ns		—	444	—	635	—	609	—	635		
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; DQ = V_{CC} – 0.2 V, 0.2 V or OPEN; A0 – A9 = V_{CC} – 0.2 V) t_{RAS} = min to 1 µs	I_{CC7}	—	1.4	—	3.8	—	2	—	3.8	mA	1, 2
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$) (All other pins not under test = 0 V)	$I_{lkg(I)}$	– 40	40	– 40	40	– 60	60	– 60	60	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} < V_{in} < V_{CC}$)	$I_{lkg(O)}$	– 10	10	– 20	20	– 10	10	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	

NOTES:
1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
2. t_{RAS} (max) = 1 µs is only applied of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.
3. All inputs must be stable (CMOS levels).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	MCM32100R8		MCM32200R8		MCM36100R8		MCM36200R8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{CC} Power Supply Current t_{RC} = 110 ns t_{RC} = 130 ns	I_{CC1}	 — —	 1068 894	 — —	 1084 910	 — —	 1393 1185	 — —	 1452 1238	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	32	—	48	—	40	—	64	mA	
V_{CC} Power Supply Current During $\overline{RAS}$-Only Refresh Cycles t_{RC} = 110 ns t_{RC} = 130 ns	I_{CC3}	 — —	 1068 894	 — —	 1084 910	 — —	 1393 1185	 — —	 1452 1238	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle t_{PC} = 35 ns t_{PC} = 40 ns	I_{CC4}	 — —	 740 720	 — —	 756 736	 — —	 920 907	 — —	 1004 984	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	1.8	—	3.4	—	2.6	—	5	mA	3
V_{CC} Power Supply Current During $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle t_{RC} = 110 ns t_{RC} = 130 ns	I_{CC6}	 — —	 1068 894	 — —	 1084 910	 — —	 1393 1185	 — —	 1452 1238	mA	1
V_{CC} Power Supply Current, Battery Backup Mode (t_{RC} = 125 µs; $\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2 V; $\overline{W}$ = V_{CC} – 0.2 V; DQ = V_{CC} – 0.2 V, 0.2 V or OPEN; A0 – A9 = V_{CC} – 0.2 V) t_{RAS} = min to 1 µs	I_{CC7}	—	2.6	—	5	—	3.8	—	7.4	mA	1, 2
Input Leakage Current (V_{SS} < V_{in} < V_{CC}) (All other pins not under test = 0 V)	$I_{lkg(I)}$	– 40	40	– 40	40	– 60	60	– 60	60	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, V_{SS} < V_{in} < V_{CC})	$I_{lkg(O)}$	– 10	10	– 20	20	– 10	10	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	

NOTES:
1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
2. t_{RAS} (max) = 1 µs is only applied of battery backup. t_{RAS} (max) = 10 µs is applied to functional operating.
3. All inputs must be stable (CMOS levels).

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	MCM16100R8 MCM32100R8 Max	MCM16200R8 MCM32200R8 Max	MCM18100R8 MCM36100R8 Max	MCM18200R8 MCM36200R8 Max	Unit
Input Capacitance	A0 – A9, $\overline{CAS}$	C_{in}	14	14	14	14	pF
	$\overline{W}$		18	18	18	18	
	$\overline{RAS}$		38	38	52	52	
Input/Output Capacitance	DQ	$C_{I/O}$	17	24	22	34	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to 55°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1 through 5)

Parameter	Symbol		-60		-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	27	—	27	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	37	—	42	ns	6, 9
Access Time from $\overline{CAS}$ Precharge	t_{CEHQZ}	t_{CPA}	—	47	—	47	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	2	—	2	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	2	27	2	27	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	27	—	27	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Page Mode Cycle Only)	t_{CEHREH}	t_{RHCP}	47	—	47	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	58	—	68	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	18	33	18	43	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	13	23	13	28	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	12	—	12	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	7	—	7	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	8	—	8	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	2	—	2	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	37	—	42	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies to all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0 ≤ T_A ≤ 55°C) is ensured.
6. Measured with a current load equivalent to two TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

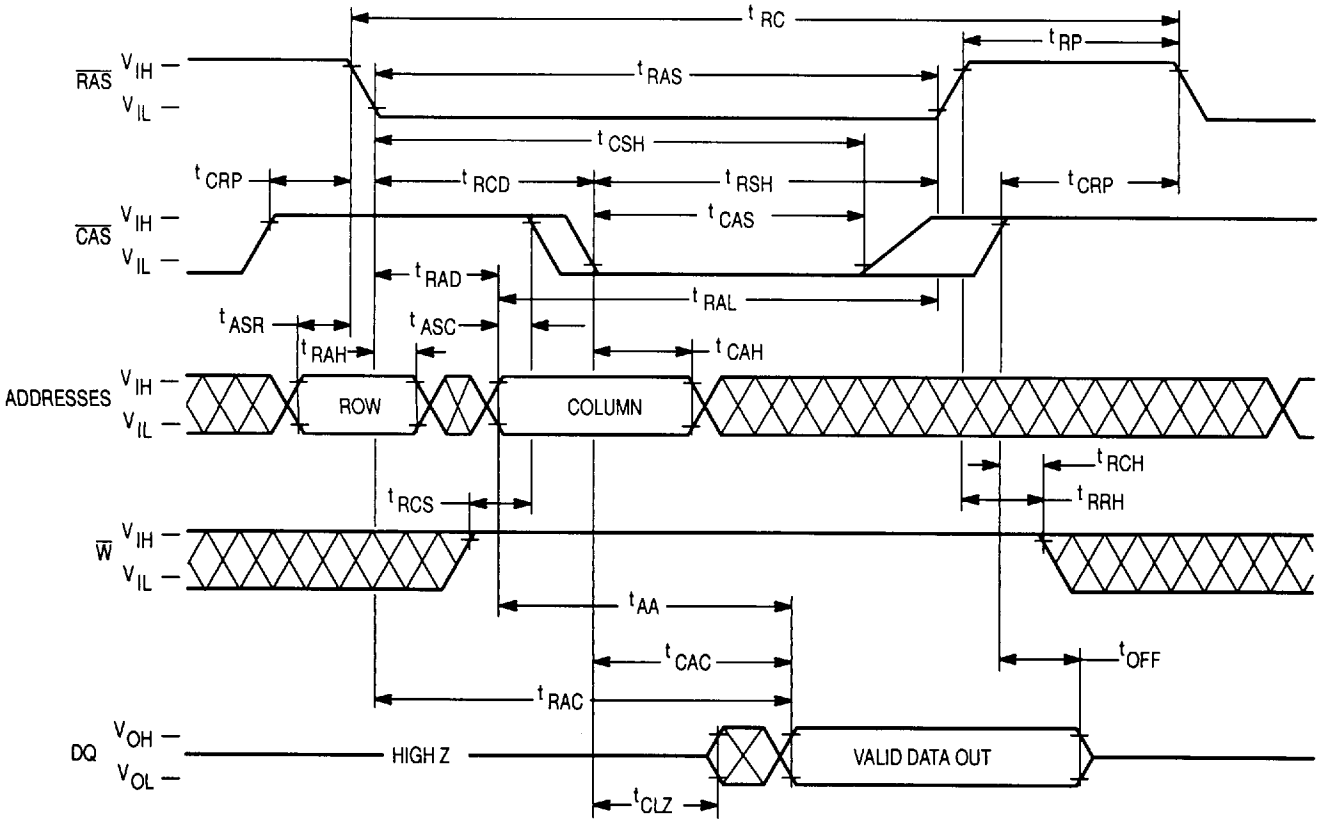
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		-60		-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	2	—	2	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	2	—	2	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	27	—	27	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	2	—	2	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	22	—	22	—	ns	14
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	55	—	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	—	128	—	128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	2	—	2	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$-Before-$\overline{RAS}$ Cycle	t_{RELCEL}	t_{CSR}	12	—	12	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$-Before-$\overline{RAS}$ Cycle	t_{RELCEH}	t_{CHR}	13	—	13	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
$\overline{CAS}$ Prescharge Time for $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	30	—	40	—	ns	

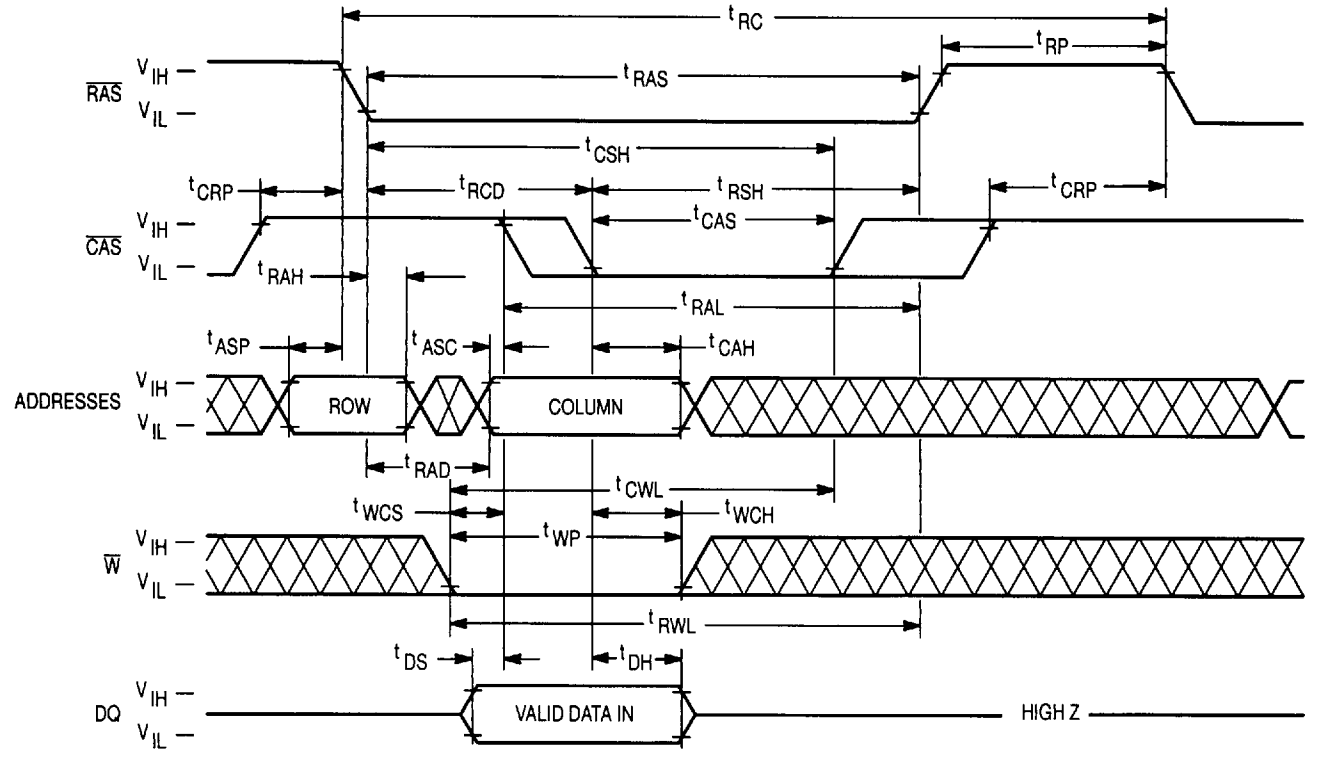
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
16. To avoid bus contention and potential damage to a two bank (2M) card, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

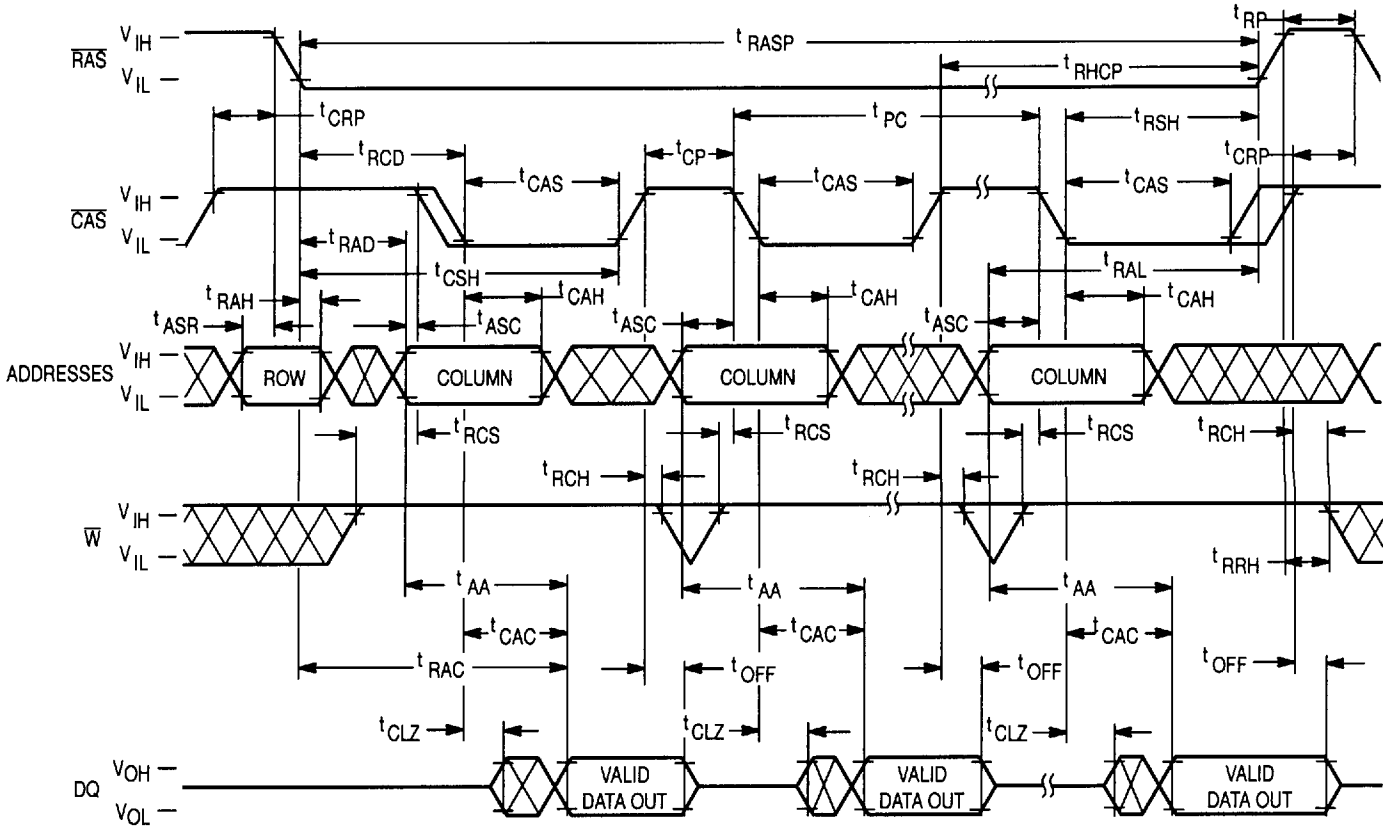
READ CYCLE



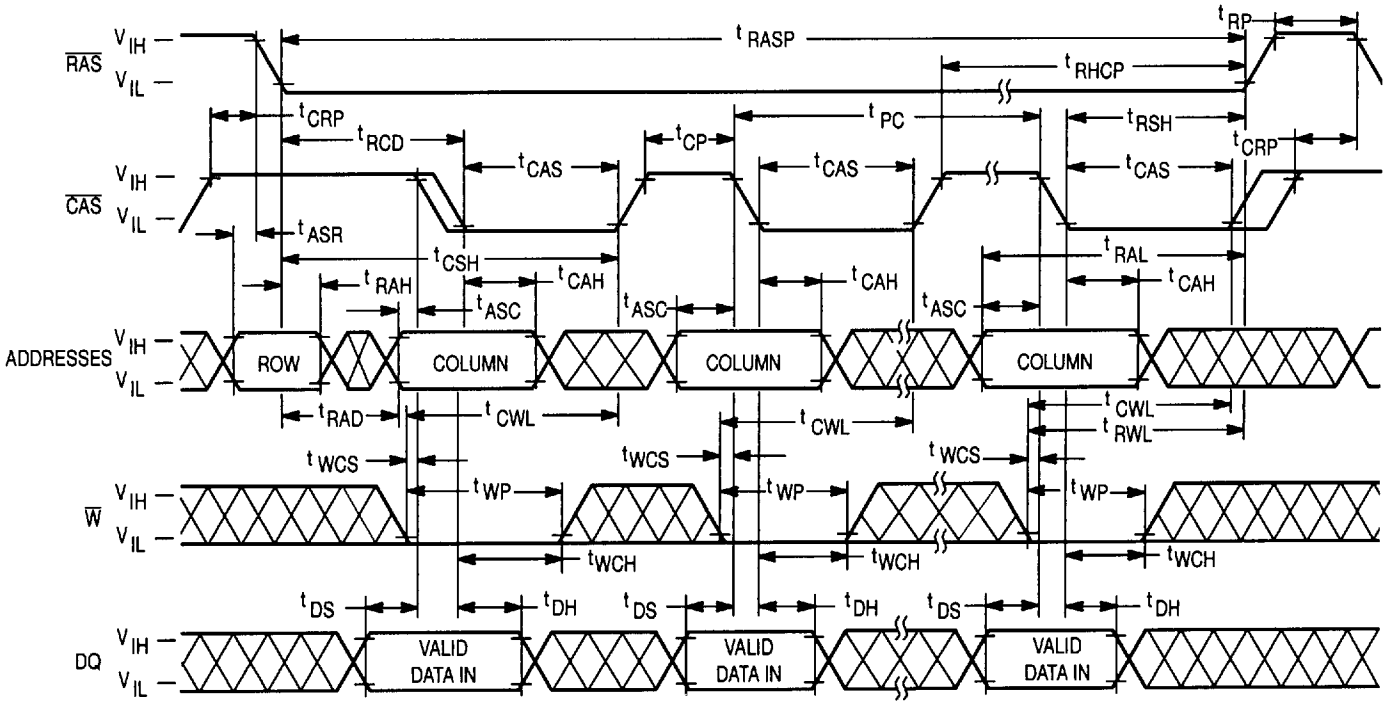
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

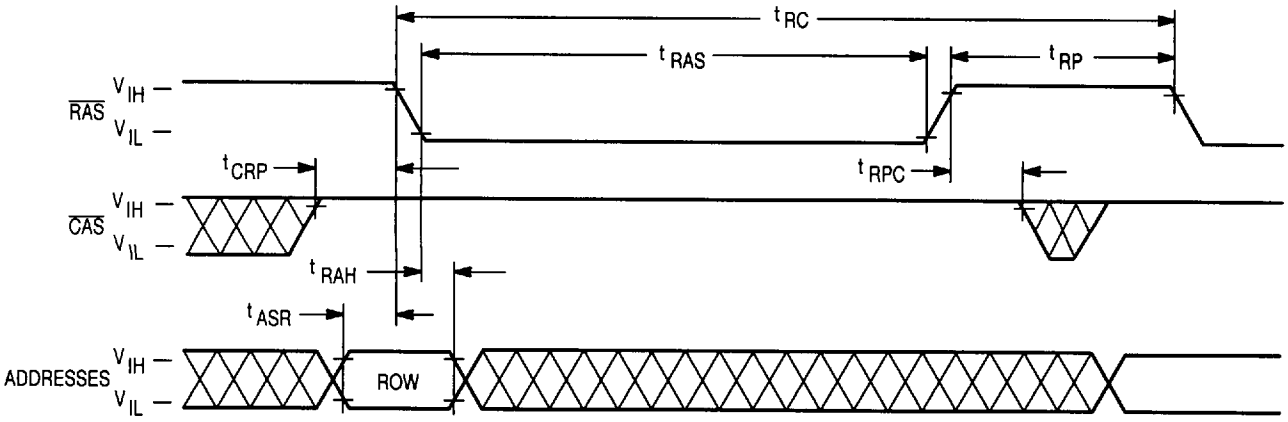


FAST PAGE MODE EARLY WRITE CYCLE



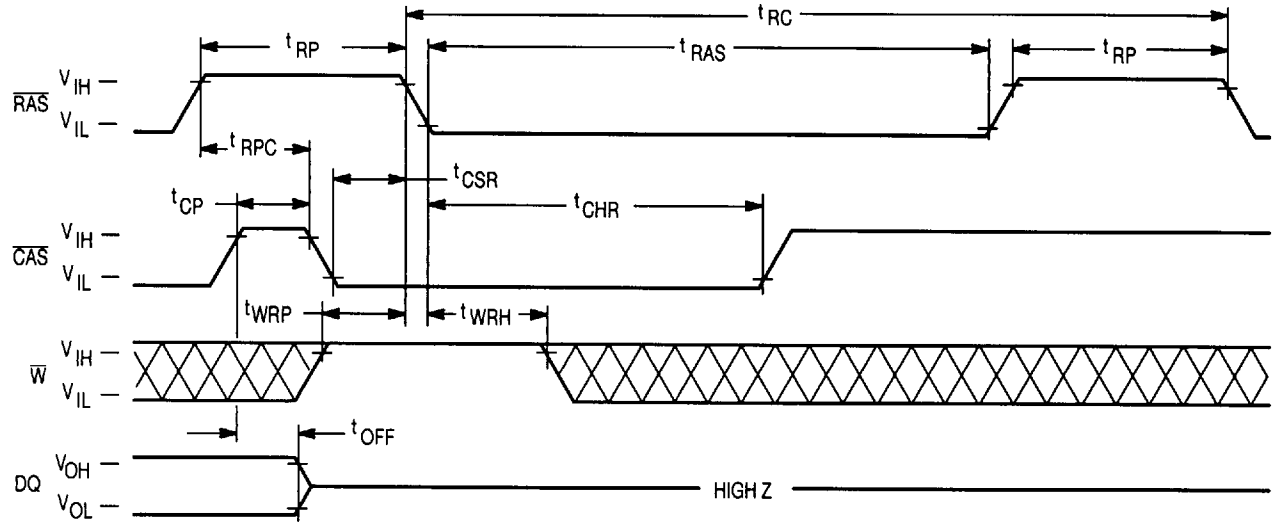
$\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{W}$ is Don't Care)

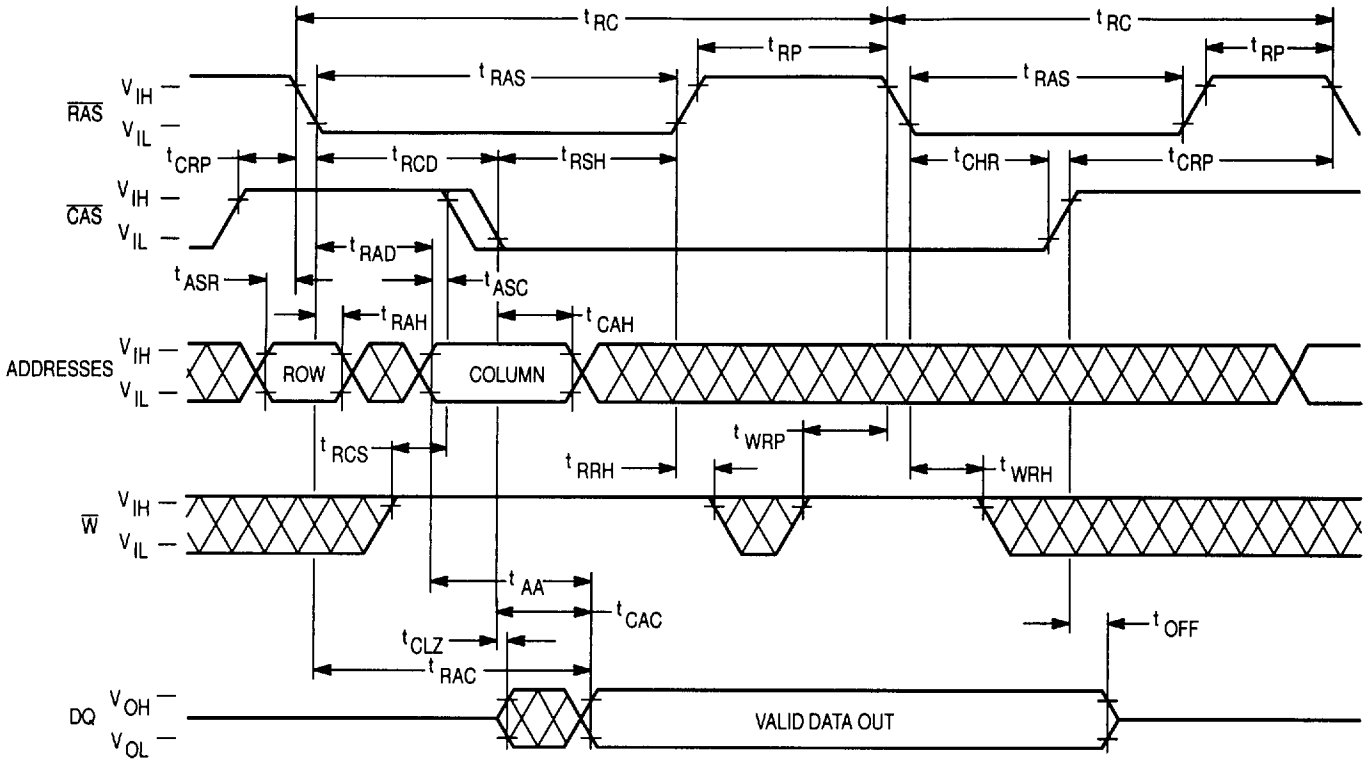


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

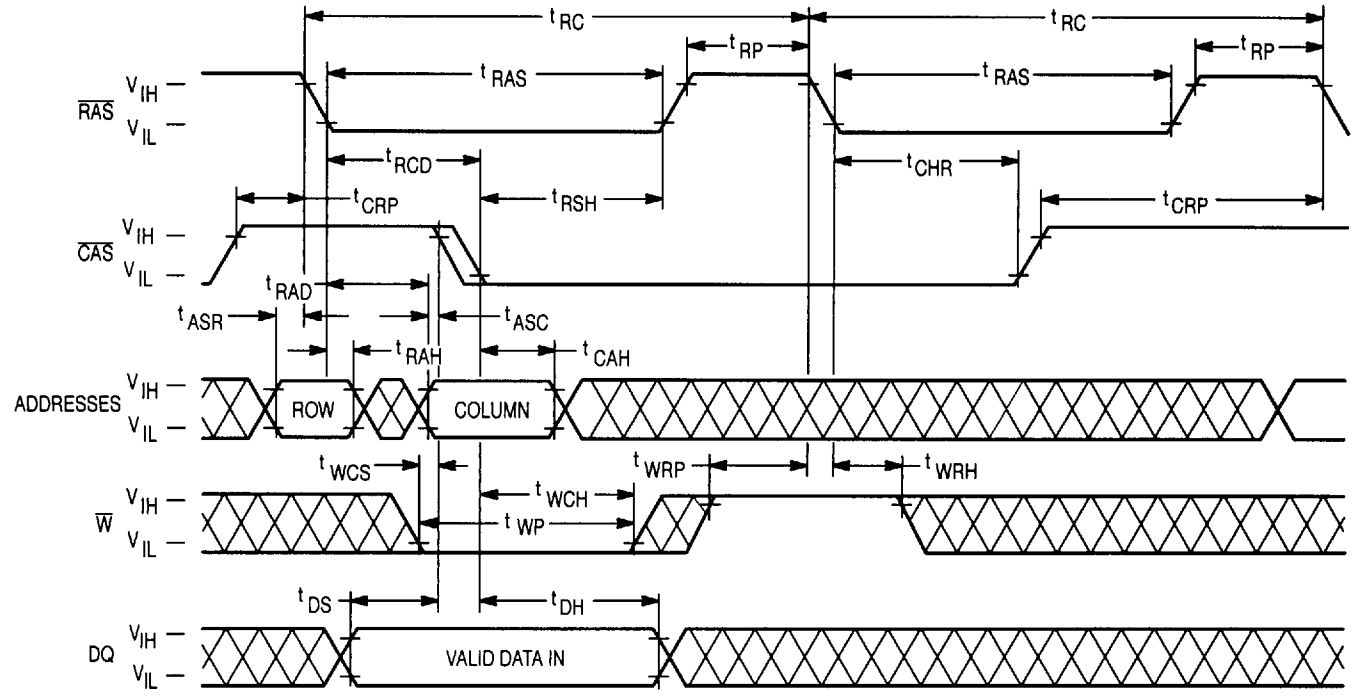
(A0 – A9 are Don't Care)



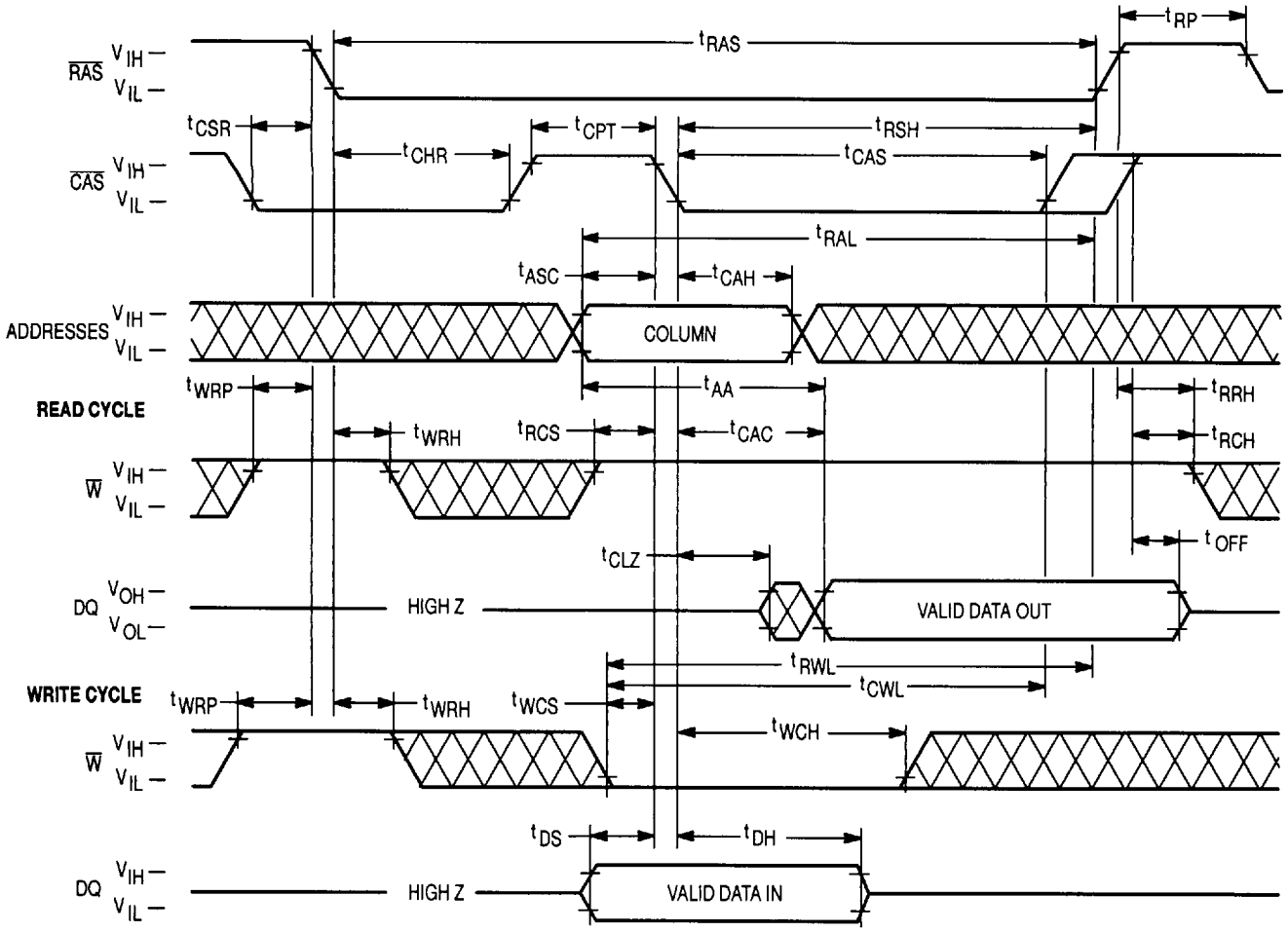
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 128 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in one bank of the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the card: **$\overline{RAS}$ only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the card. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the card require refresh every 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 124.8 microseconds. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 128 milliseconds.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle.** Repeat this operation 1024 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

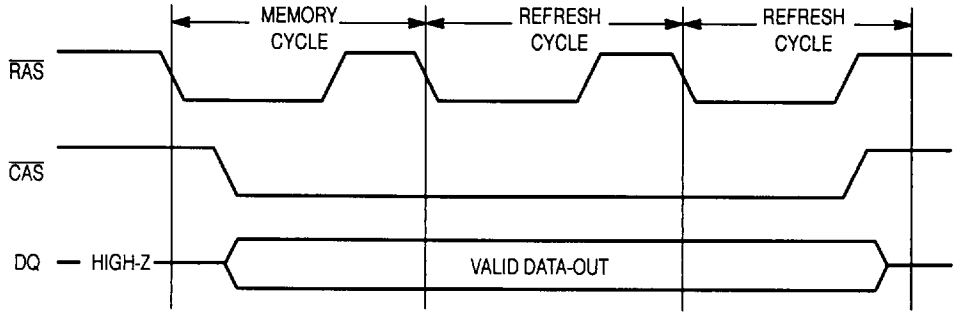


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM XXXXX X XX

Motorola Memory Prefix

Part Number

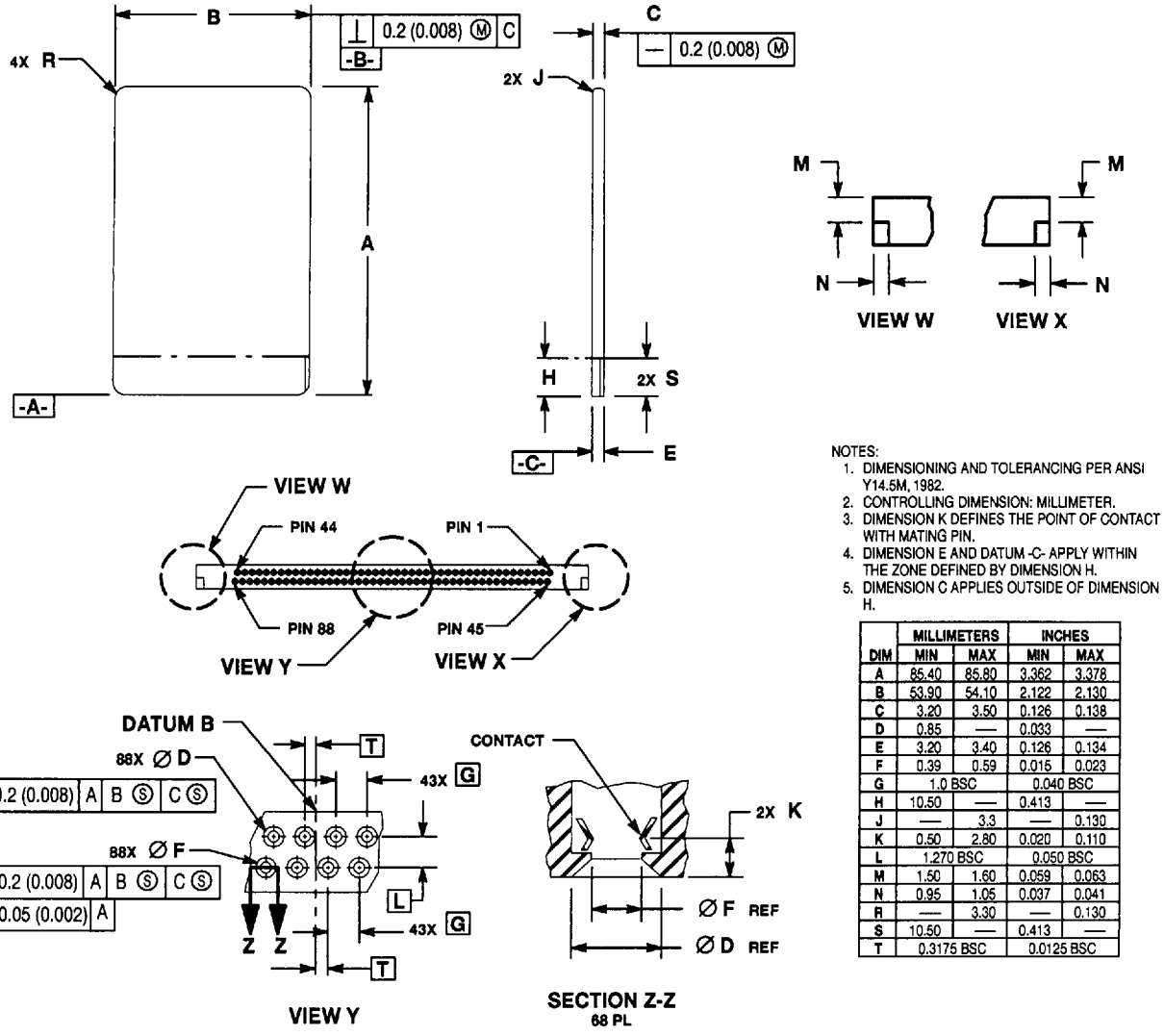
Speed (60 = 60 ns, 70 = 70 ns)

Package (R = 88 Pin Memory Card)

Full Part Numbers —		
	MCM16100R860	MCM16100R870
	MCM16200R860	MCM16200R870
	MCM18100R860	MCM18100R870
	MCM18200R860	MCM18200R870
	MCM32100R860	MCM32100R870
	MCM32200R860	MCM32200R870
	MCM36100R860	MCM36100R870
	MCM36200R860	MCM36200R870

PACKAGE DIMENSIONS

R PACKAGE
88-PIN MEMORY CARD
CASE 1102A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION K DEFINES THE POINT OF CONTACT WITH MATING PIN.
4. DIMENSION E AND DATUM -C- APPLY WITHIN THE ZONE DEFINED BY DIMENSION H.
5. DIMENSION C APPLIES OUTSIDE OF DIMENSION H.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	85.40	85.80	3.362	3.378
B	53.90	54.10	2.122	2.130
C	3.20	3.50	0.126	0.138
D	0.85	—	0.033	—
E	3.20	3.40	0.126	0.134
F	0.39	0.59	0.015	0.023
G	1.0 BSC		0.040 BSC	
H	10.50	—	0.413	—
J	—	3.3	—	0.130
K	0.50	2.80	0.020	0.110
L	1.270 BSC		0.050 BSC	
M	1.50	1.60	0.059	0.063
N	0.95	1.05	0.037	0.041
R	—	3.30	—	0.130
S	10.50	—	0.413	—
T	0.3175 BSC		0.0125 BSC	

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