calogic
CORPORATION

N-Channel JFET Switch

T-35-25

J105 – J107

J105 – J107

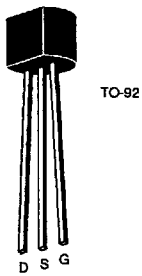
FEATURES

- Low $r_{DS(on)}$

APPLICATIONS

- Analog Switches
- Choppers
- Commutators

PIN CONFIGURATION



5036

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage ..... -25V
Gate Current 50mA
Storage Temperature Range .....-55°C to +150°C
Operating Temperature Range .....-55°C to +135°C
Lead Temperature (Soldering, 10sec) .....+300°C
Power Dissipation 360mW
Derate above 25°C .....3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
J105	Hermetic TO-92	-55°C to +135°C
XJ105	Sorted Chips in Carriers	-55°C to +135°C
J106	Hermetic TO-92	-55°C to +135°C
XJ106	Sorted Chips in Carriers	-55°C to +135°C
J107	Hermetic TO-92	-55°C to +135°C
XJ107	Sorted Chips in Carriers	-55°C to +135°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	J105			J106			J107			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
I_{GSS}	Gate-Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0V, V_{GS} = -15V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4 5	V	V_{DS} = 5V, I_D = 1µA
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0V, I_G = -1µA
I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	V_{DS} = 15V, V_{GS} = 0V
$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5V, V_{GS} = -10V
$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	V_{DS} ≤0.1V, V_{GS} = 0V
$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0V, V_{GS} = -10V (Note 3) — f = 1MHz
$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35		
$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		(Note 3) V_{DS} = V_{GS} = 0V — f = 1MHz
$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time-Test Conditions (Note 3)
t_r	Rise Time		20			20			20			J105 J106 J107
$t_{d(off)}$	Turn Off Delay Time		15			15			15			V_{DD} 1.5V 1.5V 1.5V
t_f	Fall Time		20			20			20			$V_{GS(off)}$ -12V -7V -5V
												R_L 50Ω 50Ω 50Ω

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300µs; duty cycle ≤3%.
3. For design reference only, not 100% tested.