SEEQ Technology Incorporated

Full Duplex

83C95

10BASE-T Ethernet Transceiver With On Chip Filters And AUI

PRELIMINARY

September 9, 1996

SEEQ Full Duplex Designation

Full Duplex

Symbol indentifies product as a Full Duplex device.

Note: Check for latest Data Sheet revision before starting any designs.

Call SEEQ Technology (510) 226-7400 x3051.

SEEQ Data Sheets are now on the Web, access SEEQ Home Page www.seeq.com.

Features

- ***Integrated 10BASET Transceiver With Output Waveshaping And On Chip Filters***
- ***Few External Components***
- ***Direct Interface To SEEQ 8020/8023 Manchester Code Converter MCC™***
- ***Meets All Applicable IEEE 802.3 and 10BASET Standards***
- ***Jitter Attenuation On AUI Input***
- ***Many User Features And Options***
  - ***AUI interface to ENDEC***
  - ***Full Duplex/AutoDUPLEX™ Mode***
  - ***Autopolarity***
  - ***Smart Squelch***
  - ***Long Cable Option***
  - ***Adjustable Transmit Level***
  - ***150 Ohm Cable Interface Option***
  - ***AUI Output High Impedance***
  - ***Powerdown***
  - ***SQE Disable***
  - ***Link Disable***
  - ***Loopback***
- ***LED Outputs***
  - ***Link***
  - ***Transmit Activity***
  - ***Receive Activity***
  - ***Collision***
  - ***Polarity***
  - ***Jabber***
- ***Function Compatible With SEEQ 83C94***
- ***Function Compatible With AM79C100***
- ***28L PLCC***

Description

The 83C95 is a highly integrated analog interface IC for twisted pair Ethernet applications (10BASET).

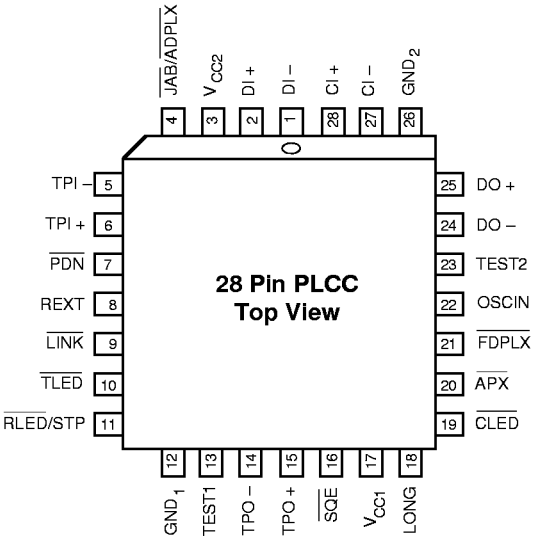
The device consists of transmit waveshaping circuitry, transmit filter, twisted pair line driver, receive filter, twisted pair receiver, and AUI interface to an external ENDEC.

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters and common mode chokes normally required in 10BASET applications.

The 83C95 is ideal for 10BASET external MAU's, embedded MAU's, and can be used for hubs and adapter cards.

The 83C95 is implemented in CMOS technology.

Pin Configuration



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Pin Description

Pin	Pin Name	I/O	Description
1	DI–	O	AUI Transmit Output, Negative
2	DI+	O	AUI Transmit Output, Positive
3	V_{CC2}	--	Positive Supply. +5 volts.
4	$\overline{JAB}$/ ADPLX	I/O Pullup	Jabber Detect output/AutoDUPLEX enable input. This pin consists of an open drain output transistor with a resistor pullup. To enable the Auto-DUPLEX function, tie the pin to GND. Otherwise, the pin is a Jabber Detect output and can drive an LED. $\overline{JAB}$/ADPLX = 1 Output Jabber Not Detected $\overline{JAB}$/ADPLX = 0 Output Jabber Detected $\overline{JAB}$/ADPLX = GND Input AutoDUPLEX Enabled
5	TPI–	I	Twisted Pair Receive Input, Negative
6	TPI+	I	Twisted Pair Receive Input, Positive
7	$\overline{PDN}$	I Pullup	Powerdown Input. $\overline{PDN}$ = 1 Normal Operation $\overline{PDN}$ = 0 Powerdown
8	REXT	--	Transmit current set. An external resistor connected between this pin and GND will set the output current supplied on TPO+, TPO–.
9	$\overline{LINK}$	I/O Pullup	Link Status output and Link Disable input. This pin consists of an open drain output transistor with a resistor pullup. To disable the link test function, tie the pin to GND. Otherwise, the pin is a Link Detect output, can drive an LED, and blinks when asserted $\overline{LINK}$ = 1 Output Link Pulse Not detected $\overline{LINK}$ = 0 Output Link Pulse Detected $\overline{LINK}$ = GND Input Disable Link Pulse
10	$\overline{TLED}$	O	Transmit Activity output or combined Transmit/Receive Activity output. Actual pin definition depends on $\overline{RLED}$. This pin is capable of driving an LED and blinks when asserted. If $\overline{RLED}$ = Receive Activity Output $\overline{TLED}$ = 1 TP Xmt Idle $\overline{TLED}$ = 0 TP Xmt Active If $\overline{RLED}$ = GND $\overline{TLED}$ = 1 TP Xmt/Rcv Idle $\overline{TLED}$ = 0 TP Xmt/Rcv Active
11	$\overline{RLED}$/ $\overline{STP}$	I/O Pullup	Receive activity output and STP mode input. This pin consists of an open drain output transistor with a resistor pullup. To select the 150 ohm cable option (STP), tie the pin to GND. Otherwise, the pin is a Receive Activity output, can drive an LED, and blinks when asserted. $\overline{RLED}$ = 1 Output No Receive Activity $\overline{RLED}$ = 0 Output Receive Active RLED = GND Input STP Mode Enabled

Pin Description *(continued)*

Pin	Pin Name	I/O	Description
12	GND_1	--	Negative Power Supply. 0 volts.
13	TEST1	I Pulldown	Test Mode Select input. There are two possible test modes, depending on $\overline{SQE}$. TEST1 = 1 Full Duplex Test Mode Enabled ($\overline{SQE}$ = 0) TEST1 = 1 Loopback Test Mode Enabled ($\overline{SQE}$ = 1) TEST1 = 0 Normal Operating Mode
14	TPO–	O	Twisted Pair Transmit Output, Negative
15	TPO+	O	Twisted Pair Transmit Output, Positive
16	$\overline{SQE}$	I Pullup	SQE Test Enable input. $\overline{SQE}$ = 1 SQE Test Off $\overline{SQE}$ = 0 SQE Test On
17	V_{CC1}	--	Positive Supply. +5 volts.
18	LONG	I Pulldown	Long Cable Select input. When this pin is asserted, the receive thresholds are lowered below by approximately 4.5db. LONG = 1 Long Cable Mode Selected LONG = 0 Normal Operation
19	$\overline{CLED}$	O	Collision Status output. This pin is capable of driving an LED and blinks when asserted. $\overline{CLED}$ = 1 No Collision $\overline{CLED}$ = 0 Collision Occurring
20	$\overline{APX}$	I/O Pullup	Reverse Polarity Detect output and Autopolarity Disable input. This pin consists of an open drain output transistor with a resistor pullup. To disable the Autopolarity function, tie this pin to GND. Otherwise, this pin is a Receive Polarity output and can drive an LED. $\overline{APX}$ = 1 Output Receive Polarity Correct $\overline{APX}$ = 0 Output Receive Polarity Incorrect $\overline{APX}$ = GND Input Disable Autopolarity
21	$\overline{FDPLX}$	I	Full Duplex Enable input. To force the device into the Full Duplex Mode, tie this pin to GND. $\overline{FDPLX}$ = GND Input Full Duplex Mode Enabled

Pin Description *(continued)*

Pin	Pin Name	I/O	Description
22	OSCIN	I	Clock oscillator input. There must be either a 20MHZ crystal or a 20MHZ clock tied between this pin and GND.
23	TEST2	I Pulldown	Test input. Reserved for factory test. Leave floating or tie to GND.
24	DO–	I	AUI Receive Input, Negative
25	DO+	I	AUI Receive Input, Positive
26	GND_2	--	Negative Supply. 0 volts.
27	CI–	O	AUI Collision Output, Negative
28	CI+	O	AUI Collision Output, Positive

Functional Description

General

The 83C95 has five main sections: AUI transmitter, AUI receiver, twisted pair transmitter, twisted pair receiver, and miscellaneous.

The AUI receiver receives incoming Manchester encoded data from the AUI cable and converts the data from AUI levels to internal digital levels.

The data then goes to the twisted pair transmitter. The TP transmitter is composed of special circuitry to remove excess jitter, a waveform generator to preshape the output, a filter to remove high frequency components, and an output driver to drive the 100 ohm twisted pair cable. In addition, the transmitter generates link pulses, start of idle pulses (SOI), and detects the jabber condition.

The twisted pair receiver receives incoming Manchester encoded data from the twisted pair cable, removes high frequency noise from the input, determines if the input signal is a valid packet, and then converts the data from twisted pair levels to internal digital levels. The twisted pair receiver also detects link pulses, detects start of idle (SOI) pulses, detects and corrects for reverse polarity on the twisted pair inputs, implements a squelch algorithm to reject invalid signals, and detects and enables full duplex operation.

The output of the twisted pair receiver then goes to the AUI transmitter. The AUI transmitter converts the internal digital signal levels to AUI levels and drives the 78 ohm AUI cable. There is a second AUI transmitter for collision signals.

The miscellaneous blocks are the crystal oscillator, collision detect circuitry, digital select inputs, and digital status outputs.

Each block plus the operating modes are described in more detail in the following sections. A block diagram of the 83C95 is shown in Figure 1.

Twisted Pair Transmitter

TP Transmit

The transmitter consists of a jitter attenuator, waveform generator, and line driver.

The jitter attenuator is designed to reduce the jitter that was present on the AUI receive input. The jitter attenuator reduces input jitter by approximately 0.2, that is, only 20% of the jitter that is present on the AUI input propagates to the twisted pair output. This block also synchronizes the AUI receiver data transitions to the waveform generator clock.

The purpose of the waveform generator is to preshape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a second order low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM addresses; the ROM addresses are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Section 14 and also shown in Figure 2.

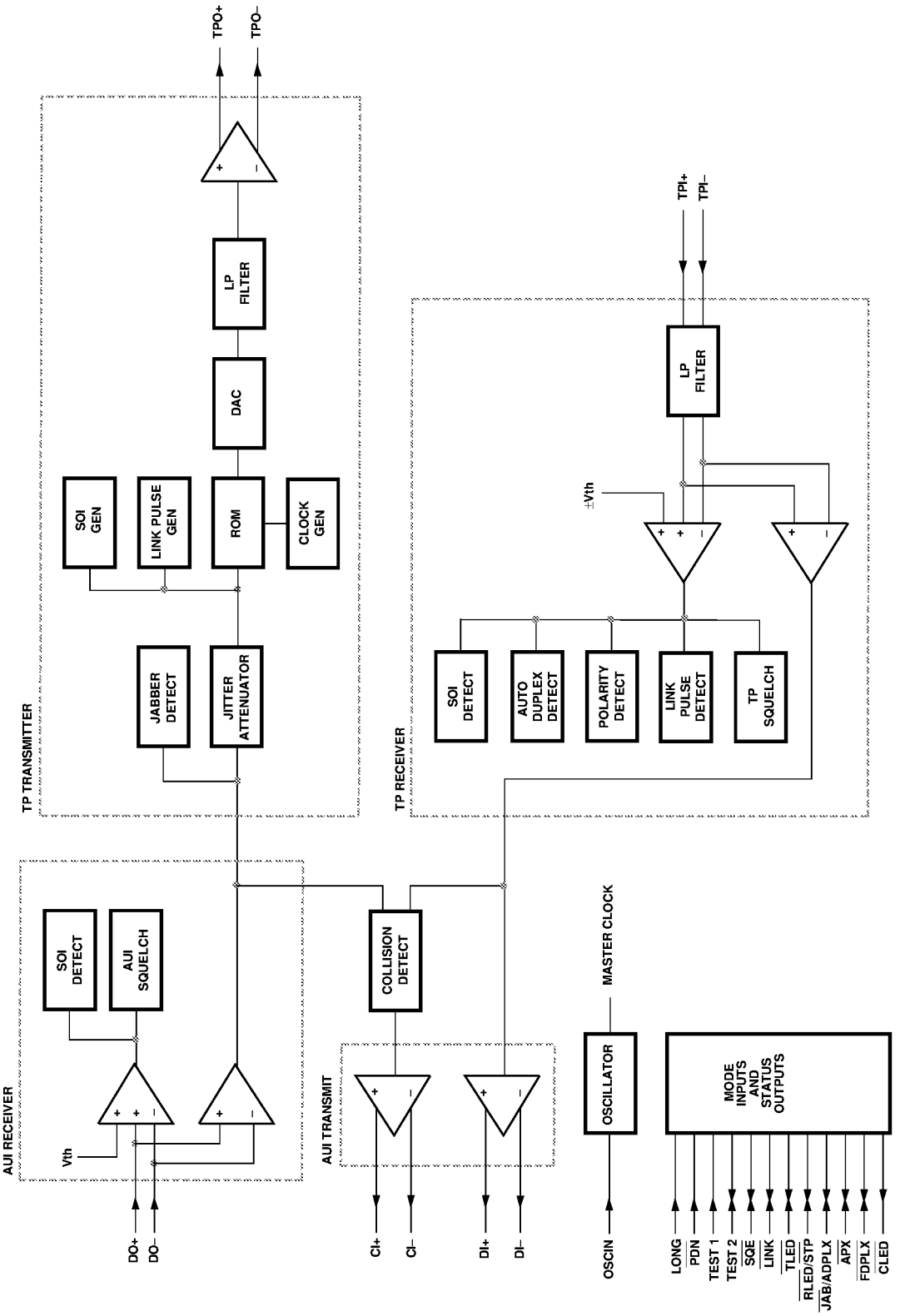


Figure 1. 83C95 Block Diagram

The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the preshaped and smoothed waveform to a current output that can drive the twisted pair cable directly without any external filters.

The 83C95 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications.

During the idle period, no output signal is transmitted on TPO± (except link pulse), but the current sources still remain active, thus eliminating glitches at the beginning and end of packet.

$\overline{\text{TLED}}$ is an output pin which indicates transmit activity or combined transmit/receive activity, depending on RLED. If $\overline{\text{RLED}}$ is used as a receive activity output, $\overline{\text{TLED}}$ is a transmit activity output. If $\overline{\text{RLED}}$ is configured as a STP mode select input, TLED is a combined transmit/receive activity output. This pin consists of an open drain output transistor with a resistor pullup. This pin can drive an LED from V_{CC} or it can drive another digital input. In order to make an LED visible when packets are being transmitted, the $\overline{\text{TLED}}$ output has an internal one shot that is triggered by the beginning of the packet. The period of the one shot is 100 ms, and at the end of the one shot pulse, the output transistor is kept off for another 100 ms. At the completion of the 100 ms off period, another 100 ms one shot pulse can be produced if a transmission is in progress.

STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 ohm cable, or shielded twisted pair cable. When STP mode is enabled, the output current is reduced the appropriate amount to keep the amplitude of the transmit signal unchanged from the specified transmit levels and template.

To place the device into the STP mode, the $\overline{\text{RLED}}/\overline{\text{STP}}$ pin must be tied to GND. This will enable STP mode and also reconfigure the $\overline{\text{TLED}}$ pin to a transmit or receive activity output (normallly $\overline{\text{TLED}}$ is a transmit activity output only).

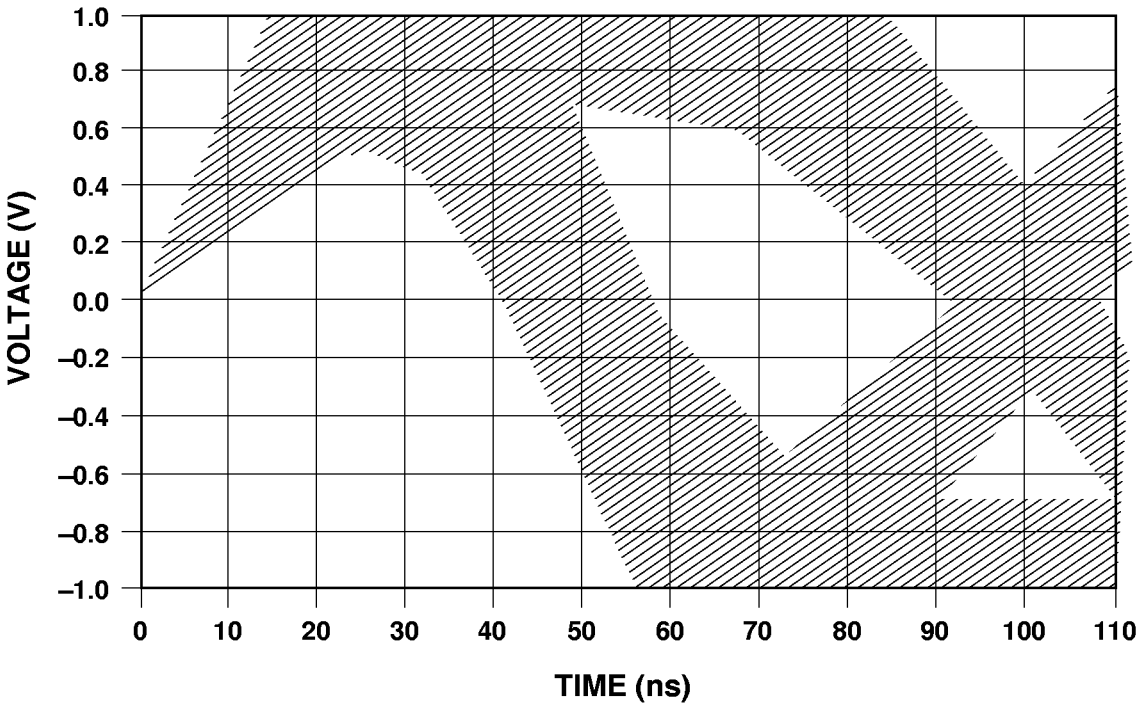


Figure 2. Twisted Pair Output Voltage Template with IEEE 802.3 Line Model.

TP Receiver

TP Receive

The TP receiver is intended to receive input signals from the twisted pair cable that reside inside the template shown in Figure 3.

The TPI± inputs are internally biased to $V_{cc}/3$ by internal 10K bias resistors. The TPI± inputs pass through a 3rd order low pass filter designed to eliminate high frequency noise on the input.

The receive filter output then goes to two different types of receive comparators, threshold and zero crossing. The threshold comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator is used for squelch, link pulse detect, SOI detect, reverse

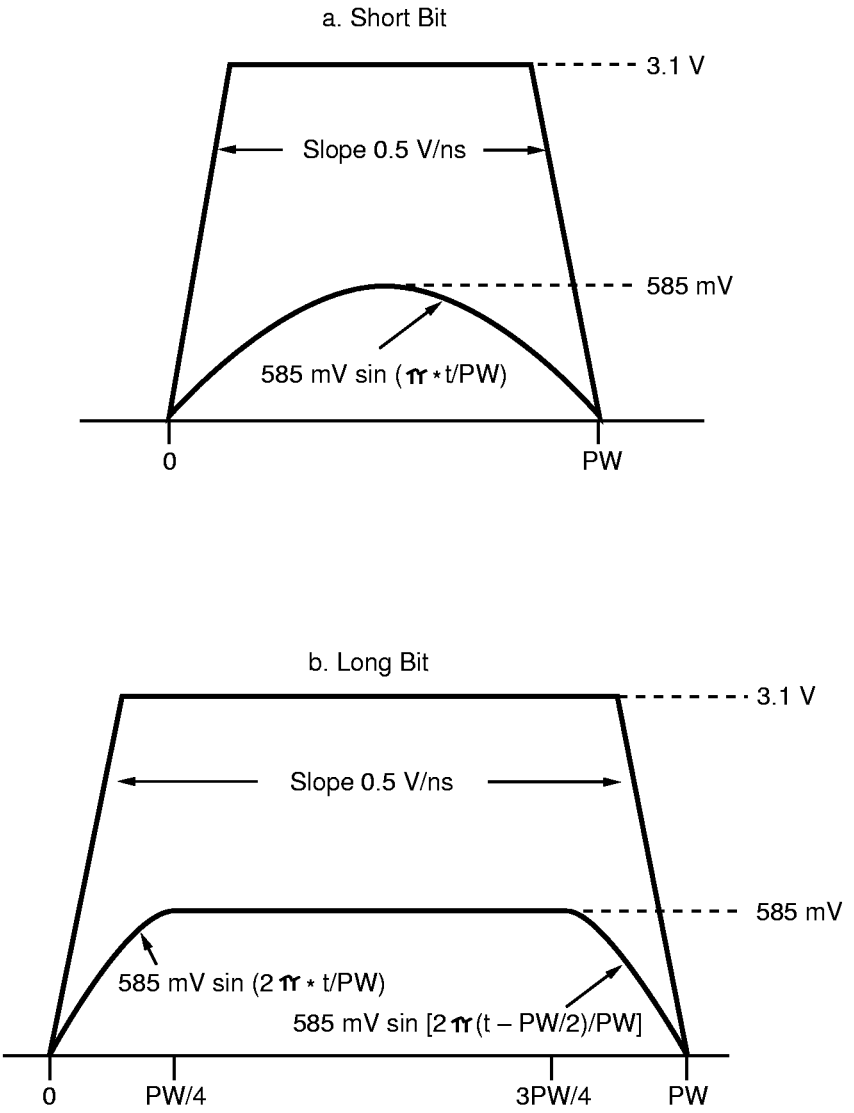


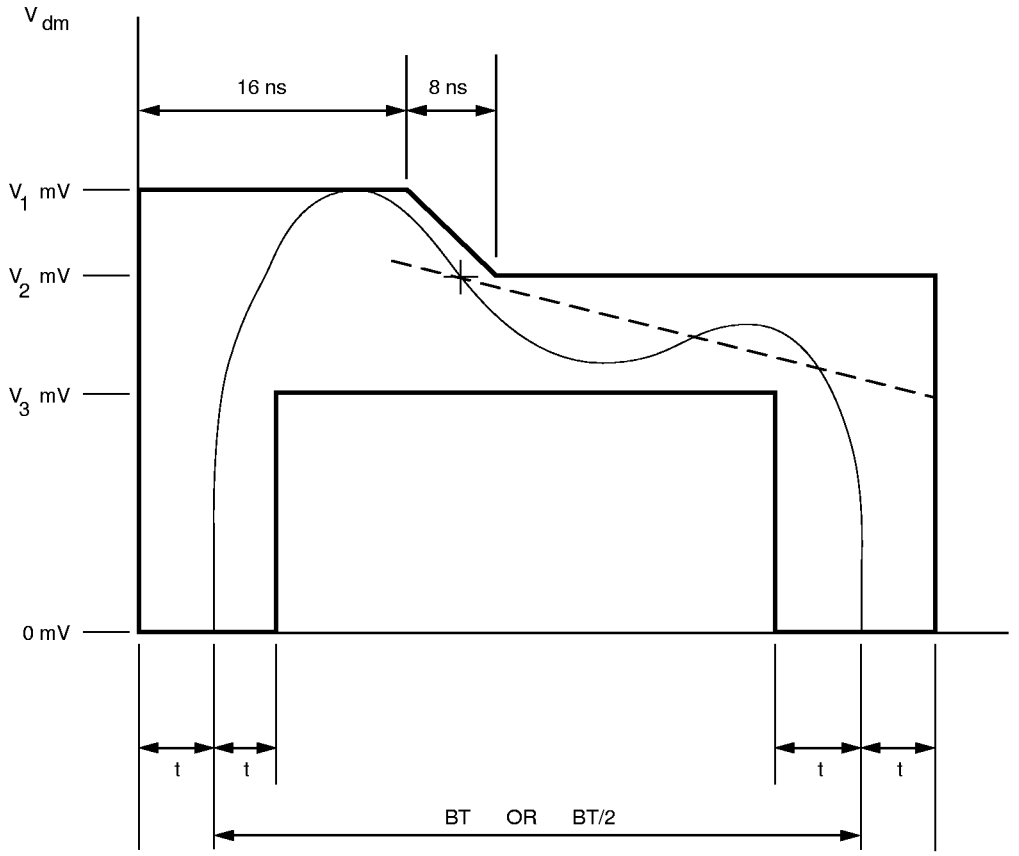
Figure 3. TP Receive Input Differential Voltage Template

polarity detect, and full duplex detect. Each of these are described in separate sections. The output of the zero crossing comparator goes to the AUI transmitter.

$\overline{RLED}$/$\overline{STP}$ is an input/output pin which can be configured to be either a receive activity output ($\overline{RLED}$) or a shielded twisted pair mode select input ($\overline{STP}$). This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and STP mode is selected for the transmitter. If the pin is not tied to GND, the pin is configured as an output and it is asserted low to indicate the occurrence of receive activity. This pin can drive an LED from V_{cc} or it can drive another digital input. In order to make an LED visible when packets are being received, the $\overline{RLED}$ output has an internal one shot that is triggered by the beginning of the packet. The period of the one shot is 100 ms, and at the end of the one shot pulse, the output transistor is turned off for 100 ms. At the completion of the 100 ms off period, another 100 ms one shot pulse is produced if a receive packet is in progress.

TP Squelch

The threshold comparator compares the TPI± inputs against fixed positive and negative thresholds, called squelch levels. The output from the threshold comparators goes to a receive squelch circuit which determines if the receive input data is valid. If the data is invalid, the



t = 2.5 ns

V_1 < 1315 mV, V_3 > 450 mV

$V_2 = 0.89\ V_1$

$V_3 = 0.82\ V_2$

Figure 4. AUI Transmit Voltage Template

receiver is in the squelched state. If the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 100 - 250 ns interval, the data is considered to be valid and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. While in the unsquelch state, the receive squelch circuit looks for SOI (Start Of Idle) pulse at the end of a packet. When the SOI signal is detected, the receive squelch is turned on again. The receiver meets the squelch requirements defined in IEEE 802.3 Section 14.

Long Cable Mode

The 83C95 can support cable lengths exceeding 100 meters by applying an active high to the LONG pin. When this pin is high, the threshold levels of the internal threshold comparators are lowered to accommodate an additional 4.5 dB of cable attenuation.

AUI Transmitter

The AUI transmitter is an output driver designed to drive a 78 ohm load to AUI levels. The outputs, DI+, are biased internally at approximately 2 volts.

The AUI output on DI± meets the transmit level and template requirements outlined in IEEE 802.3 Section 7 and shown in Figure 4.

There is a second AUI transmitter for collision. The collision AUI transmit output on CI± sends out a 10Mhz waveform whenever a collision occurs, per IEEE 802.3 Section 7.

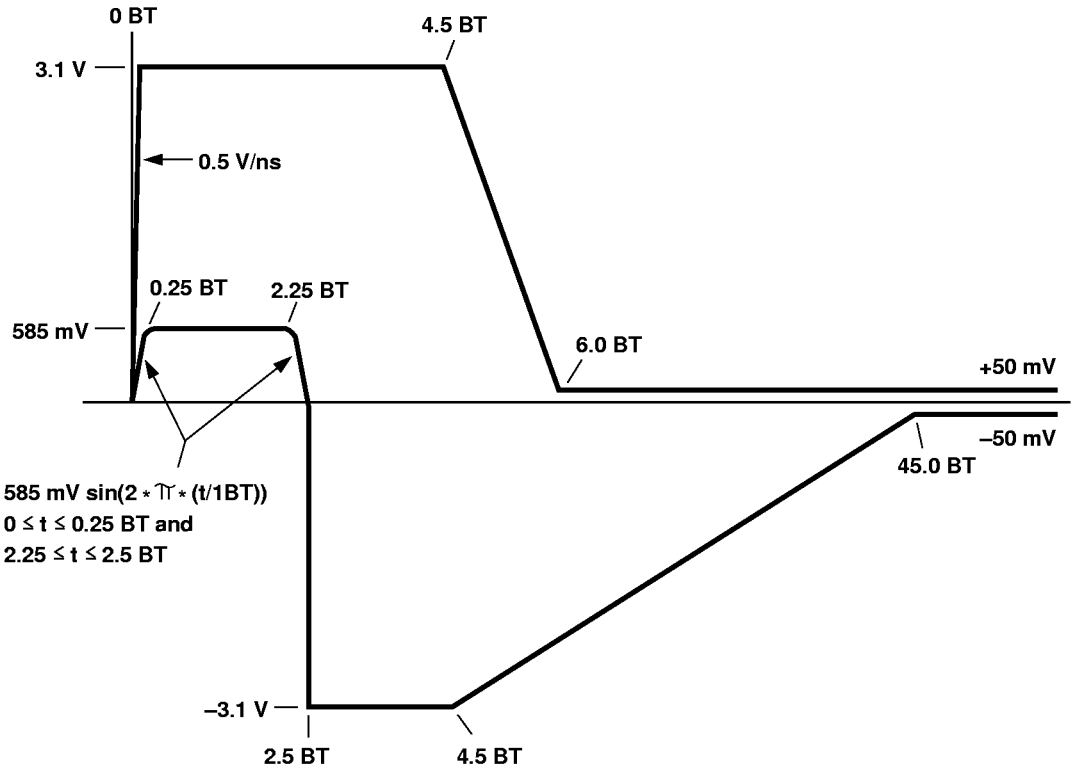


Figure 5. TP Transmit SOI Pulse Voltage Template

AUI Receiver

Receiver

The AUI receive inputs on DO± are internally biased to V_{cc}/2 by internal 10K bias resistors. The DO± inputs go to two different comparators, threshold and zero crossing. The threshold comparator output determines when the input is valid data, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator goes to the squelch circuit. The output of the zero crossing comparator goes to the TP transmitter.

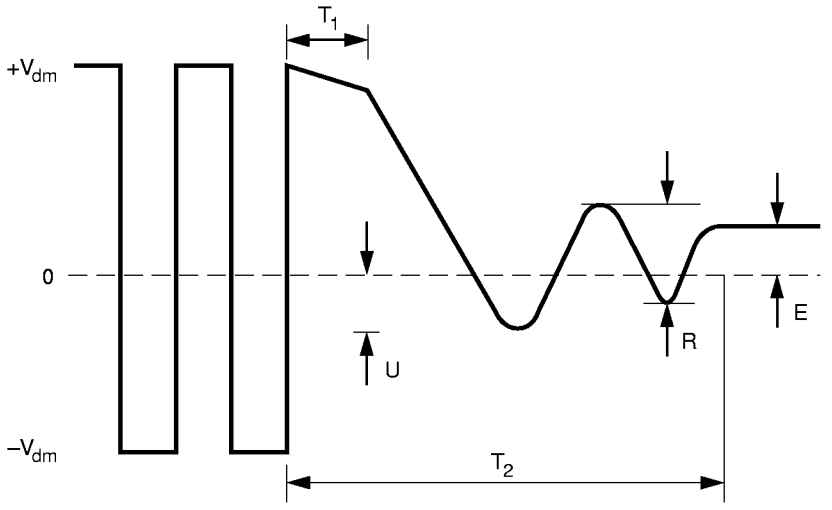
AUI Squelch

The threshold comparator compares the DO± inputs against a fixed negative threshold, called the AUI squelch level. The output from the threshold comparator goes to a receive AUI squelch circuit which determines if the receive AUI input data is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the negative squelch level for more than 20 ns, the data is considered to be valid and the AUI receiver now enters into the unsquelch state. In the unsquelch state, the AUI receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the AUI unsquelch level. While in the unsquelch state, the AUI receive squelch circuit looks for SOI (Start Of Idle) pulse at the end of a packet. When the SOI signal is detected, the receive squelch is turned on again. The AUI receiver meets all the AUI receive requirements specified in IEEE 802.3 Section 7.

SOI (Start of Idle)

The SOI pulse is a positive pulse inserted at the end of every transmitted packet to indicate the end of transmission and the start of idle.

Both the TP and AUI transmitters must generate SOI pulses. The TP transmitted SOI output pulse is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Section 14 and shown in Figure 5.



T_1 = 200 ns Minimum

T_2 = 8000 ns

U = –100 mV Maximum Undershoot

E = +/– 40 mV Max

R = <200 mV PK – PK

Figure 6 AUI Transmit SOI Pulse Voltage Template

The AUI transmit SOI output pulse meets the pulse template requirements specified in IEEE 802.3 Section 7 and shown in Figure 6.

The receiver detects the SOI pulse by sensing missing data transition. Once the SOI pulse is detected, the device goes into the idle state.

Link Integrity

The TP transmitter generates link pulses during idle to indicate that the network link is intact. The transmitted link pulses are single positive pulses sent out at 8-24 ms intervals and are preshaped by the transmit waveform generator to meet the pulse template specified in IEEE 802.3 Section 14 and shown in Figure 7.

The TP receiver monitors the TPI± pins continuously for valid data and link pulse activity. If neither data nor link pulses are detected, the 83C95 enters the Link Fail State, the TP transmit, AUI transmit, and SQE functions are disabled, and collision signals are asserted. For the device to exit the Link Fail State, three consecutive link pulses or one valid data packet need to be detected on the TPI± inputs.

$\overline{LINK}$ is an input/output pin that can be configured to be either a link pulse detect output or a link pulse disable input. This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and the link pulse detect function is disabled. If the pin is not tied to GND, the pin is configured as an output and indicates that link pulses are being detected when it is driven low. This pin can drive an LED from V_{CC} or it can drive another digital input.

Collision

Collision occurs whenever transmit and receive occur simultaneously on TPO± outputs and TPI± inputs. Collision is indicated by transmitting a 10Mhz signal on the collision AUI outputs, DI±, and by asserting $\overline{CLED}$ low. The 10Mhz collision signal is also asserted on DI± when the jabber condition has been detected and when the SQE

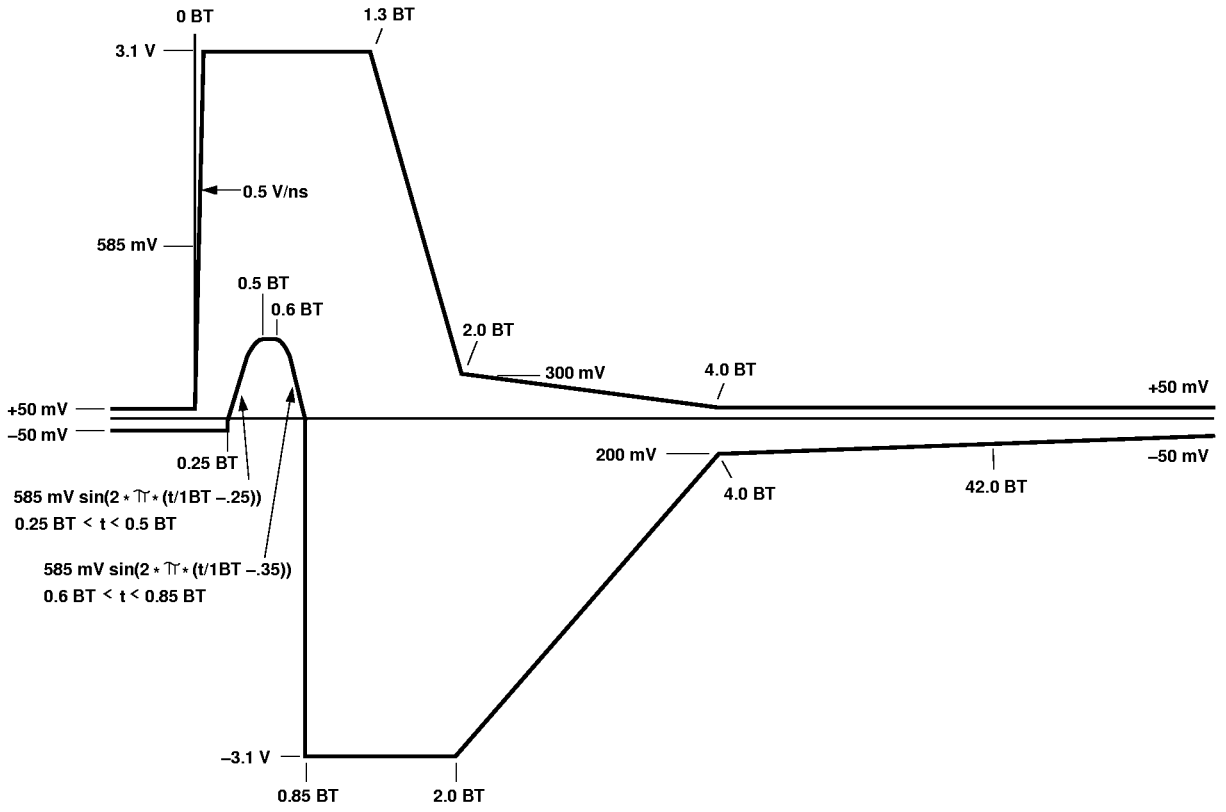


Figure 7. Transmit Link Pulse Voltage Template

test is performed. Collision function is disabled if the device is in the Link Fail State.

$\overline{CLED}$ is a collision status output. This pin consists of an open drain output transistor with a resistor pullup. This pin can drive an LED from V_{CC} or it can drive another digital input. In order to make an LED visible when collision is detected, the $\overline{CLED}$ output has an internal one shot that is triggered by the collision state. The period of the one shot is 100 ms, and at the end of the one shot pulse, the output transistor is turned off for another 100 ms. At the completion of the 100 ms off period, another 100 ms one shot pulse is produced if collision is still detected.

Signal Quality Error (SQE)

The 83C95 tests the AUI connection by sending out a 1 µs collision burst on the collision outputs, CI± , after each transmit packet. This is known as the signal quality error (SQE) test.

The SQE test is disabled when the device is in the Link Fail state or when jabber is detected. SQE test can also be manually disabled by tying the $\overline{SQE}$ pin high.

Jabber

Jabber condition occurs when the transmit packet exceeds its maximum allowable length. When jabber is detected, the transmit outputs on TPO± are forced to the idle state, collision is asserted, and $\overline{JAB}$ is asserted.

$\overline{JAB}/\overline{ADPLX}$ is an input/output pin which can be configured to be either a jabber detect output or an AutoDUPLEX mode enable input. This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and the AutoDUPLEX function is enabled (see Full Duplex section for details). If the pin is not tied to GND, the pin is configured as an output and indicates that jabber has been detected when driven low. This pin can drive an LED from V_{CC} or it can drive another digital input.

Jabber detection can be disabled by tying the TEST2 pin high.

Receive Polarity Correction

The polarity of the signal on the receive input twisted pair pins , TPI±, is continuously monitored. If the polarity is reversed, the device either indicates reverse polarity or automatically corrects for it internally (autopolarity function), depending on how $\overline{APX}$ is configured. If the autopolarity function is enabled, the polarity is initially assumed to be correct and no polarity correction occurs. If either 3 consecutive SOI or 3 consecutive link pulses indicate incorrect polarity on TPI±, the polarity is automatically corrected internally.

$\overline{APX}$ is an input/output pin which can be configured to be either a reverse polarity detect output or an autopolarity disable input. This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and the autopolarity function is disabled. If the pin is not tied to GND, the pin is configured as an output, and it indicates that the polarity is reversed and internally corrected when it is driven low. This pin can drive an LED from V_{CC} or it can drive another digital input.

Test Modes

There are three test modes on the 83C95: full duplex, loopback, and diagnostic.

The first two test modes are full duplex and loopback, and they are enabled when TEST1 is high and are selected by $\overline{SQE}$ according to Table 1. Both test modes connect various inputs and outputs together as described in Table 1.

Table 1. Test Mode Description

TEST1	$\overline{SQE}$	Test Mode	Function
0	x	--	Normal operation
1	0	Full Duplex	DO± = TPO± TPI± = DI±
1	1	Loopback	TPI± = TPO± DO± = DI±

During either full duplex or loopback test mode, the collision detection function is disabled, SQE function is disabled, receiver is forced into link pass state, and $\overline{CLED}$ will be driven low during transmit packet or link pulse transmission activity.

The third test mode, TEST2, is the diagnostic test mode and is reserved for factory use only. Tie TEST2 low or leave floating.

Full Duplex Mode

The 83C95 can be configured for full duplex mode. When the device is in the full duplex mode, transmission and reception can occur simultaneously because collision is disabled, internal loopback is disabled, and SQE pulse is disabled.

The device can either be forced into the full duplex mode, or it can detect and place itself into full duplex mode automatically (AutoDUPLEX mode).

Forced full duplex mode is enabled by tying $\overline{FDPLX}$ low.

The AutoDUPLEX mode is enabled by tying $\overline{JAB}/\overline{ADPLX}$ low. When the device is in the AutoDUPLEX mode, the transmitter transmits a double link pulse (two link pulses spaced 5µs apart) every 16th link pulse. The receiver constantly looks for these double link pulses. If the double link pulses are detected by the receiver, the device places itself in the full duplex mode automatically. In this way, the 83C95 can select either full and half duplex without a hardwire jumper.

$\overline{FDPLX}$ is an input pin which can be used to enable a full duplex mode. If the pin is tied to GND, full duplex mode is enabled.

$\overline{JAB}/\overline{ADPLX}$ is an input/output pin which can be configured to be either a jabber detect output or an AutoDUPLEX mode enable input. This pin consists of an open drain output transistor with a resistor pullup. If the pin is tied to GND, the pin is configured as an input and the AutoDUPLEX function is enabled. If the pin is not tied to GND, the pin is configured as an output, and it indicates that jabber has been detected (see Jabber section for more details). This pin can drive an LED from V_{cc} or it can drive another digital input.

Powerdown

The 83C95 can be powered down by tying $\overline{PDN}$ pin low. In powerdown mode, the outputs are tristated and the power consumption is reduced to less than 0.5 mW.

Oscillator

The 83C95 requires a 20Mhz reference frequency for internal signal generation. This 20Mhz reference frequency is generated by either connecting an external crystal or an external clock between OSCIN and GND.

APPLICATION INFORMATION

TP Transmit Interface

The interface between the TP outputs on TPO± and the twisted pair cable requires a transformer and two resistors as shown in Figures 8 and 9.

The transformer for the TP transmitter is a 2:1 CT type. Sources for the TP interface transformer are listed in Table 2.

Two external 200 ohm 1% resistors are needed between V_{cc} and TPO± to provide a 100 ohm termination impedance when looking back through the transmformer from the twisted pair cable. This is shown in Figures 8 and 9.

The 83C95 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emmissions requirements in most applications and have been eliminated from the application schematics in Figures 8 and 9.

To minimize noise pickup, the loading on TPO± should be minimized and both outputs should always be loaded equally.

TP Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with an external resistor as shown in Figures 8 and 9.

The receiver requires a 1:1 transformer. Sources for the TP interface transformer are listed in Table 2.

Table 2. TP Transformer Sources

Vendor	Part Number	Telephone
Valor	PT4152	(619) 537-2500
Coilcraft	Q4430-A	(708) 639-6400
PCA	EPE6047S	(818) 892-0761
Bel Hybrids and Magnetics	A-553-1084-01	(201) 432-0463
FEE Fil-Mag	23Z435	(619) 569-6577
NANO Pulse	000-6115-00	(714) 529-2600

The receive input needs to be terminated with 98 ohms in order to meet input impedance requirements of IEEE 802.3 Section 14. Notice that in Figures 8 and 9, the receive input has this input termination resistor broken up into two 48.7 ohm 1% resistors with a 0.1μF capacitor tied between the center points and GND. The optional 0.1 μF capacitor is needed if the device is required to meet the receive common mode input AC voltage specification in IEEE 802.3 Section 14. This capacitor attenuates common mode input noise. If the capacitor is not needed, then the two termination resistors can be combined into one 97.6 ohm 1% resistor across TPI±.

In order to minimize noise pickup into the receive path, loading on TPI± should be minimized and both inputs should be loaded equally.

TP Transmit Output Current Set

The TPO± output current level is set by an external resistor tied between REXT and GND. The output current is determined by the following equation where R is the value of REXT:

Iout = (R/10K) * 50mA

REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels.

The value of REXT should be ideally set to 10K to meet the templates and levels specified in Section 14 of IEEE 802.3. Since the output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of this resistor to compensate for the loading involved. For example, if the output loading is 10 pF, the value of the external resistor will have to be reduced to approximately 8.5K to meet the IEEE levels.

Keep REXT as close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

AUI Transmitter Interface

The AUI transmitter is a voltage driver that can drive a 78 ohm load. The outputs on DI± can be either transformer or capacitively coupled.

If the 83C95 is used in external MAU applications, transformer coupled outputs are recommended as shown in Figure 8. Any standard AUI transformer will be appropriate for this application.

If the 83C95 is used in embedded applications, the AUI outputs of the 83C95 can be capacitively coupled if desired as shown in Figure 9.

To minimize noise pickup, the loading on DI± should be minimized and both outputs should always be loaded equally.

AUI Receive Interface

The AUI receive inputs on DO± can be either transformer or capacitively coupled.

If the 83C95 is used in external MAU applications, it is recommended that the inputs be transformer coupled, as shown in Figure 8. Any standard AUI transmformer will be appropriate for this application. The inputs on DO± must be terminated with a 78.7 ohm 1% resistor in order to meet IEEE 802.3 receive termination requirements. If large common mode voltages can be encountered in a system, it can be attenuated by dividing the termination resistor into two series resistors and a 0.1 μf capacitor placed between the center point and GND.

If the 83C95 is used in imbedded applications, i.e. the interface between the 83C95 AUI port does not have an AUI cable, the inputs can be capacitively coupled if desired as shown in Figure 9. Here, no termination resistor is needed.

To minimize noise pickup, the loading on DO± should be minimized and both outputs should always be loaded equally.

Oscillator

The 83C95 requires a 20Mhz reference frequency for internal signal generation. This 20Mhz reference frequency can be generated by either connecting an external crystal or an external clock between OSCIN and GND.

If the crystal oscillator is used, it needs only an external crystal. No other external capacitors or other components are required. The crystal must have the characteristics shown in Table 3. The crystal must be placed as close as possible to OSCIN and GND, keeping parasitics to a minimum.

Table 3. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	20 Mhz +/- 0.01%
Equivelent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Max P_D	1 mW

Power Supply Decoupling

There are two V_{CC}'s on the 83C95 (V_{CC1} and V_{CC2}) and two GND's (GND_1 and GND_2).

V_{CC1} and V_{CC2} should be connected together as close as possible to the device with a large V_{CC} plane.

GND_1 and GND_2 should also be connected together as close as possible to the device with a large ground plane.

A 0.1 µF decoupling capacitor should be connected between V_{CC1} and GND_1 as close as possible to the device pins, preferably within 0.5". The same should be repeated for V_{CC2} and GND_2.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND_1, GND_2 unless otherwise specified.

V_{CC1}, V_{CC2} Supply Voltage ..... –0.3V to 7V
All Inputs and Outputs ..... –0.3V to V_{CC} + 0.3V
Input Latchup Current ..... ±25 mA
Package Power Dissipation ..... 1 Watt @ 25°C
Storage Temperature ..... –65 to +150°C
Operating Temperature ..... –65 to +125°C
Lead Temperature (Soldering, 10 Sec) ..... 250°C

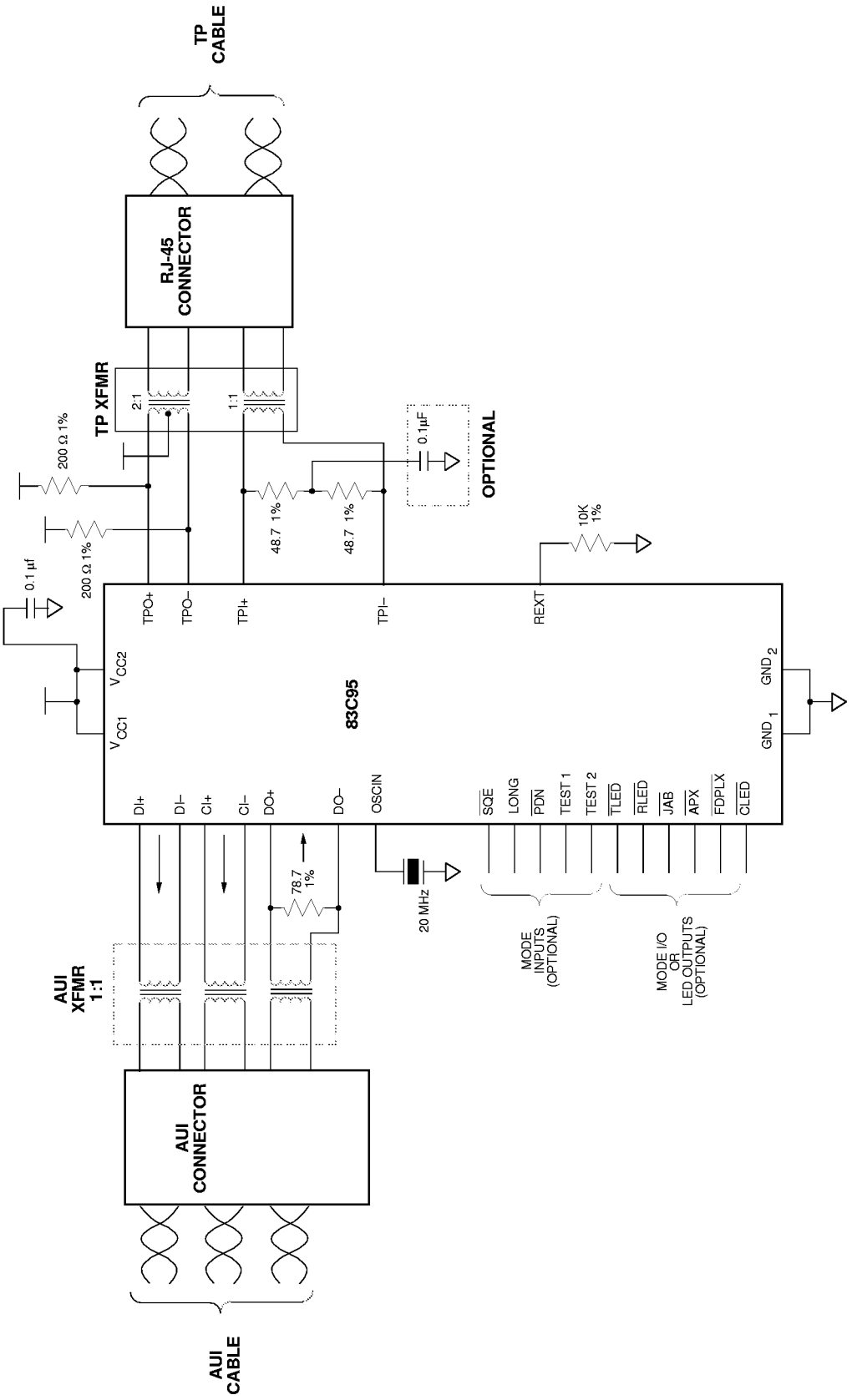


Figure 8. External MAU Schmatic Using 83C95

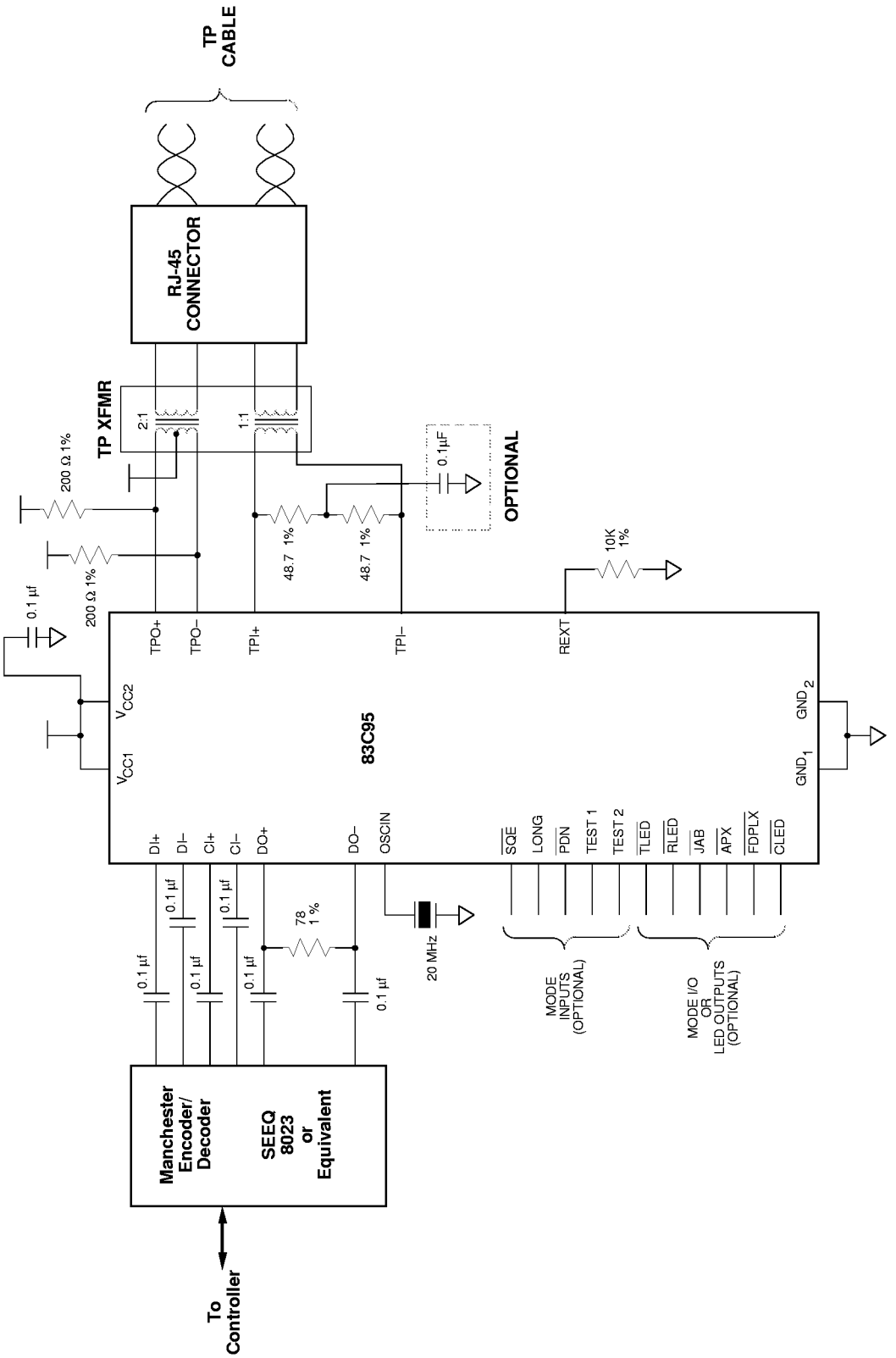


Figure 9. Internal MAU Schematic Using 83C95

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage			0.8	Volt	All Except OSCIN
				1.5	Volt	OSCIN
V_{IH}	Input High Voltage	2.0			Volt	All Except OSCIN
		3.5			Volt	OSCIN
I_{IL}	Input Low Current	–30		–120	µA	V_{IN} = GND $\overline{PDN}$, $\overline{SQE}$
		–15		–50	µA	V_{IN} = GND $\overline{JAB}$/$\overline{ADPLX}$, $\overline{LINK}$, $\overline{RLED}$/$\overline{STP}$, $\overline{APX}$, $\overline{FDPLX}$
				–300	µA	V_{IN} = GND OSCIN
I_{IH}	Input High Current	15		50	µA	V_{IN} = V_{CC} TEST1, TEST2, LONG
				300	µA	V_{IN} = V_{CC} OSCIN
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL} = –2 mA
				1.2	Volt	I_{OL} = –10 mA, $\overline{TLED}$, $\overline{RLED}$, $\overline{LINK}$ $\overline{JAB}$/$\overline{ADPLX}$, $\overline{FDPLX}$, $\overline{APX}$, $\overline{CLED}$
V_{OH}	Output High Voltage	4.0			Volt	I_{OL} = 8 µA $\overline{TLED}$, $\overline{CLED}$
		2.4			Volt	I_{OL} = 15 µA $\overline{JAB}$/$\overline{ADPLX}$, $\overline{LINK}$, $\overline{RLED}$/$\overline{STP}$, $\overline{APX}$, $\overline{FDPLX}$
C_{IN}	Input Capacitance		5		pF	
I_{CC}	V_{CC} Supply Current			190	mA	Transmitting
				0.1	mA	$\overline{PDN}$ = 0

TWISTED PAIR CHARACTERISTICS TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 50 OHM LOAD FROM TPO± TO V_{CC}

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
T_{OV}	TPO± Differential Output Voltage	2.2	2.5	2.8	V pk	
T_{OVT}	TPO± Differential Output Voltage Template	See Figure 2				
T_{SOI}	TPO± SOI Output Voltage Template	See Figure 5				
T_{LPT}	TPO± Link Pulse Output Voltage Template	See Figure 7				
T_{OIV}	TPO± Differential Output Idle Voltage			± 50	mV	Measured on Secondary Side of XFMR on Figure 8.
T_{OIA}	TPO± Output Current	44	50	56	mA pk	
		29	33	37	mA pk	STP Cable Mode
T_{OIR}	TPO± Output Current Adjustment Range	30	50	80	mA pk	V_{CC} = 5V, Adjustable with REXT
T_{CMA}	TPO± Common Mode AC Output Voltage		10	25	mV pk	
T_{HD}	TPO± Harmonic Distortion			–27	dB	All 1's Output
T_{OR}	TPO± Output Resistance		10 K		Ohm	
T_{OC}	TPO± Output Capacitance		15		pF	

TWISTED PAIR CHARACTERISTICS RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 10 MHz sinewave on TPI±

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
R_{ST}	TPI± Squelch Threshold	310		540	mV pk	LONG = 0
		190		330	mV pk	LONG = 1
R_{UT}	TPI± Unsquelch Threshold	190		330	mV pk	LONG = 0
		115		200	mV pk	LONG = 1
R_{ZT}	TPI± Zero Cross Switching Threshold			±20	mV pk	
R_{OCV}	TPI± Input Open Circuit Voltage	$V_{CC}/3$ –0.25	$V_{CC}/3$	$V_{CC}/3$ +0.25	Volt	
R_{CMR}	TPI± Input Common Mode Voltage Range	$V_{CC}/3$ –1.0		$V_{CC}/3$ +1.0	Volt	
R_{DR}	TPI± Input Differential Voltage Range	GND		V_{CC}	Volt	
R_{CRR}	TPI± Input Common Mode Rejection Ratio			–20	dB	0 – 10 Mhz
R_{IR}	TPI± Input Resistance	5K			ohm	
R_{IC}	TPI± Input Capacitance		10		pF	

AUI CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 78 ohm, 27 µH load on DI±, CI±

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
A_{OV}	DI±/CI± Differential Output Voltage	550		1200	mV pk	
A_{ORF}	DI±/CI± Output Rise And Fall Time			5	ns	t_R, t_F measured at 10 - 90% points
A_{OIV}	DI±/CI± Differential Output Idle Voltage			±40	mV	
A_{OVU}	DI±/CI± Differential Output Voltage Undershoot During Idle			–100	mV	
A_{OCD}	DI±/CI± Common Mode DC Output Voltage	V_{CC}/3.5	V_{CC}/3.0	V_{CC}/2.5	Volt	
A_{OCA}	DI±/CI± Common Mode AC Output Voltage			40	mV pk	
A_{OR}	DI±/CI± Output Resistance			75	ohm	
A_{OC}	DI±/CI± Output Capacitance		15		pF	

AUI CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 10 Mhz sinewave on DO±

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
A_{IST}	DO± Squelch Threshold	–175		–325	mV	
A_{IUT}	DO± Unsquelch Threshold	–100		–225	mV	
A_{IZT}	DO± Zero Cross Switching Threshold			20	mV pk	
A_{IOC}	DO± Input Open Circuit Voltage	$V_{CC}/2$ –0.25	$V_{CC}/2$	$V_{CC}/2$ +0.25	Volt	
A_{ICR}	DO± Input Common Mode Voltage Range	$V_{CC}/2$ –1.0		$V_{CC}/2$ +1.0	Volt	
A_{IVR}	DO± Input Voltage Range	GND		V_{CC}	Volt	
A_{ICR}	DO± Input Common Mode Rejection	20			dB	0 - 10MHZ
A_{IR}	DO± Input Resistance	5K	10K		ohm	
A_{IC}	DO± Input Capacitance		10		pF	

AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. Input conditions:
   - All Inputs: tr, tf ≤ 10 ns, 20 - 80%
6. Output Loading
   - TPO±: 50 Ohms To V_{CC} On Each Output, 10 pF
   - DI±, CI±: 78 Ohms Differentially, 10 pF
   - Open Drain Digital Outputs: 1K Pullup, 50 pF
   - All Other Digital Outputs: 50pF
7. Measurement Points:
   - TPO±, TPI±: 0v During Data, ±0.30V at start/end of packet
   - DI±, DO±, CI±: 0v During Data, ±0.45V at start/end of packet
   - All other inputs and outputs: 1.5 Volts

TRANSMIT TIMING CHARACTERISTICS

Refer To Figure 10 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	DO± To TPO± Bit Loss			2	BT	
t_2	DO± To TPO± Propagation Delay			200	ns	
t_3	DO± SOI Pulse Width Required For Idle Detection	150		200	ns	Measure DO± from last zero crossing to 0.45V point
t_4	TPO± SOI Pulse Width To 0.3V Point	225		325		See Figure 5. Measure TPO± from last zero crossing to 0.3V point
t_5	TPO± SOI Pulse Width To 50 mV Point			4500	ns	See Figure 5. Measure TPO± from last zero crossing to 50 mV point
t_6	TPO± Output Jitter			± 8	ns	
t_7	TPO± Active To $\overline{\text{TLED}}$ Assert Delay			300	ns	
t_8	$\overline{\text{TLED}}$ Assert Time	95		105	ms	
t_9	$\overline{\text{TLED}}$ Deassert Time	95		105	ms	

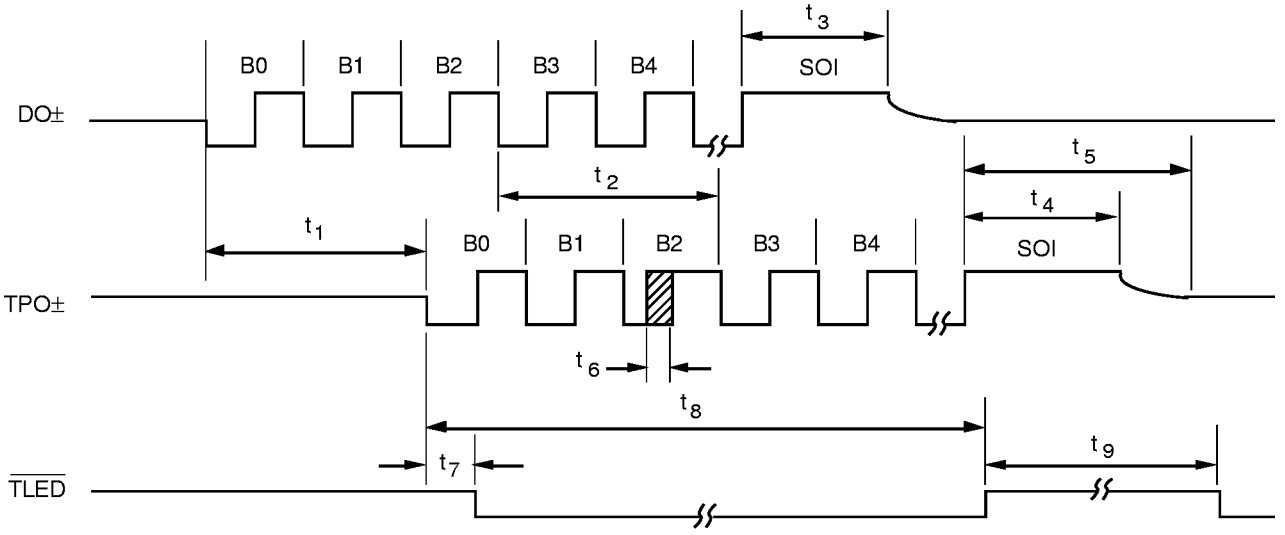


Figure 10. Transmit Section Timing

RECEIVE SECTION TIMING CHARACTERISTICS

Refer To Figure 11 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{21}	TPI± To DI± Bit Loss			5	BT	
t_{22}	TPI± to DI± Propagation Delay			200	ns	
t_{23}	TPI± SOI Pulse Width Required For Idle Detection	150		200	ns	Measure TPI± from last zero crossing to 0.3V Point
t_{24}	DI± SOI Pulse Width to 0.45V Point	225		325	ns	See Figure 6. Measure DI± from last zero crossing to 0.45V Point
t_{25}	DI± SOI Pulse Width to 40 mV Point			8000	ns	See Figure 6. Measure DI± from last zero crossing to 40 mV Point
t_{26}	DI± Output Jitter			± 1.5	ns	
t_{27}	TPI± Active To $\overline{\text{RLED}}$ Assert Delay			300	ns	
t_{28}	$\overline{\text{RLED}}$ Assert Time	95		105	ms	
t_{29}	$\overline{\text{RLED}}$ Deassert Time	95		105	ms	

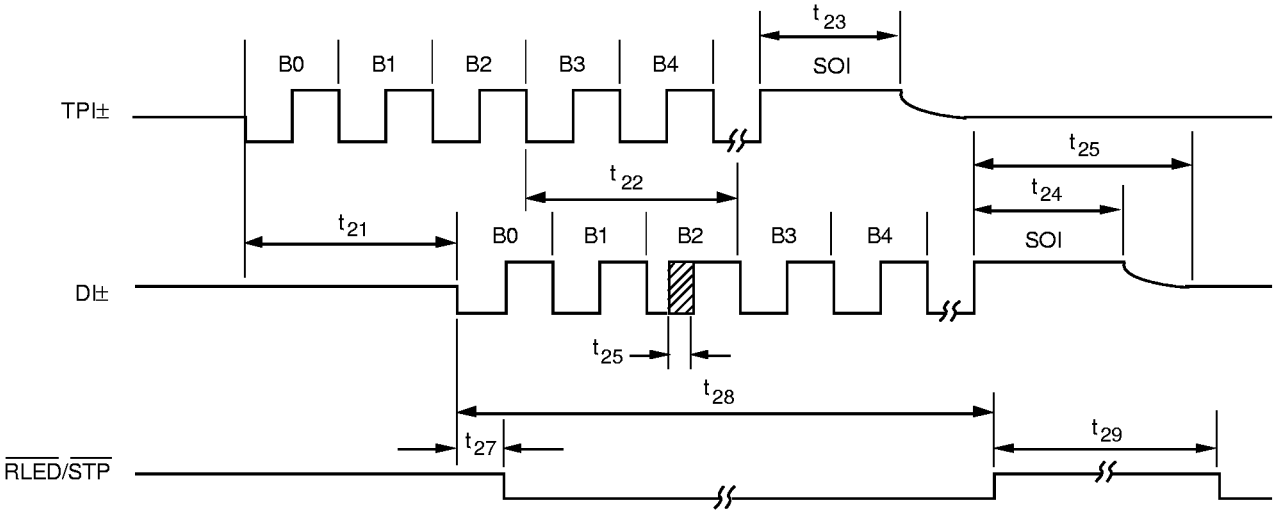


Figure 11. Receive Section Timing

COLLISION TIMING CHARACTERISTICS

Refer To Figure 12 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	Collision Start To CI± Assert Delay			600	ns	
t_{32}	Collision Start To $\overline{\text{CLED}}$ Assert Delay			600	ns	
t_{33}	Collision Start To End Of AUI Loopback On DI±			600	ns	
t_{34}	Collision Start To Start Of Receive Data On DI±			700	ns	
t_{35}	CI± Cycle Time	99.9	100	100.1	ns	
t_{36}	CI± Low Or High Time	45	50	55	ns	
t_{37}	Collision Stop To CI± Deassert			600	ns	
t_{38}	Collision Stop To $\overline{\text{CLED}}$ Deassert			600	ns	
t_{39}	Collision Stop To End Of Receive Data On DI±			600	ns	
t_{40}	Collision Stop To Start Of AUI Loopback On DI±			700	ns	
t_{41}	$\overline{\text{CLED}}$ Assert Time	95		105	ms	
t_{42}	$\overline{\text{CLED}}$ Deassert Time	95		105	ms	

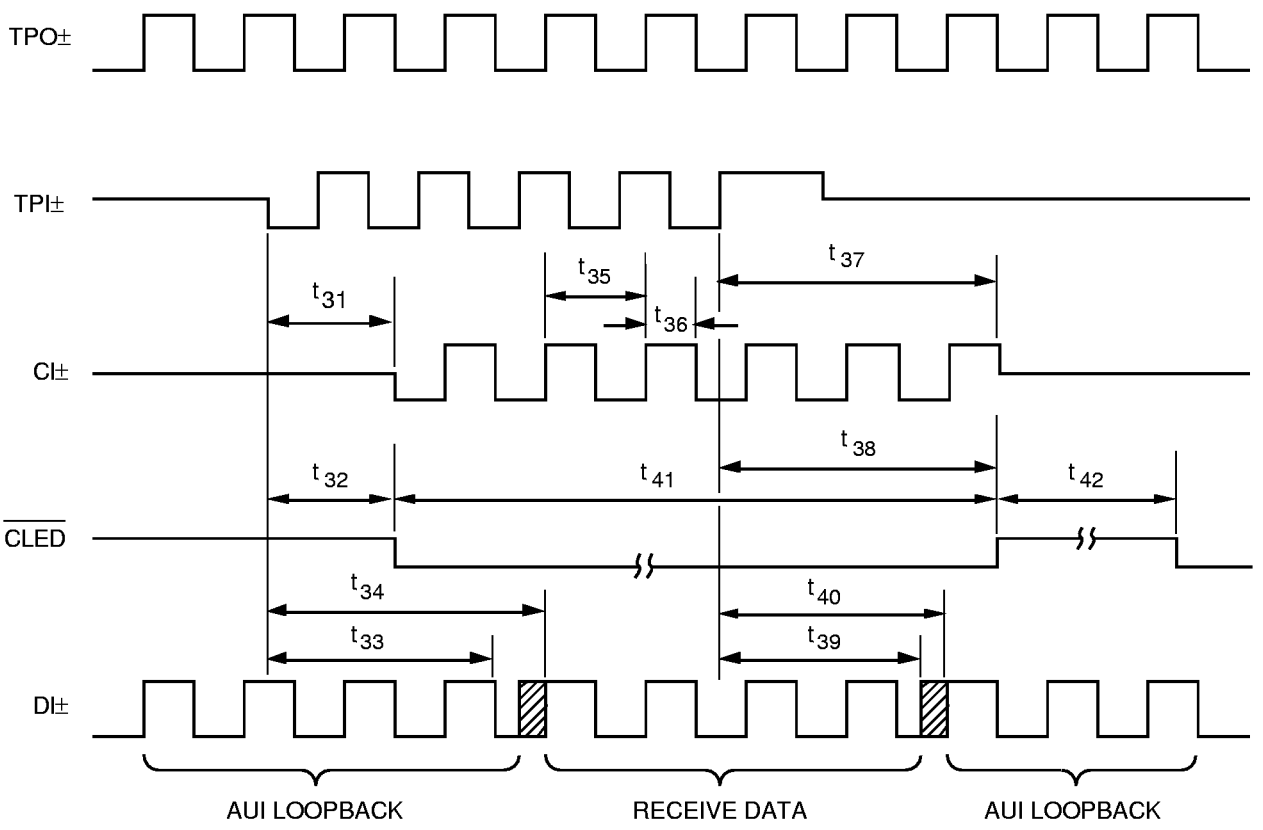


Figure 12. Collision Timing

SQE TIMING CHARACTERISTICS

Refer To Figure 13 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{51}	DO± SOI To CI± Assert Delay	0.8		1.2	µs	
t_{52}	CI± Assert Time	0.8		1.2	µs	
t_{53}	DO± SOI To $\overline{\text{CLED}}$ Assert Delay	0.8		1.2	µs	
t_{54}	$\overline{\text{CLED}}$ Assert Time	0.8		1.2	µs	

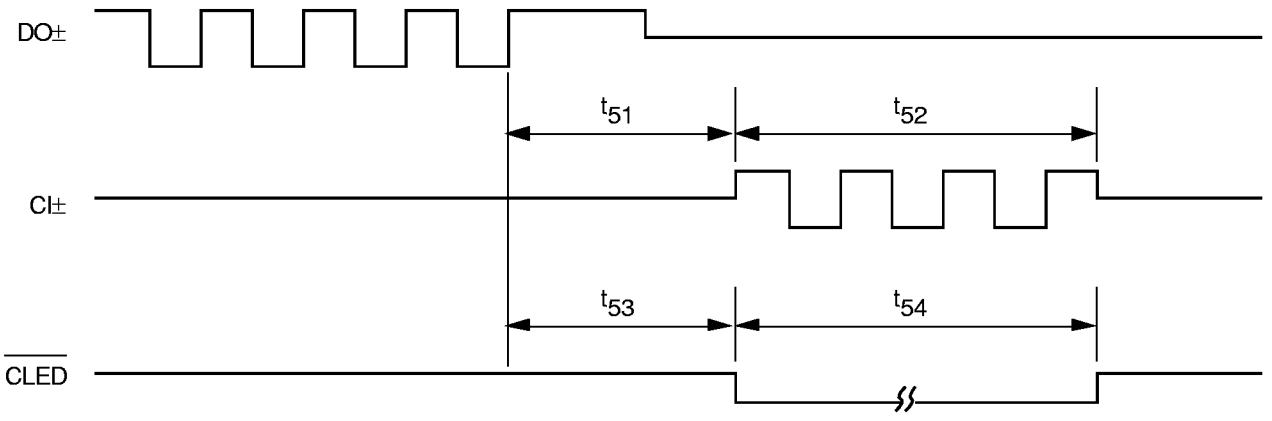


Figure 13. SQE Timing

LINK PULSE TIMING CHARACTERISTICS

Refer To Figure 14 For Timing Diagram

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{61}	Transmit Link Pulse Width	100		150	ns	See Figure 7
t_{62}	Transmit Link Pulse Period	8		24	ms	
t_{63}	Transmit Link Pulse To Double Link Pulse Spacing	5.0	5.2	5.4	µs	Full Duplex Mode
t_{64}	Transmit Double Link Pulse Interval Spacing	16		16	Link Pulses	Full Duplex Mode
t_{65}	Receive Link Pulse Width Required For Detection	50			ns	
t_{66}	Receive Link Pulse Minimum Period Required For Detection	2		7	ms	Link_Test_Min
t_{67}	Receive Link Pulse Maximum Period Required For Detection	50		150	ms	Link_Loss and Link_Test_Max
t_{68}	Receive Link Pulse To Double Link Pulse Spacing Required For Full Duplex Mode Detection	4.8		5.6	µs	Full Duplex Mode
t_{69}	Receive Double Link Pulse Minimum Period Required For Full Duplex Mode Detection	80		120	ms	Full Duplex Mode
t_{70}	Receive Double Link Pulse Maximum Period Required for Full Duplex Detection	380		420	ms	Full Duplex Mode
t_{71}	Receive Link Pulse Assert	2	3	10	Link Pulses	
t_{72}	Receive Full Duplex Assert Delay			7	µs	Full Duplex Mode Detection

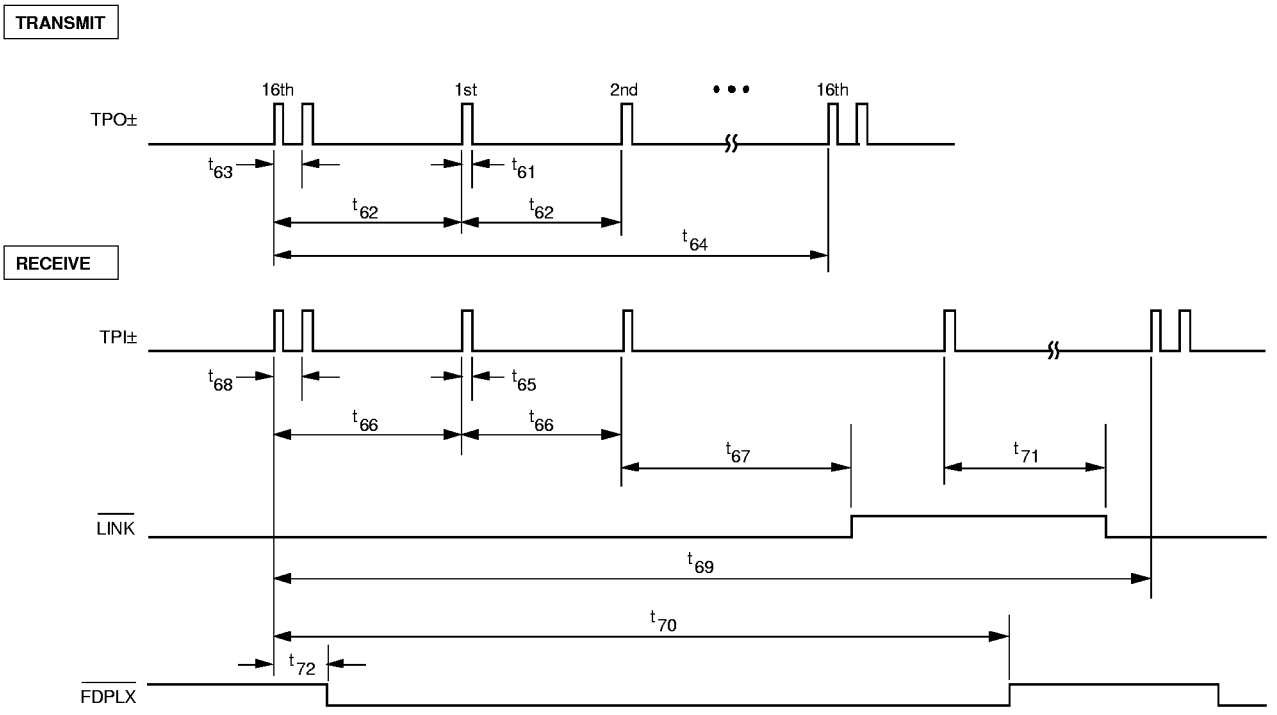


Figure 14. Link Pulse Timing

JABBER TIMING CHARACTERISTICS

Refer To Figure 15 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{81}	Jabber Activation Time	20		50	ms	
t_{82}	Jabber Deactivation Time	250		750	ms	

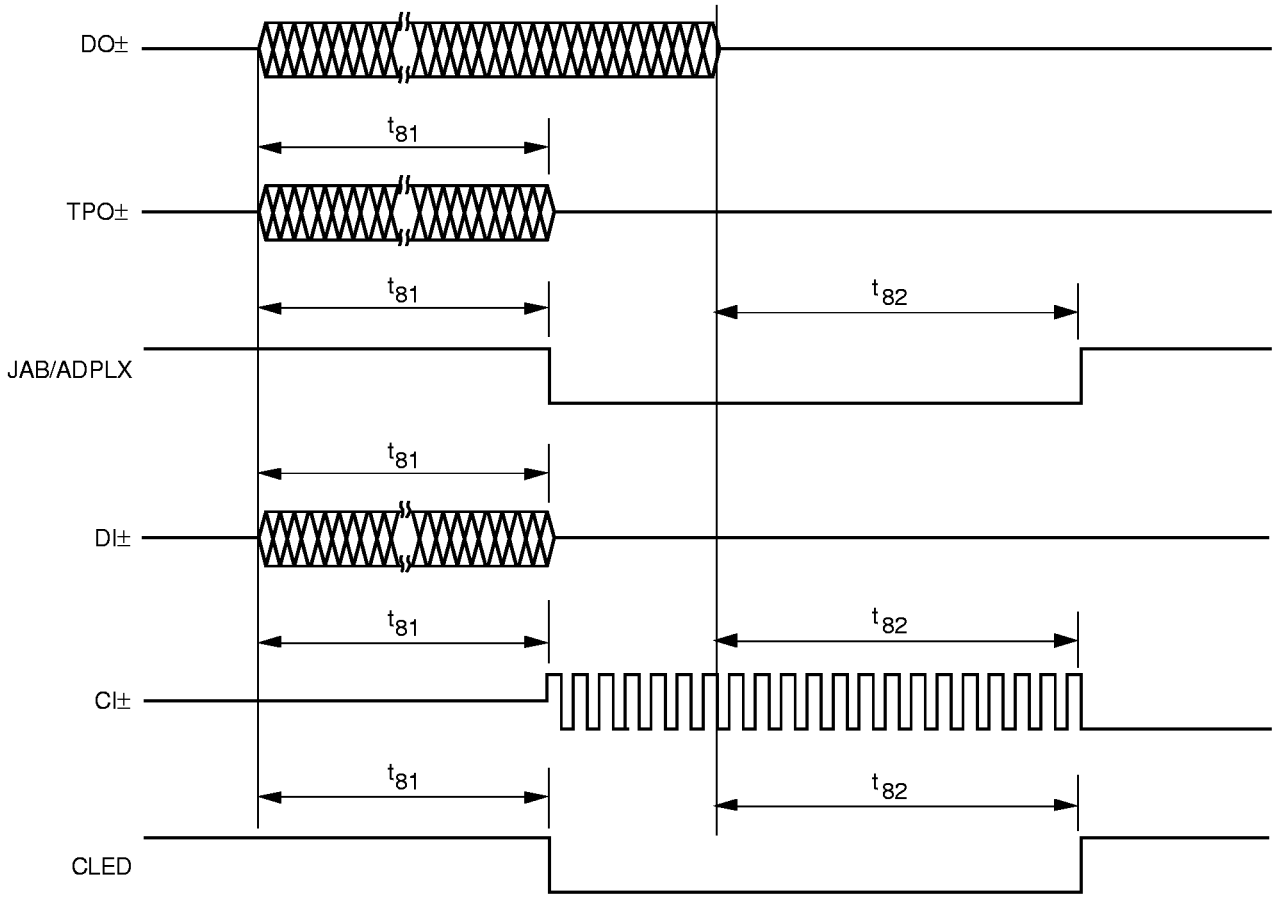
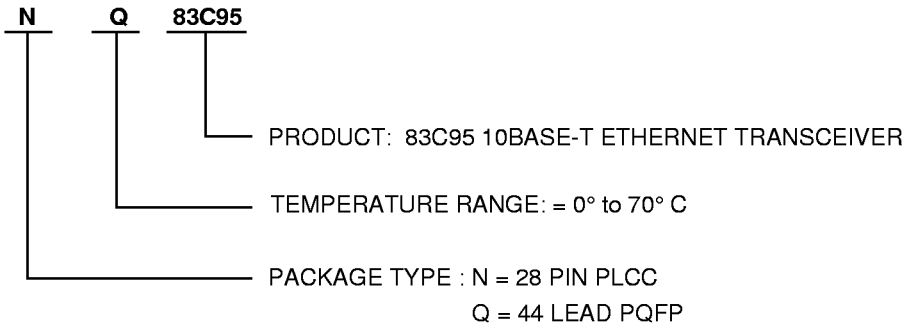


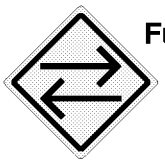
Figure 15. Jabber Timing

Ordering Information

PART NUMBER



SEEQ Full Duplex Designation



Full Duplex

Symbol indentifies product as a Full Duplex device.

Revision History

4/16/96

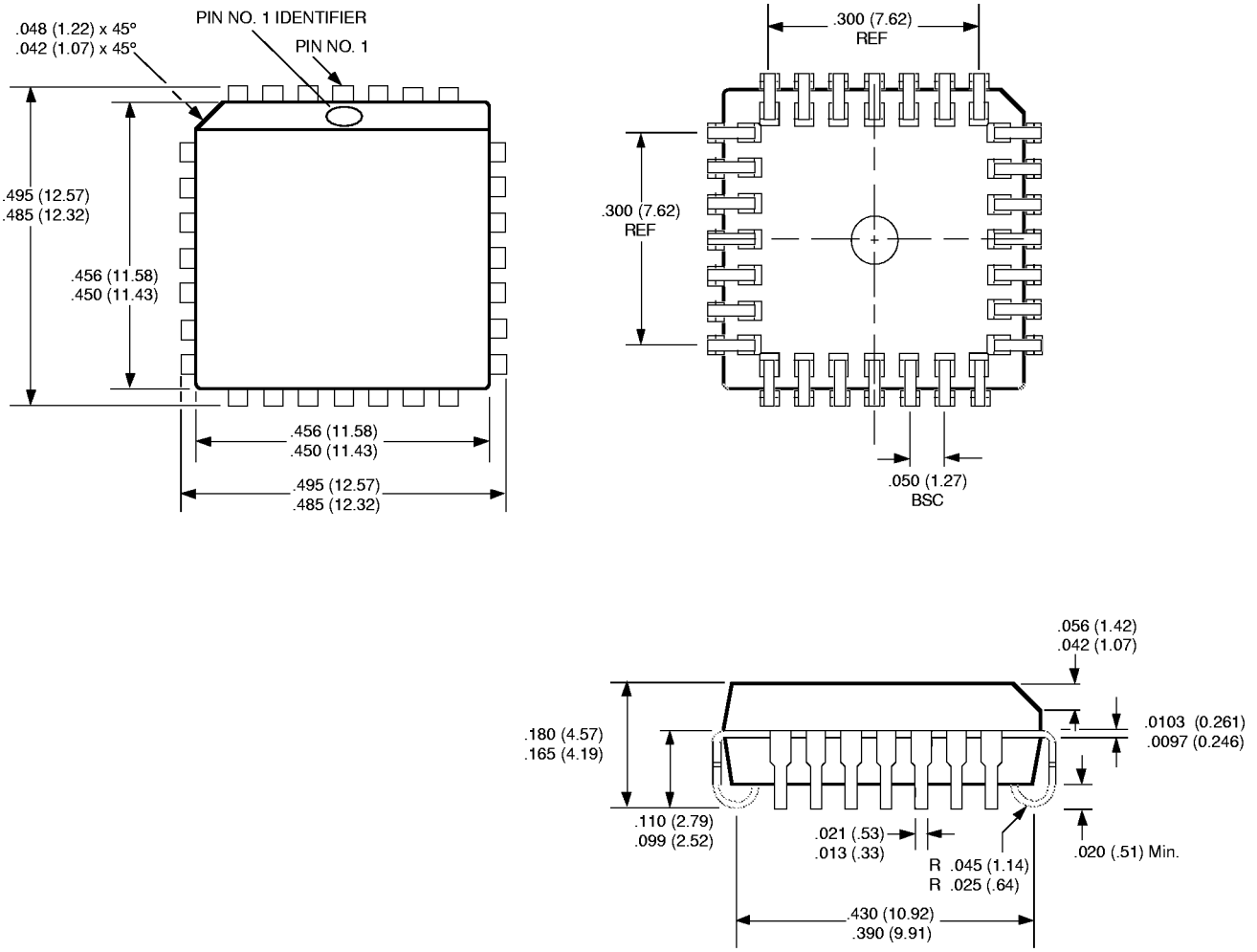
- All references to separate 'digital' and 'analog' power and grounds deleted.
- Page 3, Pin Description:
  - Pin 21(FDPLX) description corrected from I/O to input (only).
- Page 18, DC Electrical Characteristics:
  - I_{IL} (min) changed from -125 to -15 µA.
  - I_{IL} (max) changed from -500 to -50 µA.
  - I_{IL} (max) for GND and OSCIN changed from -150 to -300 µA.
  - I_{IH} (min) changed from 30 to 15 µA.
  - I_{IH} (max) changed from 120 to 50 µA.
  - I_{IH} (max) for OSCIN changed from 150 to 300 µA.
  - V_{OL} (max) changed from 0.8 to 1.2 V.
  - V_{OH} test conditions clarified.
- Page 21, AUI Characteristics
  - AOCD (min) corrected from V_{CC} -3.5 to V_{CC}/3.5.
  - AOCD (typ) corrected from V_{CC} -3.0 to V_{CC}/3.0.
  - AOCD (max) corrected from V_{CC} -2.5 to V_{CC}/2.5.

9/9/96

- Page 33, Dimension diagram has been added to this data sheet.

Surface Mount Packages

28-Pin Plastic Leaded Chip Carrier Type N



Notes

1. All dimensions are in inches and (millimeters).

2. Dimensions do not include mode flash. Maximum allowable flash is .008 (.20).

3. Formed leads shall be planar with respect to one another within 0.004 inches.