Four-Bit Bipolar Microprocessor Slice
2901A

PRELIMINARY DATA

Features/Benefits

- **Two-address architecture—**
  Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU—**
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data source selection—**
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- **Left/right shift independent of ALU—**
  Add and shift operations take only one cycle.
- **Four status flags—**
  Carry, overflow, zero, and negative.
- **Expandable—**
  Connect any number of 2901A's together for longer word lengths.
- **Microprogrammable—**
  Three groups of three bits each for source operand, ALU function, and destination control.

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2901ANC	N40	0°C to +70°C
2901AJC	J40	0°C to +70°C
2901AJM	J40	−55°C to +125°C
2901AFM	F42	−55°C to +125°C

Block Diagram

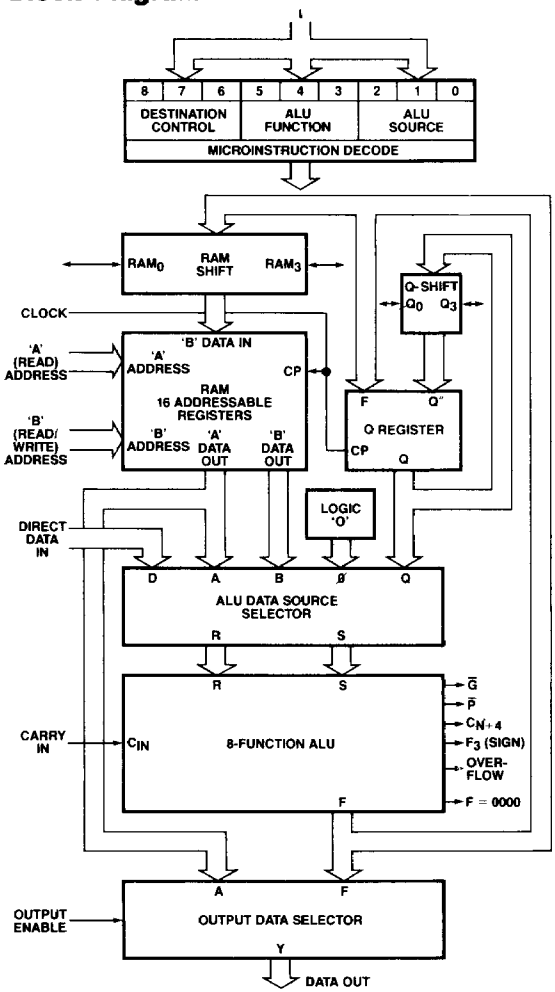


Figure 1. Microprocessor Slice Block Diagram

Description

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901A will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip. The 2901A is a plug in replacement for the 2901.

Architecture

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 2. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 2 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 2, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The 2901A microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the 2902 ('182). A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Table 3.

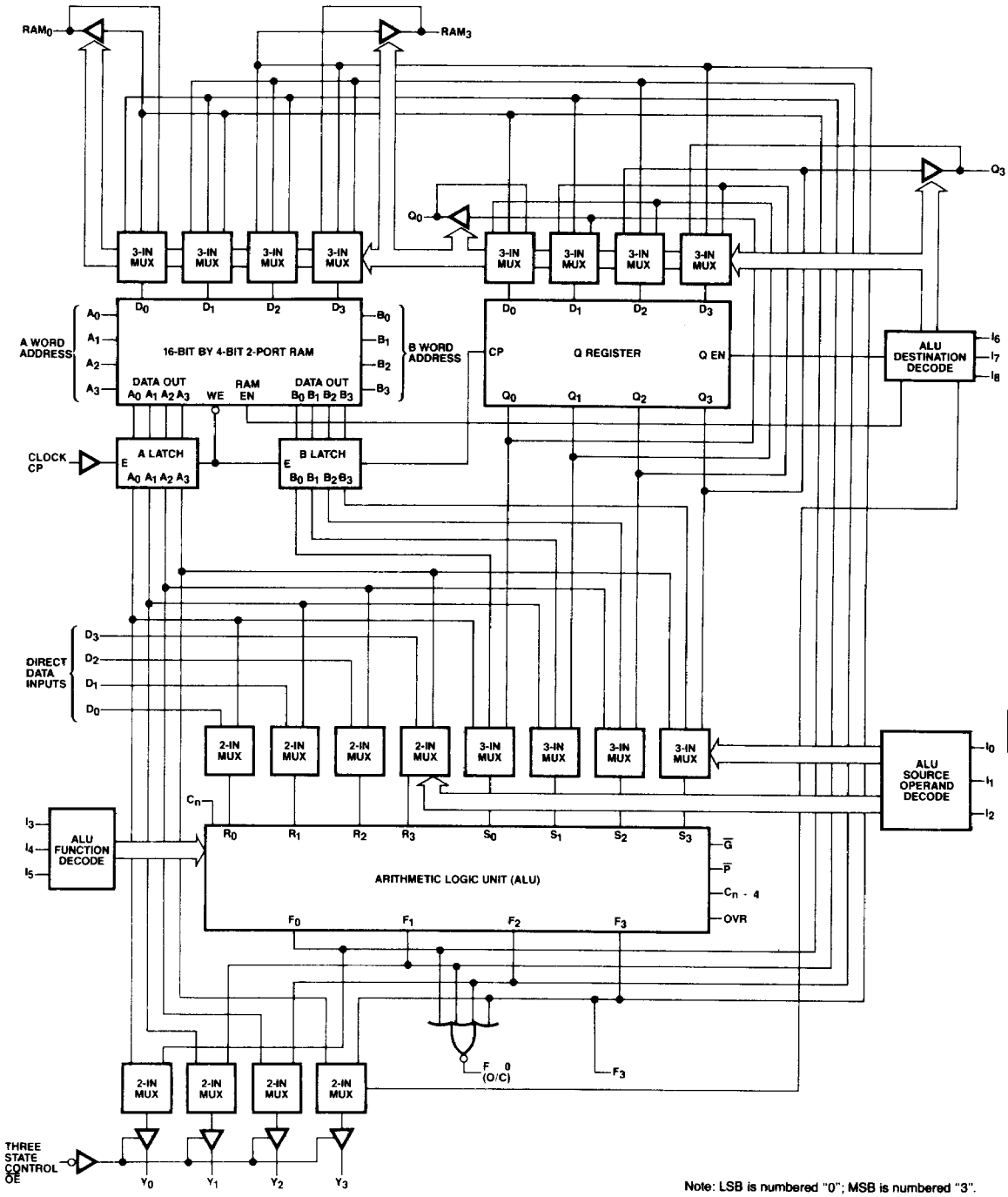
The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. this shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Table 3.

The clock input to the 2901A controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address filed when the clock input is LOW.



Note: LSB is numbered "0"; MSB is numbered "3".

Figure 2. Detailed 2901A Microprocessor Block Diagram

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5V to +7.0V
Input voltage ..... −0.5V to +5.5V
Input current ..... −30 mA to +5 mA
Output current 30mA
Storage temperature range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	MILITARY MIN	MILITARY NOM	MILITARY MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating free air temperature				0	25	75	°C
T_C	Operating case temperature	−55	25	125				°C

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY MIN	MILITARY TYP[2]	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP[2]	COMMERCIAL MAX	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA	Y_0, Y_1, Y_2, Y_3	2.4			2.4			V
			I_{OH} = −1.0mA, C_{n+4}		2.4			2.4			
			I_{OH} = −800μA, OVR, $\overline{P}$		2.4			2.4			
			I_{OH} = −600μA, F_3		2.4			2.4			
			I_{OH} = −600μA	$RAM_{0,3}$, $Q_{0,3}$	2.4			2.4			
			I_{OH} = −1.6mA, $\overline{G}$		2.4			2.4			
I_{CEX}	Output leakage current for F = 0 output	V_{CC} = MIN, V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}				250			250		μA
V_{OL}	Ouptut LOW voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA					0.5		V
				I_{OL} = 16mA		0.5					
			$\overline{G}$, F = 0	I_{OL} = 16mA		0.5			0.5		
			C_{n+4}	I_{OL} = 10mA		0.5			0.5		
			OVR, $\overline{P}$	I_{OL} = 8.0mA		0.5			0.5		
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA		0.5			0.5		
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs[7]			2.0			2.0			V
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs[7]				0.8			0.8		V
V_I	Input clamp voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5			−1.5		V
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = 0.5	Clock, $\overline{OE}$			−0.36			−0.36		mA
			A_0, A_1, A_2, A_3			−0.36			−0.36		
			B_0, B_1, B_2, B_3			−0.36			−0.36		
			D_0, D_1, D_2, D_3			−0.72			−0.72		
			I_0, I_1, I_2, I_6, I_8			−0.36			−0.36		
			I_3, I_4, I_5, I_7			−0.72			−0.72		
			$RAM_{0,3}, Q_{0,3}$[4]			−0.8			−0.8		
			C_n			−3.6			−3.6		

Electrical Characteristics (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY MIN	MILITARY TYP[2]	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP[2]	COMMERCIAL MAX	UNIT
I_{IH}	Input HIGH current	V_{CC} = MAX, V_{IN} = 2.7V	Clock, $\overline{OE}$				20			20	μA
			A_0,A_1,A_2,A_3				20			20	
			B_0,B_1,B_2,B_3				20			20	
			D_0,D_1,D_2,D_3				40			40	
			I_0,I_1,I_2,I_6,I_8				20			20	
			I_3,I_4,I_5,I_7				40			40	
			$RAM_{0,3},Q_{0,3}$[4]				100			100	
			C_n				200			200	
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 5.5V					1.0			1.0	mA
I_{OZH}	Off state (high impedance) output current	V_{CC} = MAX	Y_0,Y_1,Y_2,Y_3	V_O = 2.4V			50			50	μA
I_{OZL}				V_O = 0.5V			−50			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V[4]			100			100	
				V_O = 0.5V[4]			−800			−800	
I_{OS}	Output short circuit current	V_{CC} = 5.75V, V_O = 0.5V	$Y_0,Y_1,Y_2,Y_3,\overline{G}$		−30	−85		−30	−85		mA
			C_{n+4}		−30	−85		−30	−85		
			OVR, $\overline{P}$		−30	−85		−30	−85		
			F_3		−30	−85		−30	−85		
			$RAM_{0,3},Q_{0,3}$		−30	−85		−30	−85		
I_{CC}	Power supply current	V_{CC} = MAX	T_A = 25°C			160	250		160	250	mA
			T_A = 0°C to +70°C	2901A		160	265		160	265	
			T_A = +70°C	NC, JC		160	220		160	220	
			T_C = −55°C to +125°C	2901A		160	280		160	280	
			T_C = +125°C	JM,FM		160	190		160	190	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = 2901ADM, FM. "COM'L" = 2901A NC, JC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Table 1. ALU Source Operand Control.

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	OCTAL CODE	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Table 2. ALU Function Control.

MICRO CODE				ALU FUNCTION	SYMBOL
I_5	I_4	I_3	OCTAL CODE		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S − R
L	H	L	2	R Minus S	R − S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ⊻ S
H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Table 3. ALU Destination Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high impedance state.
B = Register Addressed by B inputs.
Up is toward MSLB, Down is toward LSB.

Table 4. Source Operand and ALU Function Matrix.

I_{543} OCTAL	I_{210} OCTAL / ALU SOURCE / ALU FUNCTION	0	1	2	3	4	5	6	7
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1	C_n = L S Minus R C_n = H	Q−A−1 Q−A	B−A−1 B−A	Q−1 Q	B−1 B	A−1 A	A−D−1 A−D	Q−D−1 Q−D	−D−1 −D
2	C_n = L R Minus S C_n = H	A−Q−1 A−Q	A−B−1 A−B	−Q−1 −Q	−B−1 −B	−A−1 −A	D−A−1 D−A	D−Q−1 D−Q	D−1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ⊻ Q	A ⊻ B	Q	B	A	D ⊻ A	D ⊻ Q	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ⊻ = EX-OR

Source Operands and ALU Functions

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect on the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode the carry will affect the function performed, while in the logic mode the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the 2901A can perform and Table 6 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Table 5. ALU Logic Mode Functions. (C_n Irrelevant)

OCTAL I_{543}, I_{210}	GROUP	FUNCTION
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ∀ Q
6 1		A ∀ B
6 5		D ∀ A
6 6		D ∀ Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

Table 6. ALU Arithmetic Mode Functions.

OCTAL	C_n = 0 (LOW)		C_n = 1 (HIGH)	
I_{543}, I_{210}	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q−1	PASS	Q
1 3		B−1		B
1 4		A−1		A
2 7		D−1		D
2 2	1's Comp.	−Q−1	2's Comp. (Negate)	−Q
2 3		−B−1		−B
2 4		−A−1		−A
1 7		−D−1		−D
1 0	Subtract (1's Comp)	Q−A−1	Subtract (2's Comp)	Q−A
1 1		B−A−1		B−A
1 5		A−D−1		A−D
1 6		Q−D−1		Q−D
2 0		A−Q−1		A−Q
2 1		A−B−1		A−B
2 5		D−A−1		D−A
2 6		D−Q−1		D−Q

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Logic Functions For G, P, C_{n+4}, and OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901A is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 = P_3P_2G_1 = P_3P_2P_1G_0 = P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 = P_2P_1P_0C_n$

Table 7. Logic Equations for Generate, Propagate, Carry-out and Overflow.

I_{543}	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute $\overline{R}_i$ for R_i in definitions →		
6	R ∀ S	← Same as $R \forall \overline{S}$, but substitute $\overline{R}_i$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + C_n)}$	See note

Note: $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Definition of Terms

A_{0-3}—The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3}—The four-address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8}—The nine instruction control lines to the 2901A, used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3, RAM_3—A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the 2901A. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0, RAM_0—Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3}—Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the 2901A. D_0 is the LSB.

Y_{0-3}—The four data outputs of the 2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$—Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$, $\overline{G}$—The carry generate and propagate outputs of the 2901A's ALU. These signals are used with the 2902 for carry-lookahead.

OVR—Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0—This is an open collector output which goes HIGH (OFF) if the data on the four ALU oututs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n—The carry-in to the 2901A's ALU.

C_{n+4}—The carry-out of the 2901A's ALU.

CP—The clock to the 2901A. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

Guaranteed Operating Conditions Over Temperature and Voltage

Tables 8, 9 and 10 define the timing requirements of the 2901A in a system. The 2901A is guaranteed to function correctly over the operating range when used within the delay and set-up time constraints of these tables for the appropriate device type. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The later table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) at which each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 8. Cycle Time and Clock Characteristics

TIME	COMMERCIAL	MILITARY
Read-modify-write cycle (time from selection of A, B registers to end of cycle)	100 ns	110 ns
Maximum clock frequency to shift Q register (50% duty cycle) I = 432 or 632	15MHz	12MHz
Minimum clock LOW time	30ns	30ns
Minimum clock HIGH time	30ns	30ns
Minimum clock period	100ns	110ns

Table 9. Combinational Propagation Delay[7]

TO OUTPUT / FROM INPUT	COMMERCIAL								MILITARY								UNIT
	Y	F_3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0 R_L = 270	OVR	SHIFT OUTPUTS RAM_0 RAM_3	Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0 R_L = 270	OVR	SHIFT OUTPUTS RAM_0 RAM_3	Q_0 Q_3	
A, B	80	80	75	65	87	85	95	—	85	85	80	70	97	90	100	—	ns
D (arithmetic mode)	45	45	45	35	57	55	65	—	50	50	50	40	62	60	70	—	ns
D (I = X37)[5]	40	40	—	—	52	—	60	—	45	45	—	—	57	—	65	—	ns
C_n	30	30	20	—	47	30	50	—	35	35	25	—	52	35	55	—	ns
I_{012}	55	55	50	45	67	65	75	—	60	60	55	50	72	70	80	—	ns
I_{345}	55	55	55	50	67	65	75	—	60	60	60	55	72	70	80	—	ns
I_{678}	30	—	—	—	—	—	30	30	35	—	—	—	—	—	35	35	ns
$\overline{OE}$ Enable/ Disable	35/ 25	—	—	—	—	—	—	—	40/ 25	—	—	—	—	—	—	—	ns
A bypassing ALU (I = 2xx)	45	—	—	—	—	—	—	—	50	—	—	—	—	—	—	—	ns
Clock[6] ↓	60	60	60	50	72	70	80	30	65	65	65	55	82	75	85	35	ns

Table 10. Set-up and Hold Times[1]

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
A, B[2,4] Source[3,5]	100 $t_{pw}L$ + 30	0	110 $t_{pw}L$ + 30	0	ns
B dest.[2,4]	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0	ns
D (arithmetic mode)	70	0	75	0	ns
D (I = X37)[5]	60	0	65	0	ns
C_n	55	0	60	0	ns
I_{012}	80	0	85	0	ns
I_{345}	80	0	85	0	ns
I_{678}	$t_{pw}L$ + 30	0	$t_{pw}L$ + 30	0	ns
$RAM_{0,3}$,$Q_{0,3}$	25	0	25	0	ns

For notes, see Figure 3.

Set-Up and Hold Times (minimum cycles from each input)

Set-up and hold times are defined relative to the clock LOW-to-HIGH edge. Inputs must be steady at all times from the set-up time prior to the clock until the hold time after the clock. The set-up times allow sufficient time to perform the correct operation on the correct data so that the proper ALU data can be written into one of the registers.

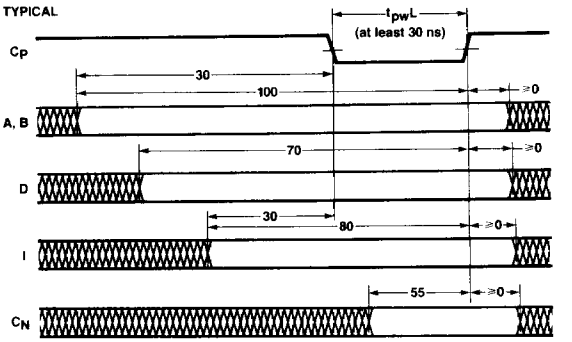
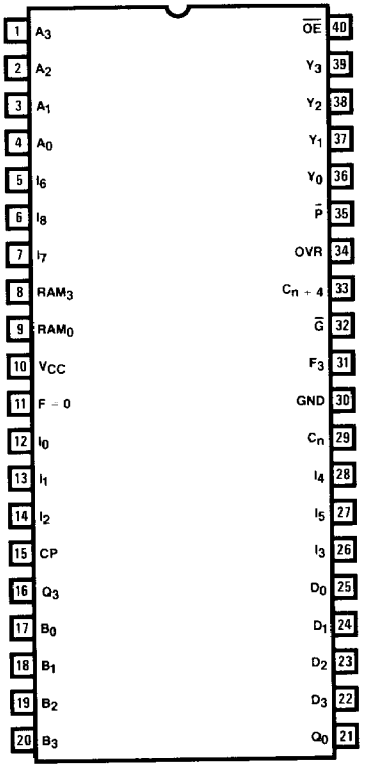


Figure 3. Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for 2901ADC, in ns. See Table 10 for Detailed Information.

Notes:
1. See Figure 3.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B Dest" set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. D V 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.
7. C_L = 50pF (except output disable tests).

Pin Configurations

DIP



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