TruePHY ™ ET1081
Gigabit Ethernet Octal PHY

Features

- 10Base-T, 100Base-TX, and 1000Base-T gigabit Ethernet transceiver:
  — 388-pin PBGA
  — 0.13 µm process
- Oversampling architecture to improve signal integrity and SNR
- SGMII or SerDes interfaces to MAC or switch
- Low power consumption:
  — Less than 750 mW per port in 1000Base-T mode
  — Advanced power management
- On-chip cable diagnostics
- Automatic speed downshift
- Optimized, extended performance echo and NEXT filters
- All-digital baseline wander correction
- Digital PGA control
- 2.5 V and 1.0 V power supplies
- JTAG
- Four programmable LEDs per port

Introduction

Agere Systems ET1081 is an 8-port gigabit Ethernet transceiver fabricated on a single CMOS chip. Packaged in a 388-pin PBGA, the ET1081 is built on 0.13 µm technology for low power consumption and application in high-density switches. The 10/100/1000Base-T device is fully compliant with *IEEE*® 802.3, 802.3u, and 802.3ab standards.

The ET1081 uses an oversampling architecture to gather more signal energy from the communication channel than possible with traditional architectures. The additional signal energy or analog complexity transfers into the digital domain. The result is an analog front end that delivers robust operation, reduced cost, and lower power consumption than traditional architectures.

Using oversampling has allowed for the implementation of a fractionally spaced equalizer, which provides better equalization and has greater immunity to timing jitter, resulting in better signal-to-noise ratio (SNR) and improved BER. In addition, advanced timing algorithms are used to enable operation over a wider range of cabling plants.

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Functional Description

Agere Systems ET1081 is an octal port gigabit Ethernet transceiver. Each port simultaneously transmits and receives on each of the four UTP pairs of category 5 cable (signal dimensions or channels A, B, C, and D) at 125 Msymbols/s using five-level pulse amplitude modulation (PAM). Figure 1 is a block diagram of a single port. Figure 2 is a block diagram of the octal PHY.

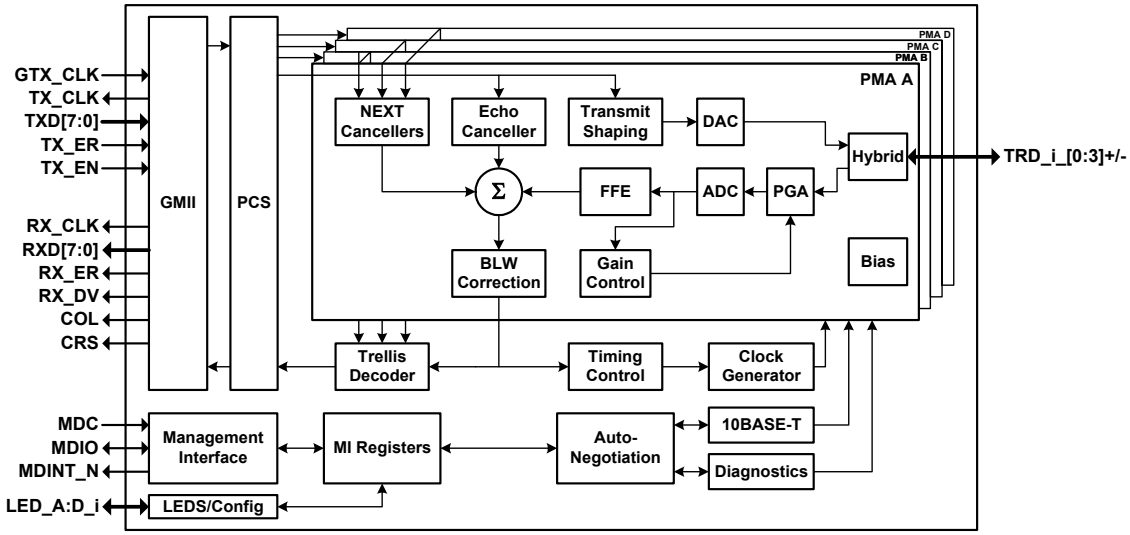


Figure 1. ET1081 Single-Port Block Diagram

Functional Description (continued)

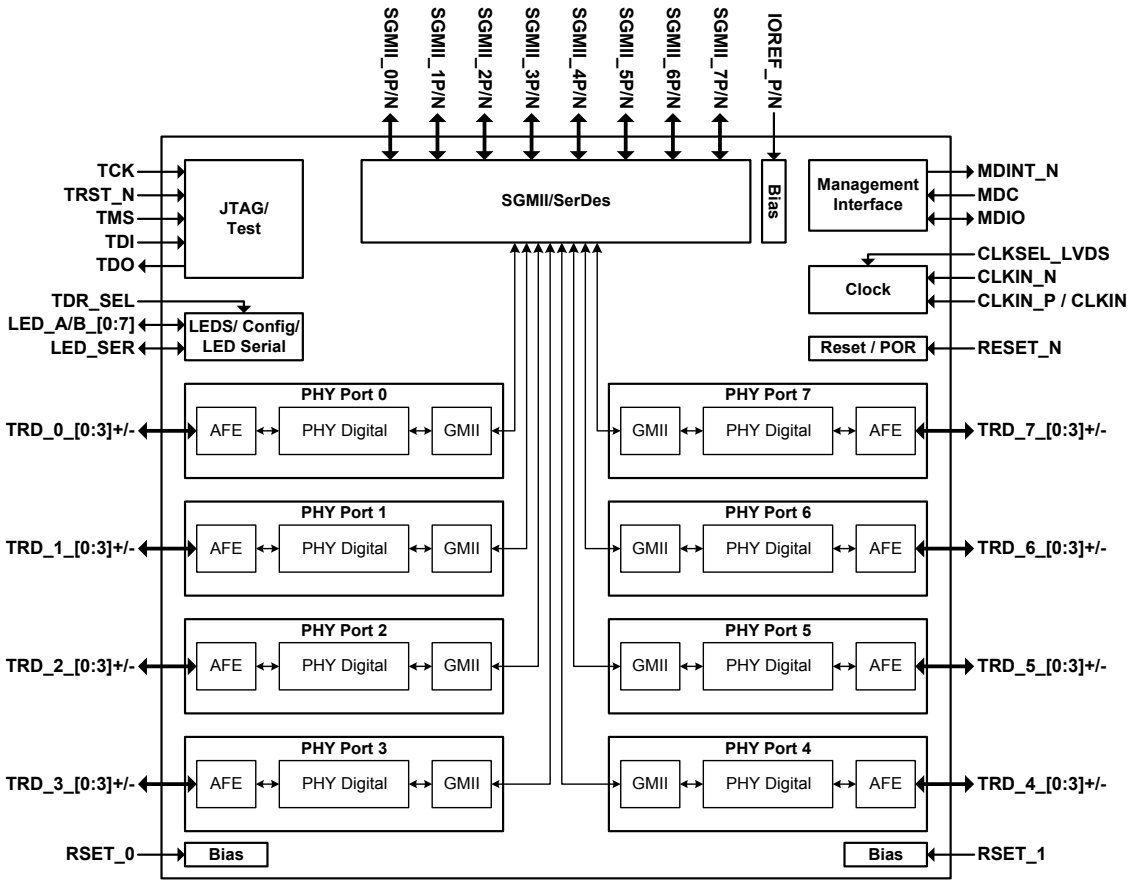


Figure 2. ET1081 Block Diagram

Oversampling Architecture

The ET1081 architecture uses oversampling techniques to sample at two times the symbol rate. A fractionally spaced, feed-forward equalizer (FFE) adapts to remove intersymbol interference (ISI) and to shape the spectrum of the received signal to maximize the (SNR) at the trellis decoder input. The FFE equalizes the channel to a fixed target response. Oversampling enables the use of a fractionally spaced equalizer (FSE) structure for the FFE, resulting in symbol rate clocking for both the FFE and the rest of the receiver. This provides robust operation and substantial power savings.

Functional Description (continued)

Automatic Speed Downshift

Automatic speed downshift is an enhanced feature of autonegotiation that allows the ET1081 to:

- Fallback in speed, based on cabling conditions or link partner abilities.
- Operate over CAT-3 cabling (in 10Base-T mode).
- Operate over two-pair CAT-5 cabling (in 100Base-TX mode).

For speed fallback, the ET1081 first tries to autonegotiate by advertising 1000Base-T capability. After a number of failed attempts to bring up the link, the ET1081 falls back to advertising 100Base-TX and restarts the autonegotiation process. This process continues through all speeds down to 10Base-T. At this point, there are no lower speeds to try and so the host enables all technologies and starts again.

PHY configuration register, address 22, bits 11 and 10 enable automatic speed downshift and specifies if fallback to 10Base-T is allowed. PHY control register, address 23, bits 11 and 12 specify the number of failed attempts before downshift (programmable to 1, 2, 3, or 4 attempts).

Transmit Functions

1000Base-T Encoder

In 1000Base-T mode, the ET1081 translates 8-bit data from the MAC interfaces into a code group of four quinary symbols that are then transmitted by the PMA as 4D five-level PAM signals over the four pairs of CAT-5 cable.

100Base-TX Encoder

In 100Base-TX mode, 4-bit data from the media-independent interface (MII) is 4B/5B encoded to output 5-bit serial data at 125 MHz. The bit stream is sent to a scrambler, and then encoded to a three-level MLT3 sequence that is then transmitted by the PMA.

10Base-T Encoder

In 10Base-T mode, the ET1081 transmits and receives Manchester-encoded data.

Receive Functions

Decoder 1000Base-T

In 1000Base-T mode, the PMA recovers the 4D PAM signals after compensating for the cabling conditions. The resulting code group is decoded to 8-bit data. Data stream delimiters are translated appropriately, and the data is output to the receive data pins of the MAC interfaces. The GMII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 100Base-TX

In 100Base-TX mode, the PMA recovers the three-level MLT3 sequence that is descrambled and 5B/4B decoded to 4-bit data. This is output to the MII receive data pins after data stream delimiters have been translated appropriately. The MII receive error signal is asserted when invalid code groups are detected in the data stream.

Decoder 10Base-T

In 10Base-T mode, the ET1081 decodes the Manchester-encoded received signal.

Hybrid

The hybrid subtracts the transmitted signal from the input signal allowing full-duplex operation on each of the twisted-pair cables.

Programmable Gain Amplifier (PGA)

The PGA operates on the received signal in the analog domain prior to the analog-to-digital converter (ADC). The gain control module monitors the signal at the output of the ADC in the digital domain to control the PGA. It implements a gain that maximizes the signal at the ADC while ensuring that no hard clipping occurs.

Clock Generator

The Octal PHY has a 25 MHz input clock. This clock is common to all eight ports. Each port has a clock generator circuit that uses the input clock signal and a phase-locked loop (PLL) circuit to generate all the required internal analog and digital clocks. This circuit is controlled by the timing control module.

Analog-to-Digital Converter

The ADC operates at 250 MHz oversampling at twice the symbol rate in 1000Base-T and 100Base-TX. This enables innovative timing recovery and fractional skew correction and has allowed transfer of analog complexity to the digital domain.

Functional Description (continued)

Receive Functions (continued)

Timing Recovery/Generation

The timing recovery and generator block creates the transmit and receive clocks for all modes of operation. In transmit mode, the 10Base-T and 100Base-TX modes use the clock input. While in receive mode, the input clock is locked to the receive data stream. 1000Base-T is implemented using a master-slave timing scheme, where the master transmit and receive are locked to the clock input, and the slave acquires timing information from the receive data stream. Timing recovery is accomplished by first acquiring lock on one channel and then making use of the constant phase relationship between channels to lock on the other pairs, resulting in a simplified PLL architecture. Timing shifts due to changing environmental conditions are tracked by the ET1081.

Adaptive Fractionally Spaced Equalizer

The ET1081's unique oversampling architecture employs an FSE in place of the traditional FFE structure. This results in robust equalization of the communications channel, which translates to superior bit error rate (BER) performance over the widest variety of worst-case cabling scenarios. The all-digital equalizer automatically adapts to changing conditions.

Echo and Crosstalk Cancellers

Since the four twisted pairs are bundled together and not insulated from each other in gigabit Ethernet, each of the transmitted signals is coupled onto the three other cables and is seen at the receiver as near-end crosstalk (NEXT). A hybrid circuit is used to transmit and receive simultaneously on each pair. If the transmitter is not perfectly matched to the line, a signal component will be reflected back as an echo. Reflections can also occur at other connectors or cable imperfections. The ET1081 cancels echo and NEXT by subtracting an estimate of these signals from the equalizer output.

Baseline Wander Correction

A known issue for 1000Base-T and 100Base-TX is that the transformer attenuates at low frequencies. As a result, when a large number of symbols of the same sign are transmitted consecutively, the signal at the receiver gradually dies away. This effect is called baseline wander. By employing a circuit that continuously monitors and compensates for this effect, the probability of encountering a receive symbol error is reduced.

Autonegotiation

Autonegotiation is implemented in accordance with *IEEE* 802.3. The device supports 10Base-T, 100Base-TX, and 1000Base-T and can autonegotiate between them in either half- or full-duplex mode. It can also parallel detect 10Base-T or 100Base-TX. If autonegotiation is disabled, a 10Base-T or 100Base-TX link can be manually selected via the *IEEE* MI registers.

Pair Skew Correction

In gigabit Ethernet, pair skew (timing differences between pairs of cable) can result from differences in length or manufacturing variations between the four individual twisted-pair cables. The ET1081 automatically corrects for both integer and fractional symbol timing differences between pairs.

Automatic MDI Crossover

During autonegotiation, the ET1081 automatically detects and sets the required MDI configuration so that the remote transmitter is connected to the local receiver and vice versa. This eliminates the need for crossover cables or crosswired (MDIX) ports. If the remote device also implements automatic MDI crossover, and/or the crossover is implemented in the cable, the crossover algorithm ensures that only one element implements the required crossover.

Polarity Inversion Correction

In addition to automatic MDI crossover that is necessary for autonegotiation, 10Base-T, and 100Base-TX operation, the ET1081 automatically corrects crossover of the additional two pairs used in 1000Base-T. Polarity inversion on all pairs is also corrected. Both of these effects may arise if the cabling has been incorrectly wired.

Functional Description (continued)

Link Monitor

1000Base-T

Once 1000Base-T is autonegotiated and the link is established, both link partners continuously monitor their local receiver status. If the master device determines a problem with its receiver, it signals the slave and both devices cease transmitting data but transmit IDLE. If the master retrains its receiver within 750 ms, then normal operation recommences. Otherwise, both devices restart autonegotiation.

If the slave device determines a problem with its receiver, it ceases transmitting and expects the master to transmit the IDLE sequence. If the slave retrains its receiver within 350 ms, normal operation recommences when the master signals that its receiver is ready. If either receiver fails to reacquire, then autonegotiation is restarted.

100Base-TX

In 100Base-TX, the ET1081 monitors the link and determines the link quality based on signal energy, mean square error, and scrambler lock. If the link quality is deemed insufficient, transmit and receive data are disabled. If the link had been autonegotiated, then control is handed back to autonegotiation. If the link had been manually set, the 100Base-TX receiver is retrained, and the transmitter is set to transmit idle. Once the link quality has been recovered, data transmit and receive are enabled.

10Base-T

In 10Base-T mode, the ET1081 monitors the link and determines the link quality based on either the presence of valid link pulses or valid 10Base-T packets. If the link is deemed to have failed and the link had been autonegotiated, then control is handed back to autonegotiation. If the link had been manually set, the ET1081 continues to try to reestablish the link.

Functional Description (continued)

Loopback Mode

Enabling loopback mode allows in-circuit testing of the ET1081's digital and analog data path.

The ET1081 provides several options for loopback that test and verify various functional blocks within the PHY. These are digital loopback, analog loopback, and remote loopback. On-chip per-port pattern generators and CRC checkers allow completely self-contained tests for all eight ports in parallel. The pattern generator allows generation of loopback data on-chip without requiring the MAC to provide the data. The on-chip CRC checker can be used to test for correct loopback operation without requiring the MAC to check the receive data. Figure 3 is a block diagram that shows the PHY loopback functionality.

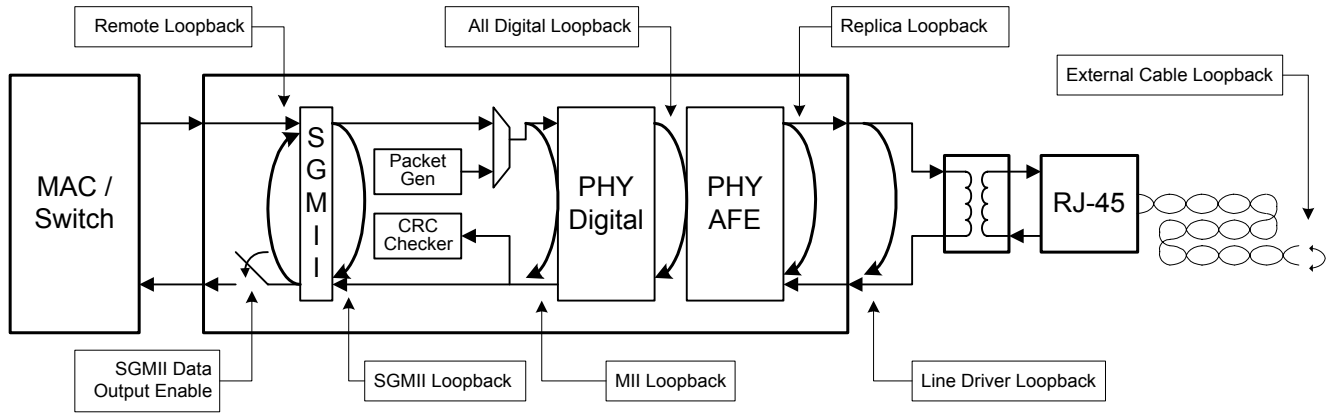


Figure 3. Loopback Functionality

The loopback mode is selected by setting the respective bit in the PHY loopback control register (MII register address 19). The default loopback mode is digital MII loopback. The SGMII Rx data output can be disabled by clearing the SGMII data output enable bit, PHY control register address 23, bit 10. SGMII autonegotiation can be disabled by clearing PHY control register 2, address 18, bit 6. Loopback is enabled by writing to the PHY control register, address 0, bit 14.

Functional Description (continued)

Loopback Mode (continued)

Digital Loopback

Digital loopback provides the ability to loop the transmitted data back to the receiver at various internal points between the MAC interface and the analog front-end (AFE) circuitry. The point at which the data is looped back is selected using the loopback control register (address 19) with the following options being available: MII, SGMII, and all digital.

Selecting the MII option gives a simple loopback with minimal latency wherein the data is looped back directly at the media-independent interface. This loopback is currently set as the default, but it should be noted that it only exercises a small percentage of the PHY circuitry.

When the all-digital option is selected, the transmitted data is looped back at the interface between the digital and the analog circuitry, thereby exercising a high percentage of the digital logic.

Enabling SGMII loopback loops the data at the SGMII pins. SGMII loopback can be used while the PHY is connected to a remote link partner. Comma detection can be disabled in SGMII loopback. Loopback control register, address 19, bit 1 (Comma Enable) is cleared to disable comma detection.

Figure 4 shows a block diagram of digital loopback.

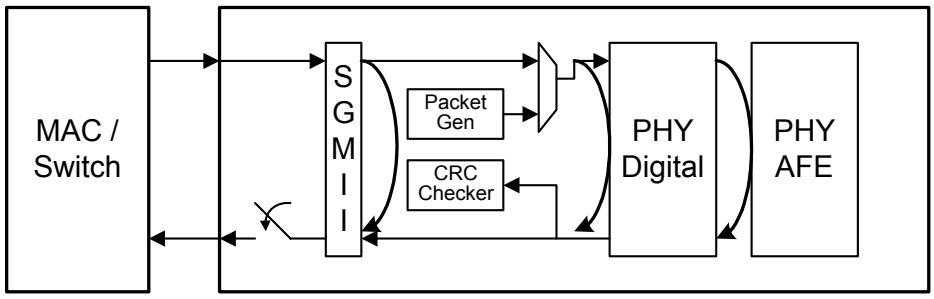


Figure 4. Digital Loopback

Functional Description (continued)

Loopback Mode (continued)

Analog Loopback

Analog loopback provides the ability to loop the transmitted signal back to the receiver within the AFE. The point at which the signal is looped back is selected using the loopback control register with the following options being provided: replica and line driver.

Selecting the replica option causes the transmitted signal to be looped back through the replica generation circuitry of the on-chip hybrid, thereby allowing most of the digital and analog circuitry to be exercised. This loopback mode may be used even when the device is connected to a network because nothing is transmitted to or received from the MDI in this case.

Selecting the line driver option causes the transmitted signal to be looped back at the transformer. This is a more thorough loopback because it tests all the analog circuitry. The most thorough loopback test available without the cooperation of a link partner is provided by enabling external cable loopback. External cable loopback loops SGMII Tx to SGMII Rx via complete digital and analog path and via an external cable. The external cable should have pair A (pins 1 and 2) looped to pair B (pins 3 and 6), and pair C (pins 4 and 5) looped to pair D (pins 7 and 8). This will test all the digital data paths and all the analog circuits. However, in general, neither analog loopback or external cable loopback may be used when the device is connected to a network because they could cause an unanticipated response from the link partner.

Figure 5 shows a block diagram of replica analog loopback, and Figure 6 shows a block diagram of line driver analog loopback and external cable loopback.

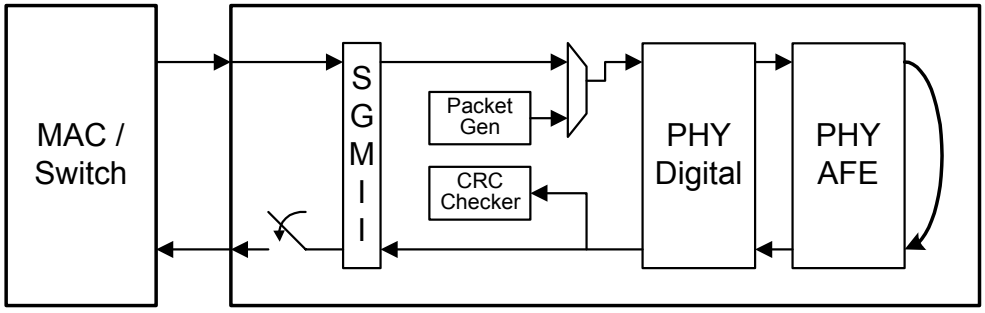


Figure 5. Replica Analog Loopback

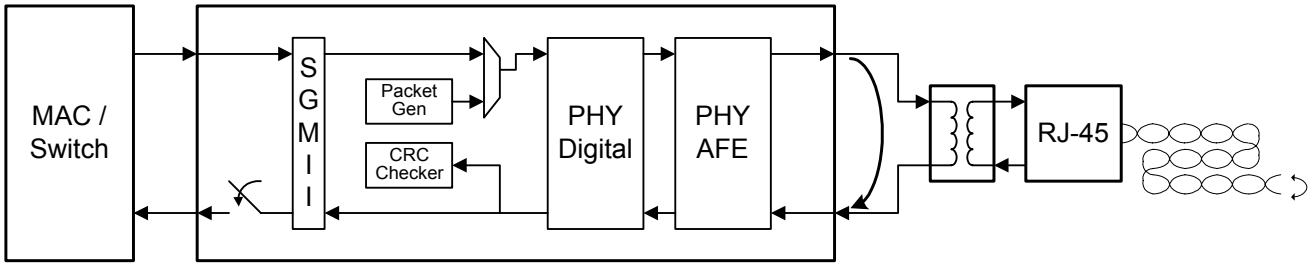


Figure 6. Line Driver and External Cable Analog Loopback

Functional Description (continued)

Loopback Mode (continued)

Remote Loopback

Remote loopback is fundamentally different from digital and analog loopback in that it does not provide self-test capability for the local PHY but, instead, supports self-test for the remote PHY. The concept is that the remote PHY transmits and receives as normal, but in the local PHY, the data received is looped back to the transmitter directly at the MAC interface pins. The result is that the remote PHY has the ability to perform a loopback that incorporates all impairments, including those introduced by the cable and the link partner. Accordingly, remote loopback may be regarded as a form of loopback of the remote PHY and not the local PHY. Figure 7 shows a block diagram of remote loopback.

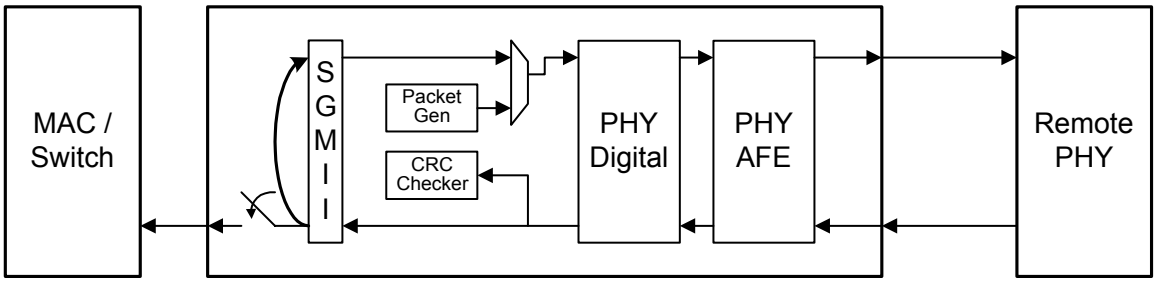


Figure 7. Remote Loopback

Remote loopback can be used to do self-contained octal PHY-to-PHY testing. By externally connecting half of the ports in normal functional mode to the other half of the ports in remote loopback mode, and using the on-chip packet generators and CRC checkers, the complete digital and analog path of all eight ports of the octal can be tested in parallel. Figure 8 shows a block diagram of remote loopback octal PHY-to-PHY testing.

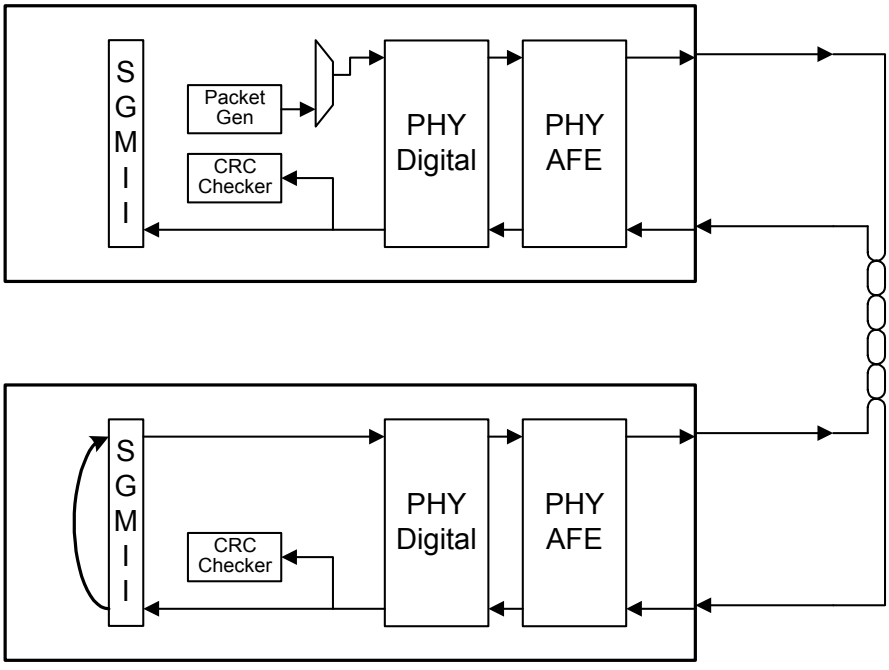


Figure 8. Octal PHY to PHY Remote Loopback (**Only Two Ports Shown**)

Functional Description (continued)

LEDS

Up to four LEDs per port can be supported. Two LEDs per port driven directly from pins and up to four LEDs per port can be supported via an LED serial interface. There is a high degree of programmability allowed and each LED can be programmed to indicate one of sixteen different status functions. Two-color LEDs are also supported. The LEDs can also be used for general-purpose I/O and can be controlled directly from the MII register interface.

Resetting the ET1081

The ET1081 provides the ability to reset the device by hardware (pin RESET_N) or via software through the management interface. A hardware reset is accomplished by driving the active-low pin RESET_N to 0 volts for a minimum of 20 μs. Once RESET_N is driven high (deasserted), the device will have successfully reset within 5 ms. The PHY address pins are read on deassertion of reset.

Hardware Reset

During hardware reset, the ET1081 does the following:

- Initializes all analog circuits.
- Initializes all digital logic and state machines.
- Reads and latches the PHYAD[3] and PHYAD[4] pins.
- Initializes all MII registers to their default values.

Software Reset

A software reset is accomplished by setting bit 15 of the control register (MII register bit 0.15).

Entering software reset, the ET1081 does the following:

- Initializes all digital logic and state machines for that port.
- Initializes all MII registers to their default values values for that port.

The physical address configuration pins PHYAD[3] and PHYAD[4] are not read during software reset.

Low Power Modes

The ET1081 supports software powerdown mode.

Software Powerdown Mode

Software powerdown is entered when bit 11 of the control register (MII register bit 0.11) is set. Software powerdown operates on a per-port basis, each port can be individually powered down. In software powerdown, all PHY functions except the serial management interface and clock circuitry are disabled. The MII registers can be read or written.

At exit from software powerdown, the ET1081 does the following:

- Initializes all digital logic and state machines for that port.

At exit from software powerdown, the physical address configuration pins PHYAD[3] and PHYAD[4] are not read and the MII registers are not reset to their default values.

Pin Information

388-PGBA Pin Diagram

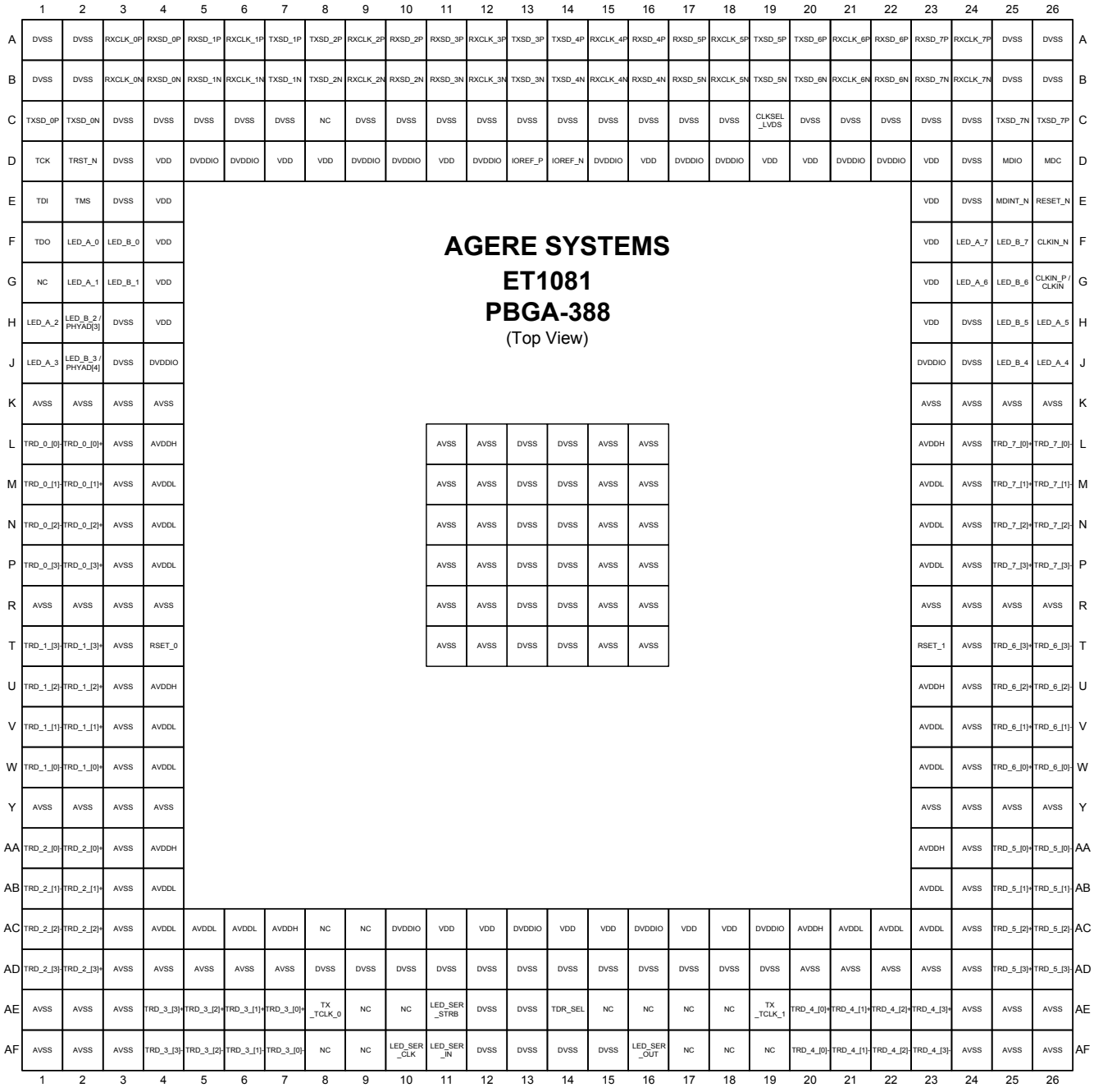


Figure 9. Pin Diagram for ET1081 in 388-Ball PBGA Package (Top View)

Pin Information (continued)

388-PGBA Functional Pin Diagram

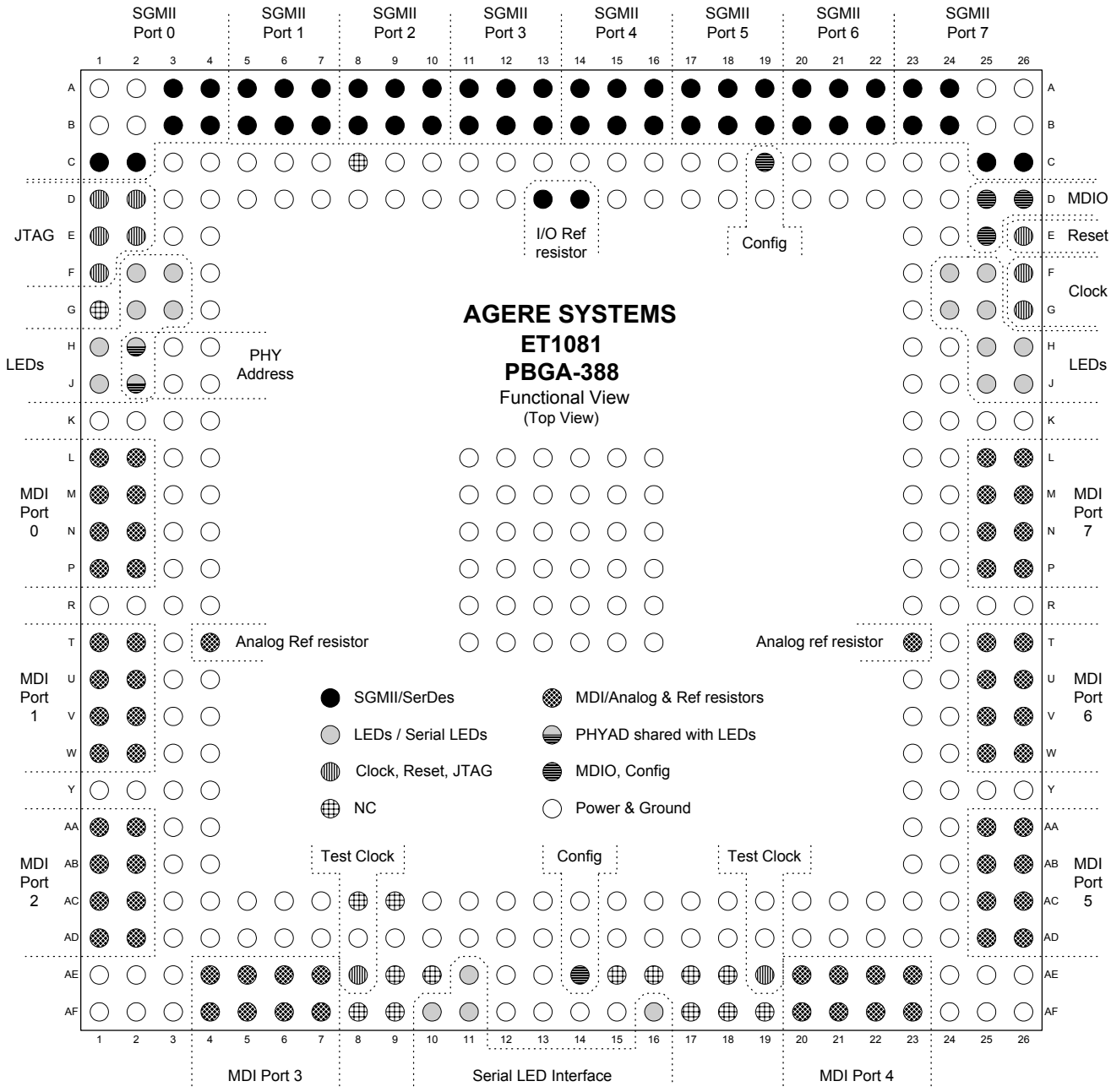


Figure 10. 388-PGBA Functional Pin Diagram

Pin Information (continued)

Pin Descriptions

Table 1. Agere Systems ET1081 Device Signals by Interface, 388-Ball PBGA

Name	Ball	Description	Pad Type	Hyster-esis/ Open Drain	Internal Pull-Up/ Pull-Down	3-State	Analog
MAC: SGMII—Gigabit Media-Independent Interface							
RXSD[7:0]P/N	A23, B23, A22, B22, A17, B17, A16, B16, A11, B11, A10, B10, A5, B5, A4, B4	Differential receive data per port to MAC/switch	O	LVDS	—	—	—
RXCLK[7:0]P/N	A24, B24, A21, B21, A18, B18, A15, B15, A12, B12, A9, B9, A6, B6, A3, B3	Differential receive clock per port synchronous with RXSD[0:7]P/N	O	LVDS	—	—	—
TXSD[7:0]P/N	C26, C25, A20, B20, A19, B19, A14, B14, A13, B13, A8, B8, A7, B7, C1, C2	Differential transmit data per port from MAC/switch	I	LVDS	—	—	—
IOREF_P, IOREF_N	D13, D14	SGMII reference resistor	I/O	—	—	—	A
MDI: Transformer Interface							
TRD_0_[0:3]+/–	L2, L1, M2, M1, N2, N1, P2, P1	Transmit and receive differential pairs for port 1	I/O	—	—	—	A
TRD_1_[0:3]+/–	W2, W1, V2, V1, U2, U1, T2, T1	Transmit and receive differential pairs for port 2	I/O	—	—	—	A
TRD_2_[0:3]+/–	AA2, AA1, AB2, AB1, AC2, AC1, AD2, AD1	Transmit and receive differential pairs for port 3	I/O	—	—	—	A
TRD_3_[0:3]+/–	AE7, AF7, AE6, AF6, AE5, AF5, AE4, AF4	Transmit and receive differential pairs for port 3	I/O	—	—	—	A
TRD_4_[0:3]+/–	AE20, AF20, AE21, AF21, AE22, AF22, AE23, AF23	Transmit and receive differential pairs for port 4	I/O	—	—	—	A
TRD_5_[0:3]+/–	AA25, AA26, AB25, AB26, AC25, AC26, AD25, AD26	Transmit and receive differential pairs for port 5	I/O	—	—	—	A
TRD_6_[0:3]+/–	W25, W26, V25, V26, U25, U26, T25, T26	Transmit and receive differential pairs for port 6	I/O	—	—	—	A
TRD_7_[0:3]+/–	L25, L26, M25, M26, N25, N26, P25, P26	Transmit and receive differential pairs for port 7	I/O	—	—	—	A
RSET_0, RSET_1	T4, T23	Analog reference resistor	I/O	—	—	—	A
Management Interface							
PHYAD[3]	H2	PHY address 3	I	—	Pull-down	—	—
PHYAD[4]	J2	PHY address 4	I	—	Pull-down	—	—
MDIO	D25	Management data I/O	I/O	—	Pull-up	Z	—
MDINT_N	E25	Management interface interrupt	O	OD	—	—	—
MDC	D26	Management interface clock	I	—	Pull-down	—	—

Pin Information (continued)

Pin Descriptions (continued)

Table 1. Agere Systems ET1081 Device Signals by Interface, 388-Ball PBGA (continued)

Name	Ball	Description	Pad Type	Hyster-esis/ Open Drain	Internal Pull-Up/ Pull-Down	3-State	Analog
LED Interface							
LED_A_0	F2	LED A output for port 0	O	—	Pull-up	—	—
LED_B_0	F3	LED B output for port 0	O	—	Pull-up	—	—
LED_A_1	G2	LED A output for port 1	O	—	Pull-up	—	—
LED_B_1	G3	LED B output for port 1	O	—	Pull-down	—	—
LED_A_2	H1	LED A output for port 2	O	—	Pull-up	—	—
LED_B_2	H2	LED B output for port 2	O	—	Pull-down	—	—
LED_A_3	J1	LED A output for port 3	O	—	Pull-up	—	—
LED_B_3	J2	LED B output for port 3	O	—	Pull-down	—	—
LED_A_4	J26	LED A output for port 4	O	—	Pull-up	—	—
LED_B_4	J25	LED B output for port 4	O	—	Pull-up	—	—
LED_A_5	H26	LED A output for port 5	O	—	Pull-up	—	—
LED_B_5	H25	LED B output for port 5	O	—	Pull-up	—	—
LED_A_6	G24	LED A output for port 6	O	—	Pull-up	—	—
LED_B_6	G25	LED B output for port 6	O	—	Pull-up	—	—
LED_A_7	F24	LED A output for port 7	O	—	Pull-up	—	—
LED_B_7	F25	LED B output for port 7	O	—	Pull-up	—	—
LED_SER_STRB	AE11	Serial LED strobe	I/O	—	Pull-down	—	—
LED_SER_CLK	AF10	Serial LED clock	I/O	—	Pull-down	—	—
LED_SER_IN	AF11	Serial LED input	I	—	Pull-down	—	—
LED_SER_OUT	AF16	Serial LED output	O	—	Pull-down	—	—
JTAG							
TCK	D1	Test clock	I	—	Pull-up	—	—
TRST_N	D2	Test reset	I	H	Pull-down	—	—
TMS	E2	Test mode select	I	—	Pull-up	—	—
TDI	E1	Test data input	I	—	Pull-up	—	—
TDO	F1	Test data output	O	—	Pull-up	—	—

Pin Information (continued)

Pin Descriptions (continued)

Table 1. Agere Systems ET1081 Device Signals by Interface, 388-Ball PBGA (continued)

Name	Ball	Description	Pad Type	Hysteresis/ Open Drain	Internal Pull-Up/ Pull-Down	3-State	Analog
Configuration							
TDR_SEL	AE14	Select TDR Cable Diagnostic Mode	I	—	Pull-down	—	—
Clocking and Reset							
CLKSEL_LVDS	C19	Select LVDS input clock	I	—	Pull-up	—	—
CLKIN	G26	Single-ended input system clock	I	—	—	—	—
CLKIN_P	G26	Input system clock	I	LVDS	—	—	A
CLKIN_N	F26						
RESET_N	E26	Reset	I	—	—	—	—
TX_TCLK_0	AE8	Transmit test clock for ports 0 to 3	O	—	—	—	—
TX_TCLK_1	AE19	Transmit test clock for ports 4 to 7	O	—	—	—	—
Power, Ground, and No Connect							
DVDDIO	D5, D6, D9, D10, D12, D15, D17, D18, D21, D22, J4, J23, AC10, AC13, AC16, AC19	Digital I/O 2.5 V	V_{DD}	—	—	—	—
VDD	D4, D7, D8, D11, D16, D19, D20, D23, E4, E23, F4, F23, G4, G23, H4, H23, AC11, AC12, AC14, AC15, AC17, AC18	Digital core 1.0 V	V_{DD}	—	—	—	—
DVSS	A1, A2, A25, A26, B1, B2, B25, B26, C3, C4, C5, C6, C7, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C20, C21, C22, C23, C24, D3, D24, E3, E24, H3, H24, J3, J24, L13, L14, M13, M14, N13, N14, P13, P14, R13, R14, T13, T14, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AE12, AE13, AF12, AF13, AF14, AF15	Digital ground	V_{SS}	—	—	—	—
AVDDH	L4, L23, U4, U23, AA4, AA23, AC7, AC20	Analog 2.5 V	V_{DD}	—	—	—	—

Pin Information (continued)

Pin Descriptions (continued)

Table 1. Agere Systems ET1081 Device Signals by Interface, 388-Ball PBGA (continued)

Name	Ball	Description	Pad Type	Hysteresis/ Open Drain	Internal Pull-Up/ Pull-Down	3-State	Analog
Power, Ground, and No Connect (continued)							
AVDDL	M4, M23, N4, N23, P4, P23, V4, V23, W4, W23, AB4, AB23, AC4, AC5, AC6, AC21, AC22, AC23	Analog power 1.0 V	V_{DD}	—	—	—	—
AVSS	K1, K2, K3, K4, K23, K24, K25, K26, L3, L11, L12, L15, L16, L24, M3, M11, M12, M15, M16, M24, N3, N11, N12, N15, N16, N24, P3, P11, P12, P15, P16, P24, R1, R2, R3, R4, R11, R12, R15, R16, R23, R24, R25, R26, T3, T11, T12, T15, T16, T24, U3, U24, V3, V24, W3, W24, Y1, Y2, Y3, Y4, Y23, Y24, Y25, Y26, AA3, AA24, AB3, AB24, AC3, AC24, AD3, AD4, AD5, AD6, AD7, AD20, AD21, AD22, AD23, AD24, AE1, AE2, AE3, AE24, AE25, AE26, AF1, AF2, AF3, AF24, AF25, AF26	Analog ground	V_{SS}	—	—	—	—
NC	C8, G1, AC8, AC9, AE9, AE10, AE15, AE16, AE17, AE18, AF8, AF9, AF17, AF18, AF19	Reserved—do not connect	—	—	—	—	—

Pin Information (continued)

Pin Descriptions (continued)

Table 2. Alphabetical Pin Listings

Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin
AVDDH	L4	AVSS	K25	AVSS	R15	AVSS	AD3
AVDDH	L23	AVSS	K26	AVSS	R16	AVSS	AD4
AVDDH	U4	AVSS	L3	AVSS	R23	AVSS	AD5
AVDDH	U23	AVSS	L11	AVSS	R24	AVSS	AD6
AVDDH	AA4	AVSS	L12	AVSS	R25	AVSS	AD7
AVDDH	AA23	AVSS	L15	AVSS	R26	AVSS	AD20
AVDDH	AC7	AVSS	L16	AVSS	T3	AVSS	AD21
AVDDH	AC20	AVSS	L24	AVSS	T11	AVSS	AD22
AVDDL	M4	AVSS	M3	AVSS	T12	AVSS	AD23
AVDDL	M23	AVSS	M11	AVSS	T15	AVSS	AD24
AVDDL	N4	AVSS	M12	AVSS	T16	AVSS	AE1
AVDDL	N23	AVSS	M15	AVSS	T24	AVSS	AE2
AVDDL	P4	AVSS	M16	AVSS	U3	AVSS	AE3
AVDDL	P23	AVSS	M24	AVSS	U24	AVSS	AE24
AVDDL	V4	AVSS	N3	AVSS	V3	AVSS	AE25
AVDDL	V23	AVSS	N11	AVSS	V24	AVSS	AE26
AVDDL	W4	AVSS	N12	AVSS	W3	AVSS	AF1
AVDDL	W23	AVSS	N15	AVSS	W24	AVSS	AF2
AVDDL	AB4	AVSS	N16	AVSS	Y1	AVSS	AF3
AVDDL	AB23	AVSS	N24	AVSS	Y2	AVSS	AF24
AVDDL	AC4	AVSS	P3	AVSS	Y3	AVSS	AF25
AVDDL	AC5	AVSS	P11	AVSS	Y4	AVSS	AF26
AVDDL	AC6	AVSS	P12	AVSS	Y23	CLKIN	G26
AVDDL	AC21	AVSS	P15	AVSS	Y24	CLKIN_N	F26
AVDDL	AC22	AVSS	P16	AVSS	Y25	CLKIN_P	G26
AVDDL	AC23	AVSS	P24	AVSS	Y26	CLKSEL_LVDS	C19
AVSS	K1	AVSS	R1	AVSS	AA3	DVDDIO	D5
AVSS	K2	AVSS	R2	AVSS	AA24	DVDDIO	D6
AVSS	K3	AVSS	R3	AVSS	AB3	DVDDIO	D9
AVSS	K4	AVSS	R4	AVSS	AB24	DVDDIO	D10
AVSS	K23	AVSS	R11	AVSS	AC3	DVDDIO	D12
AVSS	K24	AVSS	R12	AVSS	AC24	DVDDIO	D15

Pin Information (continued)

Pin Descriptions (continued)

Table 2. Alphabetical Pin Listings (continued)

Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin
DVDDIO	D17	DVSS	C20	DVSS	AD16	MDINT_N	E25
DVDDIO	D18	DVSS	C21	DVSS	AD17	MDIO	D25
DVDDIO	D21	DVSS	C22	DVSS	AD18	NC	C8
DVDDIO	D22	DVSS	C23	DVSS	AD19	NC	G1
DVDDIO	J4	DVSS	C24	DVSS	AE12	NC	AC8
DVDDIO	J23	DVSS	D3	DVSS	AE13	NC	AC9
DVDDIO	AC10	DVSS	D24	DVSS	AF12	NC	AE9
DVDDIO	AC13	DVSS	E3	DVSS	AF13	NC	AE10
DVDDIO	AC16	DVSS	E24	DVSS	AF14	NC	AE15
DVDDIO	AC19	DVSS	H3	DVSS	AF15	NC	AE16
DVSS	A1	DVSS	H24	IOREF_N	D14	NC	AE17
DVSS	A2	DVSS	J3	IOREF_P	D13	NC	AE18
DVSS	A25	DVSS	J24	LED_A_0	F2	NC	AF8
DVSS	A26	DVSS	L13	LED_A_1	G2	NC	AF9
DVSS	B1	DVSS	L14	LED_A_2	H1	NC	AF17
DVSS	B2	DVSS	M13	LED_A_3	J1	NC	AF18
DVSS	B25	DVSS	M14	LED_A_4	J26	NC	AF19
DVSS	B26	DVSS	N13	LED_A_5	H26	PHYAD[3]	H2
DVSS	C3	DVSS	N14	LED_A_6	G24	PHYAD[4]	J2
DVSS	C4	DVSS	P13	LED_A_7	F24	RESET_N	E26
DVSS	C5	DVSS	P14	LED_B_0	F3	RSET_0	T4
DVSS	C6	DVSS	R13	LED_B_1	G3	RSET_1	T23
DVSS	C7	DVSS	R14	LED_B_2	H2	RXCLK_0N	B3
DVSS	C9	DVSS	T13	LED_B_3	J2	RXCLK_0P	A3
DVSS	C10	DVSS	T14	LED_B_4	J25	RXCLK_1N	B6
DVSS	C11	DVSS	AD8	LED_B_5	H25	RXCLK_1P	A6
DVSS	C12	DVSS	AD9	LED_B_6	G25	RXCLK_2N	B9
DVSS	C13	DVSS	AD10	LED_B_7	F25	RXCLK_2P	A9
DVSS	C14	DVSS	AD11	LED_SER_CLK	AF10	RXCLK_3N	B12
DVSS	C15	DVSS	AD12	LED_SER_IN	AF11	RXCLK_3P	A12
DVSS	C16	DVSS	AD13	LED_SER_OUT	AF16	RXCLK_4N	B15
DVSS	C17	DVSS	AD14	LED_SER_STRB	AE11	RXCLK_4P	A15
DVSS	C18	DVSS	AD15	MDC	D26	RXCLK_5N	B18

Pin Information (continued)

Pin Descriptions (continued)

Table 2. Alphabetical Pin Listings (continued)

Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin
RXCLK_5P	A18	TRD_0_[3]+	P2	TRD_5_[0]–	AA26	TXSD_4N	B14
RXCLK_6N	B21	TRD_1_[0]–	W1	TRD_5_[0]+	AA25	TXSD_4P	A14
RXCLK_6P	A21	TRD_1_[0]+	W2	TRD_5_[1]–	AB26	TXSD_5N	B19
RXCLK_7N	B24	TRD_1_[1]–	V1	TRD_5_[1]+	AB25	TXSD_5P	A19
RXCLK_7P	A24	TRD_1_[1]+	V2	TRD_5_[2]–	AC26	TXSD_6N	B20
RXSD_0N	B4	TRD_1_[2]–	U1	TRD_5_[2]+	AC25	TXSD_6P	A20
RXSD_0P	A4	TRD_1_[2]+	U2	TRD_5_[3]–	AD26	TXSD_7N	C25
RXSD_1N	B5	TRD_1_[3]–	T1	TRD_5_[3]+	AD25	TXSD_7P	C26
RXSD_1P	A5	TRD_1_[3]+	T2	TRD_6_[0]–	W26	TX_TCLK_0	AE8
RXSD_2N	B10	TRD_2_[0]–	AA1	TRD_6_[0]+	W25	TX_TCLK_1	AE19
RXSD_2P	A10	TRD_2_[0]+	AA2	TRD_6_[1]–	V26	VDD	D4
RXSD_3N	B11	TRD_2_[1]–	AB1	TRD_6_[1]+	V25	VDD	D7
RXSD_3P	A11	TRD_2_[1]+	AB2	TRD_6_[2]–	U26	VDD	D8
RXSD_4N	B16	TRD_2_[2]–	AC1	TRD_6_[2]+	U25	VDD	D11
RXSD_4P	A16	TRD_2_[2]+	AC2	TRD_6_[3]–	T26	VDD	D16
RXSD_5N	B17	TRD_2_[3]–	AD1	TRD_6_[3]+	T25	VDD	D19
RXSD_5P	A17	TRD_2_[3]+	AD2	TRD_7_[0]–	L26	VDD	D20
RXSD_6N	B22	TRD_3_[0]–	AF7	TRD_7_[0]+	L25	VDD	D23
RXSD_6P	A22	TRD_3_[0]+	AE7	TRD_7_[1]–	M26	VDD	E4
RXSD_7N	B23	TRD_3_[1]–	AF6	TRD_7_[1]+	M25	VDD	E23
RXSD_7P	A23	TRD_3_[1]+	AE6	TRD_7_[2]–	N26	VDD	F4
TCK	D1	TRD_3_[2]–	AF5	TRD_7_[2]+	N25	VDD	F23
TDI	E1	TRD_3_[2]+	AE5	TRD_7_[3]–	P26	VDD	G4
TDO	F1	TRD_3_[3]–	AF4	TRD_7_[3]+	P25	VDD	G23
TDR_SEL	AE14	TRD_3_[3]+	AE4	TRST_N	D2	VDD	H4
TMS	E2	TRD_4_[0]–	AF20	TXSD_0N	C2	VDD	H23
TRD_0_[0]–	L1	TRD_4_[0]+	AE20	TXSD_0P	C1	VDD	AC11
TRD_0_[0]+	L2	TRD_4_[1]–	AF21	TXSD_1N	B7	VDD	AC12
TRD_0_[1]–	M1	TRD_4_[1]+	AE21	TXSD_1P	A7	VDD	AC14
TRD_0_[1]+	M2	TRD_4_[2]–	AF22	TXSD_2N	B8	VDD	AC15
TRD_0_[2]–	N1	TRD_4_[2]+	AE22	TXSD_2P	A8	VDD	AC17
TRD_0_[2]+	N2	TRD_4_[3]–	AF23	TXSD_3N	B13	VDD	AC18
TRD_0_[3]–	P1	TRD_4_[3]+	AE23	TXSD_3P	A13	—	—

Hardware Interfaces

The following hardware interfaces are included on each ET1081 gigabit Ethernet transceiver:

- MAC interface: SGMII/SerDes
- Management interface
- LED interface
- MDI interface
- Clock and reset
- JTAG
- Power and ground

The following diagram shows the various interfaces on each ET1081 and how they connect to the MAC/switch and other support devices in a typical application.

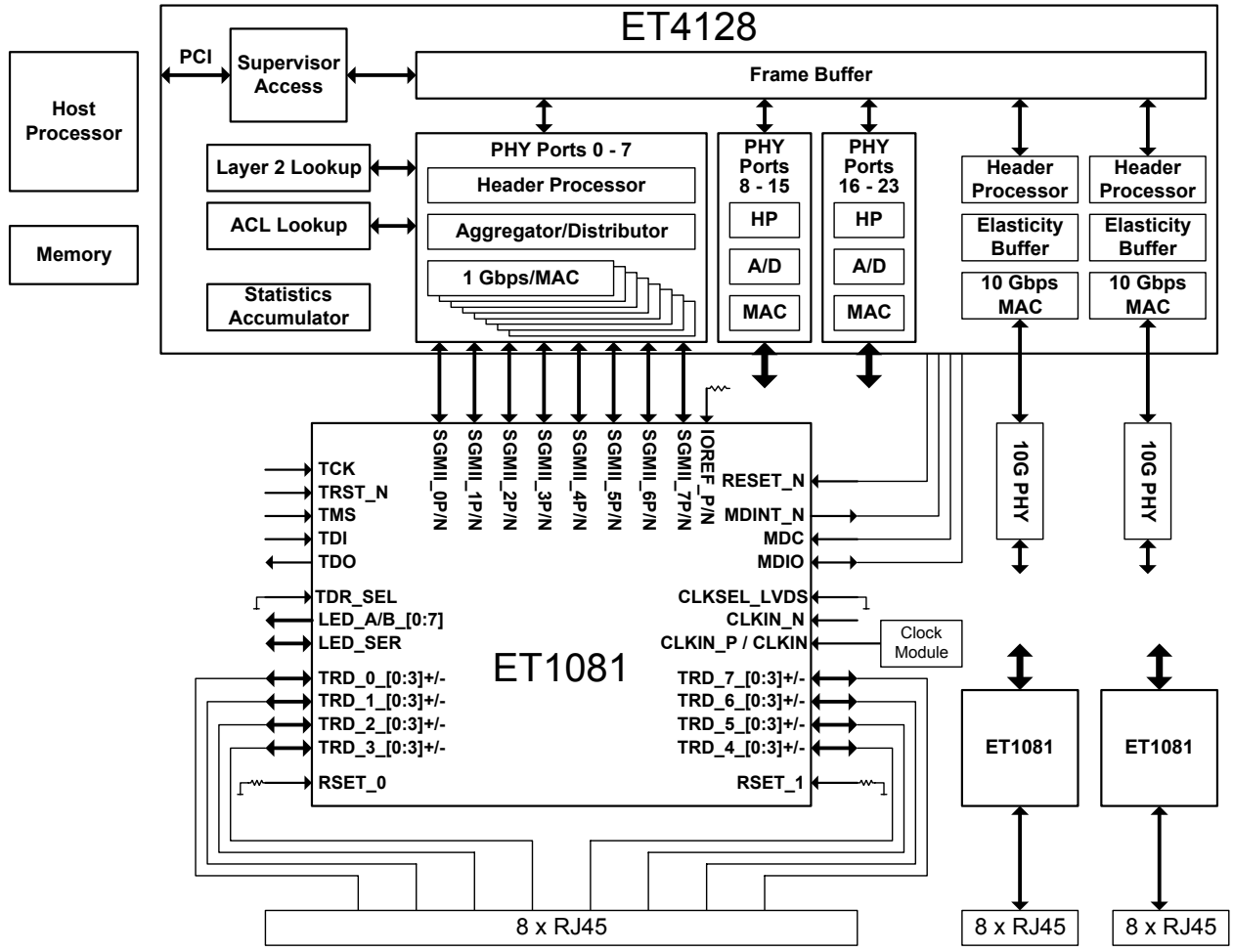


Figure 11. ET1081/ET4128 28 + 2 Gigabit Switch System Block Diagram

Hardware Interfaces (continued)

MAC Interface

The ET1081 supports both a serial SGMII interface and a SerDes interface to the MAC/switch.

Serial Gigabit Media-Independent Interface (SGMII)

The SGMII interface is a high-speed serial interface that supports all the MII/GMII functionality while decreasing the pin count from 25 pins for the GMII to 6 pins. The SGMII interface supports all three Ethernet speeds of 10/100/1000 Mbits/s.

The data path from PHY to MAC/switch is fully source synchronous using receive clock and receive data signals. The connection from the MAC/switch to the PHY only uses the transmit data signal; the clock is recovered from the data stream using clock data recovery (CDR) inside the PHY. The signaling is differential, thus a total of 6 pins per port are required.

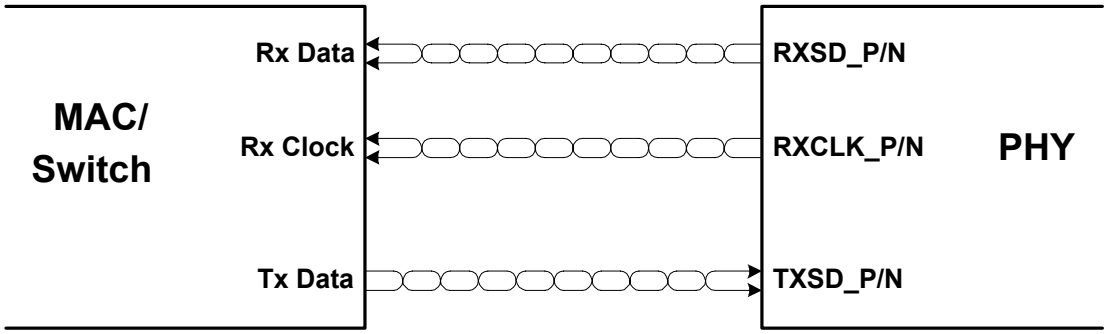


Figure 12. Six-Pin SGMII Interface

Hardware Interfaces (continued)

MAC Interface (continued)

SerDes Interface

The SerDes interface is a high-speed serial interface that supports all the MII/GMII functionality using just 4 pins. All three Ethernet speeds of 10/100/1000 Mbits/s are supported.

The data path between the MAC/switch and the PHY uses transmit and receive data signals. The transmit and receive clocks are recovered from the data streams using CDR in both the MAC/switch and the PHY. The signaling is differential; thus, a total of 4 pins per port are required.

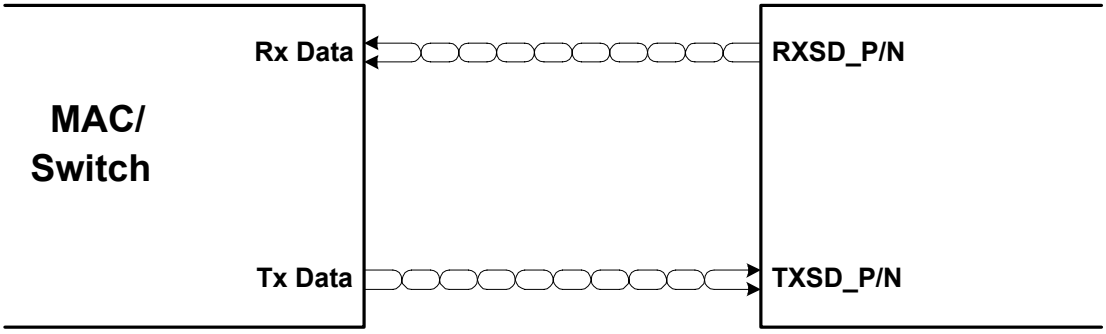


Figure 13. Four-Pin SerDes Interface

The ET1081 uses the SGMII interface by default. The SerDes interface is chosen by disabling the receive clock. This is done by clearing the SGMII RXCLK enable bit in the PHY control register, address 23, bit 9.

Table 3. SGMII/SerDes Signal Description (10/100/1000 Modes)

Pin Name	Pin #	Pin Description	Functional Description
RXSD_[7:0]P, RXSD_[7:0]N	A23, B23, A22, B22, A17, B17, A16, B16, A11, B11, A10, B10, A5, B5, A4, B4	Differential Receive Data	The PHY sources differential receive data (from MDI) to the MAC/switch on a per-port basis. The data rate is 1250 Mbits/s regardless of the link speed.
RXCLK_[7:0]P, RXCLK_[7:0]N	A24, B24, A21, B21, A18, B18, A15, B15, A12, B12, A9, B9, A6, B6, A3, B3	Differential Receive Clock	The PHY sources a 625 MHz clock synchronous with the RXSD_[7:0]P,N on a per-port basis for the MAC/switch to use for capturing the data. This output can be powered down in SGMII 4-pin mode to reduce overall power consumption.
TXSD_[7:0]P, TXSD_[7:0]N	C26, C25, A20, B20, A19, B19, A14, B14, A13, B13, A8, B8, A7, B7, C1, C2	Differential Transmit Data	The MAC/switch sources differential transmit data to the PHY on a per-port basis. The PHY does not require a source synchronous clock to capture this data. The data rate is 1250 Mbits/s regardless of the link speed.
IOREF_P, IOREF_N	D13, D14	I/O Reference Resistor	This pin is an LVDS I/O reference resistor. A precision 100 Ω 1% series resistor should be connected between these two pins.

Hardware Interfaces (continued)

Management Interface

Serial Management Interface

The MII management interface (MI) provides a simple, two-wire serial interface between the MAC and the PHY to allow access to control and status information in the internal registers of the ET1081. The interface is compliant with *IEEE* 802.3 clause 22 and is compatible with the clause 45.3, enabling the two systems to co-exist on the same MDIO bus.

Management Frame Structure

Frames transmitted on the MI have the following structure.

Table 4. Management Frame Structure

Function	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1 . . . 1	01	10	aaaaa	rrrrr	ZO	d . . . d	Z
Write	1 . . . 1	01	01	aaaaa	rrrrr	10	d . . . d	Z

- PRE (preamble): At the beginning of each transaction, the MAC may send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization. The ET1081 supports MF preamble suppression, and thus the MAC may initiate management frames with the ST (start of frame) pattern.
- ST (start of frame): The start of frame is indicated by a <01> pattern. This pattern ensures transitions from the default logic one line state to zero and back to one. When a clause 45 start of frame <00> is received, the frame is ignored.
- OP (operation code): The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.
- PHYAD (PHY address): The PHY address is 5 bits. The first PHY address bit transmitted and received is the MSB of the address. Only the PHY that is addressed will respond to the MI operation.
- REGAD (register address): The register address is 5 bits. The first register address bit transmitted and received is the MSB of the address.
- TA (turnaround): The turnaround time is a 2-bit time spacing between the register address field and the data field of a management frame to avoid contention during a read transaction. For a read transaction, the PHY remains in a high-impedance state for the first bit time of the turnaround and drives a zero bit during the second bit time of the turnaround. During a write transaction, the PHY expects a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround.
- DATA (data): The data field is 16 bits. The first data bit transmitted and received is the MSB of the register being addressed.
- IDLE (idle condition): The IDLE condition on MDIO is a high-impedance state, and the ET1081 internal pull-up resistor will pull the MDIO line to logic one.

Hardware Interfaces (continued)

Management Interface (continued)

Management Frame Structure (continued)

Table 5. Management Interface

Pin Name	Pin #	Pin Description	Functional Description
PHYAD4, PHYAD3	J2, H2	PHY Address 4, PHY Address 3	The physical address of the ET1081 is configured at reset by the current state of the PHYAD4 and PHYAD3 pins. Once these pins have been latched in at reset, the ET1081 is accessible via the management interface at the configured address. The physical address of port 0 is configured by the latched values of PHYAD[4:3] and by assigning 0 to PHYAD[2:0]. The physical address of ports 1—7 is configured by the latched values of PHYAD[4:3] and by assigning 1—7 to PHYAD[2:0]. The default address for port 0 is set to 0 by internal pull up/downs. These may be overridden by external pull-up/downs. The valid range is 0 to 31.
MDC	D26	Management Interface Clock	The management data clock is a reference for the data signal and is generated by the MAC. The ET1081 has a weak internal pull-down resistor on these pins. The management data clock is nominally 2.5 MHz, and can work up to a maximum of 8 MHz.
MDIO	D25	Management Data I/O	The management data input/output is a bidirectional data signal between the MAC and one or more PHYs. This is a 3-state pin that allows either the MAC or the selected PHY to drive this signal. The ET1081 has a weak internal pull-up resistor on these pins. An external pull-up resistor should be used. The exact value depends on the number of PHYs sharing the MDIO signal. Data signals written by the MAC are sampled by the PHY synchronously with respect to the corresponding MDC. Data signals written by the PHY are generated synchronously with respect to the corresponding MDC. This pin requires an external pull-up (1 kΩ to 10 kΩ).
MDINT_N	E25	Management Interface Interrupt	This pin is an active-low, open-drain pin and indicates an unmasked management interrupt on one of ports 0 to 7. This pin requires an external pull-up resistor (1 kΩ to 4.7 kΩ).

Hardware Interfaces (continued)

Management Interface (continued)

Physical Address

The physical address of the ET1081 is configured at reset by the current state of the PHYAD[4:3] pins. These inputs are shared with LED_B_2 and LED_B_3 pins. These pins are read on initial powerup of the ET1081 and during a hardware reset. The logic value at the pin is sensed and latched. After RESET_N has been deasserted (raised high), the shared pins become outputs that are used to drive LEDs.

The physical address of port 0 is configured by the latched values of PHYAD[4:3] and by assigning 0 to PHYAD[2:0]. The physical address of ports 1 to 7 is configured by the latched values of PHYAD[4:3] and by assigning 1 to 7 to PHYAD[2:0]. Thus, the physical address of ports 0 to 7 is a block of eight sequential addresses with port 0 being a multiple of 8.

Management Interrupt

The ET1081 is capable of generating hardware interrupts on pin MDINT_N in response to a variety of user-selectable conditions. MDINT_N is an open-drain, active-low signal that can be wire-ORed with several other ET1081 devices. A single 2.2 kΩ pull-up resistor is recommended for this wire-OR configuration.

When an interrupt occurs, the system can poll the status of the interrupt status register on each port of each device to determine the origin of the interrupt. There are ten conditions that can be selected to generate an interrupt:

- Autonegotiation status change
- CRC error
- Autonegotiation page received
- Full error counter
- FIFO overflow/underflow
- Local/remote Rx status change
- Link status change
- Automatic speed downshift occurred
- MDIO synchronization lost
- TDR completed

The ET1081 is configured to generate an interrupt based on any of these conditions by use of the interrupt mask register (MII register 24). By setting the corresponding bit in the interrupt mask register for the desired condition, the ET1081 will generate the desired interrupt. The ET1081 can be polled on the status of an activated interrupt condition by accessing the MII register interrupt status register (MII register 25). If this condition has occurred, the corresponding bit in the interrupt status register will be set. The interrupt status register is self-clearing on a read operation.

Hardware Interfaces (continued)

LED Interface

Table 6. LED Interface

Pin Name	Pin #	Pin Description	Functional Description
LED_A_0, LED_B_0	F2, F3	LED outputs for port 0	These are the direct-drive LEDs for port 0. LED_A_0 indicates that the link is established. LED_B_0 indicates that there is transmit or receive activity. Setting can be overridden.
LED_A_1, LED_B_1	G2, G3	LED outputs for port 1	As above.
LED_A_2, LED_B_2	H1, H2	LED outputs for port 2	As above.
LED_A_3, LED_B_3	J1, J2	LED outputs for port 3	As above.
LED_A_4, LED_B_4	J26, J25	LED outputs for port 4	As above.
LED_A_5, LED_B_5	H26, H25	LED outputs for port 5	As above.
LED_A_6, LED_B_6	G24, G25	LED outputs for port 6	As above.
LED_A_7, LED_B_7	F24, F25	LED outputs for port 7	As above.

The ET1081 supports two direct-drive, active high LEDs. These LEDs are used to provide link status information to the user. The LEDs can be programmed to stretch out events to either 28 ms, 60 ms, or 100 ms. This makes very short events more visible to the user. All LEDs can be programmed to be on, off, or blink instead of the default status function. This is useful for alternative function indication under host processor control: for example, a system error during power-on self-check. By default, LED_A_i indicates link established and LED_B_i indicates transmit or receive activity. The LEDs can be programmed to indicate one of 16 different status functions:

- 1000Base-T
- 100Base-TX
- 10Base-T
- 10Base-T or 100Base-TX
- 1000Base-T (on) and activity (blink)
- 10Base-T or 100Base-TX (on) and activity (blink)
- 1000Base-T (on) and 100Base-TX (blink)
- Link established
- Link established (on) and activity (blink)
- Link established (on) and receive activity (blink)
- Transmit activity
- Receive activity
- Transmit or receive activity
- Full duplex
- Collision
- Full duplex (on) and collision (blink)

Hardware Interfaces (continued)

LED Interface (continued)

Two-color LEDs are supported. Two LED signals can be used to drive a single, two-color LED. If the two LED signals are not mutually exclusive (e.g., DUPLEX and Collision), a special two-color mode is provided to ensure that the LED will be on when both signals are active. The two-color mode can be configured by use of LED control register 1 (MI registers 27).

The default blink function is a 512 ms, 50% duty cycle blink. The frequency and blink pattern can be programmed over a wide range of values. The LED drivers can be configured by use of LED control register 1, LED control register 2, and LED control register 3 (MI registers 27—29).

LED Serial Interface

Table 7. LED Serial Interface

Pin Name	Pin #	Pin Description	Functional Description
LED_SER_STRB	AE11	Serial LED strobe	Strobe signal for the LED serial interface.
LED_SER_CLK	AF10	Serial LED clock	Clock signal for the LED serial interface.
LED_SER_IN	AF11	Serial LED Input	Input signal for the LED serial interface.
LED_SER_OUT	AF16	Serial LED Output	Output signal for the LED serial interface.

An LED serial interface enables up to four LEDs per port to be supported. The LED values for all eight ports are clocked out of the LED_SER_OUT pin using LED_SER_CLK and LED_SER_STRB as control signals. Up to six octal PHYs can be chained together using the LED_SER_IN pin. External shift registers can then be used to drive the LEDs. It is possible to mix both direct-drive and serial LEDs.

Hardware Interfaces (continued)

Media-Dependent Interface: Transformer Interface

Table 8. Transformer Interface Signals

Pin Name	Pin #	Pin Description	Functional Description
TRD_0_[0:3]+/–	L2, L1, M2, M1, N2, N1, P2, P1	Transmit and Receive Differential Pairs for Port 0	Connect these signal pairs through a transformer to the media-dependent interface for port 0. In 1000Base-T mode, transmit and receive occur simultaneously on all pairs. In 10Base-T and 100Base-TX modes, TRD_0_[0]P/N are used to transmit when operating in the MDI configuration and to receive when operating in the MDI-X configuration. In 10Base-T and 100Base-TX modes, TRD_0_[1]P/N are used to receive when operating in the MDI configuration and to transmit when operating in the MDI-X configuration. In 10Base-T and 100Base-TX modes, TRD_0_[2:3]P/N are unused. The PHY automatically determines the appropriate MDI/MDI-X configuration.
TRD_1_[0:3]+/–	W2, W1, V2, V1, U2, U1, T2, T1	Transmit and Receive Differential Pairs for Port 1	As above for port 1.
TRD_2_[0:3]+/–	AA2, AA1, AB2, AB1, AC2, AC1, AD2, AD1	Transmit and Receive Differential Pairs for Port 2	As above for port 2.
TRD_3_[0:3]+/–	AE7, AF7, AE6, AF6, AE5, AF5, AE4, AF4	Transmit and Receive Differential Pairs for Port 3	As above for port 3.
TRD_4_[0:3]+/–	AE20, AF20, AE21, AF21, AE22, AF22, AE23, AF23	Transmit and Receive Differential Pairs for Port 4	As above for port 4.
TRD_5_[0:3]+/–	AA25, AA26, AB25, AB26, AC25, AC26, AD25, AD26	Transmit and Receive Differential Pairs for Port 5	As above for port 5.
TRD_6_[0:3]+/–	W25, W26, V25, V26, U25, U26, T25, T26	Transmit and Receive Differential Pairs for Port 6	As above for port 6.
TRD_7_[0:3]+/–	L25, L26, M25, M26, N25, N26, P25, P26	Transmit and Receive Differential Pairs for Port 7	As above for port 7.
RSET_0, RSET_1	T4, T23	Analog Reference Resistors	RSET_0 and RSET_1 set the absolute value reference current for the transmitters. Connect each of these signal to analog ground through a precision 6.34 kΩ 1% resistor.

Hardware Interfaces (continued)

Configuration

The default cable diagnostic mode can be set by the TDR_SEL hardware configuration pin. This pin is latched at poweron and reset and sets the default value of the cable diagnostic mode bit in the PHY control register, MI register address 23, bit 13. If TDR_SEL is asserted at reset, MI register address 23, bit 13, will be zero after reset.

Table 9. Configuration

Pin Name	Pin #	Pin Description	Functional Description
TDR_SEL	AE14	Select TDR Cable Diagnostic Mode	Selects the default cable diagnostic mode. 0 = Link analysis mode (default). 1 = TDR mode.

Clocking and Reset

The ET1081 supports both a single-ended input system clock and an LVDS input system clock. The single-ended input system clock is a standard 2.5 V CMOS input (3.3 V tolerant) and uses pin CLKIN. The LVDS input system clock uses pins CLKIN_P and CLKIN_N. Asserting CLKSEL_LVDS selects the LVDS input system clock. Deasserting CLKSEL_LVDS selects the single-ended input system clock. CLKIN and CLKIN_P share the same pin (G26). In single-ended mode, the CLKIN_N pin should be left unconnected.

The ET1081 can output the transmit test clock on pins TX_TCLK_0 and TX_TCLK_1. These are multiplexed outputs of ports 0 to 3 and ports 4 to 7, respectively. They can be used to run the *IEEE* transmitter timing jitter test (40.6.1.2.5). The clock output can be enabled by setting PHY configuration register, address 22 bit 5. Only one PHY out of ports 0 to 3 and one out of ports 4 to 7 should be enabled at a time.

Table 10. Clocking and Reset

Pin Name	Pin #	Pin Description	Functional Description
CLKSEL_LVDS	C19	Select LVDS Input Clock	CLKSEL_LVDS selects the LVDS input system clock. 0 = Single-ended input system clock. 1 = LVDS input system clock.
CLKIN	G26	Single-ended Input System Clock	CLKIN is a 25 MHz single-ended input system clock. In single-ended mode, the CLKIN_N pin should be left unconnected.
CLKIN_P, CLKIN_N	G26, F26	Input System Clock	CLKIN_P/N is a 25 MHz LVDS input system clock.
RESET_N	E26	Reset	RESET_N is an active-low hardware reset. Drive low for 20 μs to initiate a hardware reset. The ET1081 completes all reset operations within 5 ms of this signal returning to a high state. The physical address configuration pins PHYAD[3] and PHYAD[4] (shared with LED pins) are read at the end of hardware reset.
TX_TCLK_0, TX_TCLK_1	AE8, AE19	Transmit test clock	Transmit test clock pins that are available for the purpose of running the *IEEE* jitter test. TX_TCLK_0 is the multiplexed output of the transmit clock for ports 0 to 3 and TX_TCLK_1 is for ports 4 to 7.

Hardware Interfaces (continued)

JTAG

The ET1081 has a standard *IEEE* 1149.1 JTAG test interface. The interface provides extensive test and diagnostics capability. It contains internal circuitry that allows the device to be controlled through the JTAG port to provide on-chip, in-circuit emulation.

The JTAG interface is a bidirectional serial interface with its own reset strobe (TRST_N). The reset strobe can be used independently to reset the JTAG state machine but must be used during a power-on reset (see Reset Timing, page 69). The only exception is when the JTAG interface is not being used. In this scenario, connect the reset strobe to ground to keep the interface in the reset state.

Table 11. JTAG Test Interface

Pin Name	Pin #	Pin Description	Functional Description
TDI	E1	Test Data Input	This signal is the JTAG serial input. All instructions and scanned data are input using this pin. This pin has an internal pull-up resistor.
TDO	F1	Test Data Output	This signal is the JTAG serial output. Scanned data and status bits are output using this pin. This pin has an internal pull-up resistor.
TCK	D1	Test Clock	This signal is the JTAG serial shift clock. It clocks all of the data that passes through the port on TDI and TDO. This pin has an internal pull-up resistor.
TMS	E2	Test Mode Select	This signal is the JTAG test mode control. This pin has an internal pull-up resistor.
TRST_N	D2	Test Reset (JTAG Reset)	This signal is active low and causes the JTAG TAP controller to enter the reset state. This pin has an internal pull-down resistor.

Hardware Interfaces (continued)

Power, Ground, and No Connect

Table 12. Power, Ground, and No Connect

Pin Name	Pin #	Pin Description	Functional Description
DVDDIO	D5, D6, D9, D10, D12, D15, D17, D18, D21, D22, J4, J23, AC10, AC13, AC16, AC19	V_{DD}	Digital I/O 2.5 V supply.
VDD	D4, D7, D8, D11, D16, D19, D20, D23, E4, E23, F4, F23, G4, G23, H4, H23, AC11, AC12, AC14, AC15, AC17, AC18	V_{DD}	Digital core 1.0 V supply.
DVSS	A1, A2, A25, A26, B1, B2, B25, B26, C3, C4, C5, C6, C7, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C20, C21, C22, C23, C24, D3, D24, E3, E24, H3, H24, J3, J24, L13, L14, M13, M14, N13, N14, P13, P14, R13, R14, T13, T14, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AE12, AE13, AF12, AF13, AF14, AF15	V_{SS}	Digital ground.
AVDDH	L4, L23, U4, U23, AA4, AA23, AC7, AC20	V_{DD}	Analog power 2.5 V.
AVDDL	M4, M23, N4, N23, P4, P23, V4, V23, W4, W23, AB4, AB23, AC4, AC5, AC6, AC21, AC22, AC23	V_{DD}	Analog power 1.0 V.
AVSS	K1, K2, K3, K4, K23, K24, K25, K26, L3, L11, L12, L15, L16, L24, M3, M11, M12, M15, M16, M24, N3, N11, N12, N15, N16, N24, P3, P11, P12, P15, P16, P24, R1, R2, R3, R4, R11, R12, R15, R16, R23, R24, R25, R26, T3, T11, T12, T15, T16, T24, U3, U24, V3, V24, W3, W24, Y1, Y2, Y3, Y4, Y23, Y24, Y25, Y26, AA3, AA24, AB3, AB24, AC3, AC24, AD3, AD4, AD5, AD6, AD7, AD20, AD21, AD22, AD23, AD24, AE1, AE2, AE3, AE24, AE25, AE26, AF1, AF2, AF3, AF24, AF25, AF26	V_{SS}	Analog ground.
NC	C8, G1, AC8, AC9, AE9, AE10, AE15, AE16, AE17, AE18, AF8, AF9, AF17, AF18, AF19	No Connect	Reserved—do not connect.

Cable Diagnostics

The ET1081 has on-chip cable diagnostics. The cable analysis uses two distinct methods for evaluating the cable: link analysis and time domain reflectometry (TDR) analysis. This analysis can be used to detect cable impairments that may be preventing a gigabit link or affecting performance.

When there is a link active, the link analysis can detect cable length, link quality, pair skew, pair swaps (MDI/MDI-X configuration), and polarity reversal. When there is no link, TDR can detect cable faults (open circuit, short circuit), distance to the fault, pair fault is on, cable length, pair skew, and excessive crosstalk. Table 10 summarizes the specifications of the cable diagnostic functions.

Table 13. Cable Diagnostic Functions

Feature	Description	10	100	1000	Term	Unterm	Analysis
Detection of Cable Fault on Any Pair	Cable open	—	—	—	✓	✓	Line Probing
	Cable short	—	—	—	✓	✓	
	Indicate distance to fault	—	—	—	±2 m	±2 m	
	Pair swaps	✓	✓	✓[1]	—	—	Link Analysis
Detect Polarity Reversal	—	✓	—[2]	✓	—	—	Link Analysis
Good Cable with Link	Indicate length	—	±10 m	±10 m	—	—	Link Analysis
Good Cable Without Link	Indicate length	—	—	—	±5 m[3]	±2 m	Line Probing
Pair Skew with Link	Detect excessive, >50 ns	—	—	✓	—	—	Link Analysis
Pair Skew Without Link	Detect excessive, >50 ns	—	—	—	✓[3]	✓	Line Probing
Excessive Crosstalk	Cable quality or split pairs	—	—	—	✓	✓	Line Probing

1. Pair swaps on C and D as well as pairs A and B are reported.
2. Polarity reversal in 100Base-TX is not detected because MLT-3 signaling is polarity insensitive.
3. If the magnitude of the peak reflection is greater than 15% of an open circuit.

Register Description

MI Register Address Map

Table 14. MI Register Address Map

Address	Description
00	Control register.
01	Status register.
02	PHY identifier register 1.
03	PHY identifier register 2.
04	Autonegotiation advertisement register.
05	Autonegotiation link partner ability register.
06	Autonegotiation expansion register.
07	Autonegotiation next page transmit register.
08	Link partner next page register.
09	1000Base-T control register.
10	1000Base-T status register.
11—14	Reserved.
15	Extended status register.
16—17	Reserved.
18	PHY control register 2.
19	Loopback control register.
20	RX error counter register.
21	Register management (MI) control register.
22	PHY configuration register.
23	PHY control register.
24	Interrupt mask register.
25	Interrupt status register.
26	PHY status register.
27	LED control register 1.
28	LED control register 2.
29	LED control register 3.
30	Diagnostics control register.
31	Diagnostics status register.

Table 15. Register Type Definition

Type	Description
LL	Latching low.
LH	Latching high.
R/W	Read write. Register can be read or written.
RO	Read only. Register is read only. Writes to register are ignored.
SC	Self-clearing. Register is self-clearing; if a one is written, the register will automatically clear to zero after the function is completed.

Register Description (continued)

Register Functions/Settings

Table 16. Control Register—Address 00

Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reset	1 = PHY reset. 0 = Normal operation.	R/W SC	0	1
14	Loopback	1 = Enable loopback. 0 = Disable loopback.	R/W	0	2
13	Speed Selection (LSB)	Bit 6,13. 11 = Reserved. 10 = 1000 Mbits/s. 01 = 100 Mbits/s. 00 = 10 Mbits/s.	R/W	0	3
12	Autonegotiation Enable	1 = Enable autonegotiation process. 0 = Disable autonegotiation process.	R/W	1	4
11	Powerdown	1 = Powerdown. 0 = Normal operation.	R/W	0	—
10	Isolate	1 = Isolate PHY from MII. 0 = Normal operation.	R/W	0	5
9	Restart Autonegotiation	1 = Restart autonegotiation process. 0 = Normal operation.	R/W SC	0	—
8	Duplex Mode	1 = Full duplex. 0 = Half duplex.	R/W	0	6
7	Collision Test	1 = Enable collision test. 0 = Disable collision test.	R/W	0	7
6	Speed Selection (MSB)	See bit 13.	R/W	1	3
5:0	Reserved	—	RO	0	—

1. The reset bit is automatically cleared upon completion of the reset sequence. This bit is set to 1 during reset.
2. This is the master enable for digital and analog loopback as defined by the standard. The exact type of loopback is determined by the loopback control register (address 19). Bit 0.14 should not be set when using remote loopback
3. The speed selection address 00, bits 13 and 6, may be used to configure the link manually. Setting these bits has no effect unless address 00, bit 12, is clear.
4. When this bit is cleared, the link configuration is determined manually.
5. Setting this bit isolates the PHY from the MII, GMII, or RGMII interfaces.
6. This bit may be used to configure the link manually. Setting this bit has no effect unless address 00, bit 12, is clear.
7. Enables *IEEE* 22.2.4.1.9 collision test.

Register Description (continued)

Register Functions/Settings (continued)

Table 17. Status Register—Address 01

Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	100Base-T4	0 = Not 100Base-T4 capable.	RO	0	1
14	100Base-X Full Duplex	1 = 100Base-X full-duplex capable. 0 = Not 100Base-X full-duplex capable.	RO	1	—
13	100Base-X Half Duplex	1 = 100Base-X half-duplex capable. 0 = Not 100Base-X half-duplex capable.	RO	1	—
12	10Base-T Full-Duplex	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	RO	1	—
11	10Base-T Half-Duplex	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	RO	1	—
10	100Base-T2 Full-Duplex	0 = Not 100Base-T2 full-duplex capable.	RO	0	—
9	100Base-T2 Half-Duplex	0 = Not 100Base-T2 half-duplex capable.	RO	0	—
8	Extended Status	1 = Extended status information in register 0Fh.	RO	1	—
7	Reserved	—	RO	—	—
6	MF Preamble Suppression	1 = Preamble suppressed management frames accepted.	RO	1	—
5	Autonegotiation Complete	1 = Autonegotiation process complete. 0 = Autonegotiation process not complete.	RO	0	2
4	Remote Fault	1 = Remote fault detected. 0 = No remote fault detected.	RO LH	0	3
3	Autonegotiation Ability	1 = Autonegotiation capable. 0 = Not autonegotiation capable.	RO	1	—
2	Link Status	1 = Link is up. 0 = Link is down.	RO LL	0	4
1	Jabber Detect	1 = Jabber condition detected. 0 = No jabber condition detected.	RO LH	0	—
0	Extended Capability	1 = Extended register capabilities.	RO	1	5

1. The ET1081 does not support 100Base-T4 or 100Base-T2; therefore, these register bits will always be set to zero.
2. Upon completion of autonegotiation, this bit becomes set.
3. This bit indicates that a remote fault has been detected. Once set, it remains set until it is cleared by reading register 1 via the management interface or by PHY reset.
4. This bit indicates that a valid link has been established. Once cleared due to link failure, this bit will remain cleared until register 1 is read via the management interface.
5. Indicates that the PHY provides an extended set of capabilities that may be accessed through the extended register set. For a PHY that incorporates a GMII/RGMII, the extended register set consists of all management registers except registers 0, 1, and 15.

Register Description (continued)

Register Functions/Settings (continued)

Table 18. PHY Identifier Register 1—Address 02

PHY Identifier Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	PHY Identifier Bits 3:18	Organizationally unique identifier (OUI), bits 3:18.	RO	0x0282	1

Table 19. PHY Identifier Register 2—Address 03

PHY Identifier Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:10	PHY Identifier Bits 19:24	Organizationally unique identifier (OUI), bits 19:24.	RO	111100	1
9:4	Model Number	Model number = 03.	RO	000011	—
3:0	Revision Number	Revision number = 5.	RO	0101	—

1. Agere's OUI is 00-05-3D.

Register Description (continued)

Register Functions/Settings (continued)

Table 20. Autonegotiation Advertisement Register—Address 04

Autonegotiation Advertisement Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Advertise next page ability supported. 0 = Advertise next page ability not supported.	R/W	0	—
14	Reserved	—	RO	0	—
13	Remote Fault	1 = Advertise remote fault detected. 0 = Advertise no remote fault detected.	R/W	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Advertise asymmetric pause ability. 0 = Advertise no asymmetric pause ability.	R/W	0	—
10	Pause Capable	1 = Capable of full-duplex pause operation. 0 = Not capable of pause operation.	R/W	0	—
9	100Base-T4 Capability	1 = 100Base-T4 capable. 0 = Not 100Base-T4 capable.	R/W	0	1
8	100Base-TX Full-Duplex Capable	1 = 100Base-TX full-duplex capable. 0 = Not 100Base-TX full-duplex capable.	R/W	1	2
7	100Base-TX Half-Duplex Capable	1 = 100Base-TX half-duplex capable. 0 = Not 100Base-TX half-duplex capable.	R/W	1	2
6	10Base-T Full-Duplex Capable	1 = 10Base-T full-duplex capable. 0 = Not 10Base-T full-duplex capable.	R/W	1	2
5	10Base-T Half-Duplex Capable	1 = 10Base-T half-duplex capable. 0 = Not 10Base-T half-duplex capable.	R/W	1	2
4:0	Selector Field	00001 = *IEEE* 802.3 CSMA/CD.	R/W	00001	—

1. The ET1081 does not support 100Base-T4, so the default value of this register bit is zero.
2. A write to this register prior to the completion of autonegotiation causes a restart of autonegotiation. This register is not updated following autonegotiation.

Register Description (continued)

Register Functions/Settings (continued)

Table 21. Autonegotiation Link Partner Ability Register—Address 05

Autonegotiation Link Partner Ability Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next page	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	RO	0	—
14	Acknowledge	1 = Link partner has received link code word. 0 = Link partner has not received link code word.	RO	0	—
13	Remote Fault	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	RO	0	—
12	Reserved	—	RO	0	—
11	Asymmetric Pause	1 = Link partner desired asymmetric pause. 0 = Link partner does not desire asymmetric pause.	RO	0	—
10	Pause Capable	1 = Link partner capable of full-duplex pause operation. 0 = Link partner is not capable of pause operation.	RO	0	—
9	100Base-T4 Capability	1 = Link partner is 100Base-T4 capable. 0 = Link partner is not 100Base-T4 capable.	RO	0	—
8	100Base-TX Full-Duplex Capable	1 = Link partner is 100Base-TX full-duplex capable. 0 = Link partner is not 100Base-TX full-duplex capable.	RO	0	—
7	100Base-TX Half-Duplex Capable	1 = Link partner is 100Base-TX half-duplex capable. 0 = Link partner is not 100Base-TX half-duplex capable.	RO	0	—
6	10Base-T Full-Duplex Capable	1 = Link partner is 10Base-T full-duplex capable. 0 = Link partner is not 10Base-T full-duplex capable.	RO	0	—
5	10Base-T Half-Duplex Capable	1 = Link partner is 10Base-T half-duplex capable. 0 = Link partner is not 10Base-T half-duplex capable.	RO	0	—
4:0	Protocol Selector Field	Link partner protocol selector field.	RO	0	—

Register Description (continued)

Register Functions/Settings (continued)

Table 22. Autonegotiation Expansion Register—Address 06

Autonegotiation Expansion Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:5	Reserved	—	RO	—	—
4	Parallel Detection Fault	1 = Parallel link fault detected. 0 = Parallel link fault not detected.	RO LH	0	—
3	Link Partner Next Page Ability	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	RO	0	—
2	Next Page Capability	1 = Local device has next page capability. 0 = Local device does not have next page capability.	RO LH	1	—
1	Page Received	1 = New page has been received from link partner. 0 = New page has not been received.	RO LH	0	—
0	Link Partner Autonegotiation Ability	1 = Link partner has autonegotiation capability. 0 = Link partner does not have autonegotiation capability.	RO	0	—

Table 23. Autonegotiation Next Page Transmit Register—Address 07

Autonegotiation Next Page Transmit Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	R/W	0	—
14	Reserved	—	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	1	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	1	—

Register Description (continued)

Register Functions/Settings (continued)

Table 24. Link Partner Next Page Register—Address 08

Link Partner Next Page Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Next Page	1 = Additional next pages follow. 0 = Sending last next page.	RO	0	—
14	Acknowledge	1 = Acknowledge. 0 = No acknowledge.	RO	0	—
13	Message Page	1 = Formatted page. 0 = Unformatted page.	R/W	0	—
12	Acknowledge 2	1 = Complies with message. 0 = Cannot comply with message.	R/W	0	—
11	Toggle	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one.	RO	0	—
10:0	Message/ Unformatted Code Field	Next page message code or unformatted data.	R/W	0	—

Register Description (continued)

Register Functions/Settings (continued)

Table 25. 1000 Base-T Control Register—Address 09

1000Base-T Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:13	Test Mode	000 = Normal mode. 001 = Test mode 1—transmit waveform test. 010 = Test mode 2—master transmit jitter test. 011 = Test mode 3—slave transmit jitter test (slave mode). 100 = Test mode 4—transmit distortion test. 101, 110, 111 = Reserved.	R/W	000	—
12	Master/Slave Configuration Enable	1 = Enable master/slave configuration. 0 = Automatic master/slave configuration.	R/W	0	1
11	Master/Slave Configuration Value	1 = Configure PHY as master. 0 = Configure PHY as slave.	R/W	1	1
10	Port Type	1 = Prefer multiport device (master). 0 = Prefer single-port device (slave).	R/W	1	1
9	Advertise 1000Base-T Full-duplex Capability	1 = Advertise 1000Base-T full-duplex capability. 0 = Advertise no 1000Base-T full-duplex capability.	R/W	1	1
8	Advertise 1000Base-T Half-duplex Capability	1 = Advertise 1000Base-T half-duplex capability. 0 = Advertise no 1000Base-T half-duplex capability.	R/W	1	1
7:0	Reserved	—	RO	9.7:0	—

1. Logically, bits 12:8 may be regarded as an extension of the technology ability field of register 4.

Register Description (continued)

Register Functions/Settings (continued)

Table 26. 1000Base-T Status Register—Address 10

1000Base-T Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Master/ Slave Configuration Fault	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	RO, LH, SC	0	1
14	Master/Slave Configuration Resolution	1 = Local PHY resolved to master. 0 = Local PHY resolved to slave.	RO	0	2
13	Local Receiver Status	1 = Local receiver okay. 0 = Local receiver not okay.	RO	0	—
12	Remote Receiver Status	1 = Remote receiver okay. 0 = Remote receiver not okay.	RO	0	—
11	Link Partner 1000Base-T Full-duplex Capability	1 = Link partner is capable of 1000Base-T full duplex. 0 = Link partner not 1000Base-T full-duplex capable.	RO	0	3
10	Link Partner 1000Base-T Half-duplex Capability	1 = Link partner is 1000Base-T half-duplex capable. 0 = Link partner not 1000Base-T half-duplex capable.	RO	0	3
9:8	Reserved	—	RO	—	—
7:0	Idle Error Count	MSB of idle error count.	RO	0	4

1. Once set, this bit remains set until cleared by the following actions:
   - Read of register 10 via the management interface.
   - Reset.
   - Completion of autonegotiation.
   - Enable of autonegotiation.
2. This bit is not valid when bit 15 is set.
3. Note that logically, bits 11:10 may be regarded as an extension of the technology ability field of register 5.
4. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and both local and remote receiver status are okay. The count is held at 255 in the event of overflow and is reset to zero by reading register 10 via the management interface or by reset.

Register Description (continued)

Register Functions/Settings (continued)

Table 27. Reserved Registers—Addresses 11—14

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Table 28. Extended Status Register—Address 15

Extended Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	1000Base-X Full-duplex	0 = Not 1000Base-X full-duplex capable.	RO	0	1
14	1000Base-X Half-duplex	0 = Not 1000Base-X half-duplex capable.	RO	0	—
13	1000Base-T Full-duplex	1 = 1000Base-T full-duplex capable. 0 = Not 1000Base-T full-duplex capable.	RO	1	—
12	1000Base-T Half-duplex	1 = 1000Base-T half-duplex capable. 0 = Not 1000Base-T half-duplex capable.	RO	1	—
11:0	Reserved	—	RO	0	—

1. 1000Base-X not supported.

Table 29. Reserved Registers—Addresses 16—17

Reserved Registers					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Reserved	—	—	—	—

Register Description (continued)

Register Functions/Settings (continued)

Table 30. PHY Control Register 2—Address 18

PHY Control Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reserved	—	—	—	—
14	Count False Carrier Events	1 = Rx error counter counts false carrier events. 0 = Rx error counter does not count false carrier events.	R/W	0	1
13	Count Symbol Errors	1 = Rx error counter counts symbol errors. 0 = Rx error counter counts CRC errors.	R/W	0	1
12:11	Reserved	—	—	—	—
10	Automatic MDI/MDI-X	1 = Enable automatic MDI/MDI-X detection. 0 = Disable automatic MDI/MDI-X detection.	R/W	1	—
9	MDI/MDI-X Configuration	1 = Manual MDI-X configuration. 0 = Manual MDI configuration.	R/W	1	See Table 31.
8:7	Reserved	—	—	—	—
6	SGMII Autone-gotiation Enable	1 = Enable SGMII autonegotiation. 0 = Disable SGMII autonegotiation.	R/W	1	—
5:3	Reserved	—	—	—	—
2	Enable Diagnostics	1 = Enable diagnostics. 0 = Disable diagnostics.	R/W	0	2
1:0	Reserved	—	—	—	—

1. Count symbol errors (18.13) and count false carrier events (18.14) control the type of errors that the Rx error counter (20.15:0) counts (settings are shown below). The default is to count CRC errors.

Count False Carrier Events	Count Symbol Errors	Rx Error Counter
1	1	Counts symbol errors and false carrier events.
1	0	Counts symbol errors.
0	1	Counts CRC errors and false carrier events.
0	0	Counts CRC errors.

2. This bit enables PHY diagnostics, which include IP phone detection and TDR cable diagnostics. It is not recommended to enable this bit in normal operation (when the link is active). This bit does not need to be set for link analysis cable diagnostics.

Register Description (continued)

Register Functions/Settings (continued)

Bit 9, PHY Control Register 2, manually sets the MDI/MDI-X configuration if automatic MDIX is disabled, as indicated below:

Table 31. MDI/MDI-X Configuration

Automatic MDI/MDI-X	MDI/MDI-X Configuration	MDI/MDI-X Mode
1	X	Automatic MDI/MDI-X detection.
0	0	MDI configuration (NIC/DTE).
0	1	MDI-X configuration (switch).

The mapping of the transmitter and receiver to pins for MDI and MDI-X configuration for 10Base-T, 100Base-TX and 1000Base-T is shown below. Note that even in manual MDI/MDI-X configuration, the PHY automatically detects and corrects for C and D pair swaps.

Table 32. MDI/MDI-X Pin Mapping

Pin	MDI Pin Mapping			MDI-X Pin Mapping		
	10Base-T	100Base-TX	1000Base-T	10Base-T	100Base-TX	1000Base-T
TDR_[0:7]_[0]+/–	Transmit +/–	Transmit +/–	Transmit A+/– Receive B+/–	Receive +/–	Receive +/–	Transmit B+/– Receive A+/–
TDR_[0:7]_[1]+/–	Receive +/–	Receive +/–	Transmit B+/– Receive A+/–	Transmit +/–	Transmit +/–	Transmit A+/– Receive B+/–
TDR_[0:7]_[2]+/–	—	—	Transmit C+/– Receive D+/–	—	—	Transmit D+/– Receive C+/–
TDR_[0:7]_[3]+/–	—	—	Transmit D+/– Receive C+/–	—	—	Transmit C+/– Receive D+/–

Register Description (continued)

Register Functions/Settings (continued)

Table 33. Loopback Control Register—Address 19

Loopback Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	MII Select	1 = MII loopback selected. 0 = MII loopback not selected.	R/W	1	1
14:13	Reserved	—	—	—	—
12	All Digital Select	1 = All digital loopback selected. 0 = All digital loopback not selected.	R/W	0	1
11	Replica Select	1 = Replica loopback selected. 0 = Replica loopback not selected.	R/W	0	1, 2
10	Line Driver Select	1 = Line driver loopback selected. 0 = Line driver loopback not selected.	R/W	0	1
9	Remote Enable	1 = Enable remote loopback. 0 = Disable remote loopback.	R/W	0	1, 3
8	SGMII Enable	1 = Enable SGMII loopback. 0 = Disable SGMII loopback.	R/W	0	1, 4
7	External Cable Enable	1 = Enable external cable loopback. 0 = Disable external cable loopback.	R/W	0	1
6	Tx Suppression	1 = Suppress Tx during SGMII or all digital loopback. 0 = Do not suppress Tx during SGMII or all digital loopback.	R/W	1	—
5:2	Reserved	—	—	—	—
1	Comma Enable	1 = Enable COMMA detection in SGMII loopback. 0 = Disable COMMA detection in SGMII loopback.	R/W	1	—
0	Force Link Status	1 = Force link status OK in MII loopback. 0 = Force link status Not OK in MII loopback.	R/W	0	5

1. MII, all digital, replica, and line driver-select bits select the loopback mode when the loopback bit, 0.14, is set. Remote, SGMII, and external cable enable bits enable a loopback mode independent of the loopback bit, 0.14. These three loopbacks are very close to normal PHY operation.
2. Replica loopback is not available in 10Base-T.
3. In remote loopback, SGMII Tx data is ignored.
4. SGMII loopback can also be used while the PHY is connected with a remote link partner. In SGMII loopback, the link status is set when the link comes up with a remote link partner.
5. This bit can be used to force link status OK during MII loopback. In MII loopback, the link status bit will not be set unless force link status is used. In all other loopback modes, the link status bit will be set when the link comes up.

Register Description (continued)

Register Functions/Settings (continued)

Table 34. RX Error Counter Register—Address 20

RX Error Counter Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:0	Rx Error Counter	16-bit Rx error counter.	RO, SC	0	1

Table 35. Management Interface (MI) Control Register—Address 21

Management Interface (MI) Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:3	Reserved	—	—	—	—
2	Ignore 10G Frames	1 = Management frames with ST = <00> are ignored. 0 = Management frames with ST = <00> are treated as wrong frames.	R/W	1	—
1	Reserved	—	—	—	—
0	Preamble Suppression Enable	1 = MI preamble is ignored. 0 = MI preamble is required.	R/W	1	—

Register Description (continued)

Register Functions/Settings (continued)

Table 36. PHY Configuration Register—Address 22

PHY Configuration Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	Reserved	—	—	—	—
13:12	TX FIFI depth (1000Base-T)	00 = ±8. 01 = ±16. 10 = ±24. 11 = ±32.	R/W	01	—
11:10	Automatic Speed Downshift Mode	00 = Disable automatic speed downshift. 01 = 10Base-T downshift enabled. 10 = 100Base-TX downshift enabled. 11 = 100Base-TX and 10Base-T enabled.	R/W	11	1
9:8	Reserved	—	—	—	—
7	Alternate Next-Page	1 = Enables manual control of 1000Base-T next pages only. 0 = Normal operation of 1000Base-T next page exchange.	R/W	0	—
6	Group MDIO Mode Enable	1 = Enable group MDIO mode. 0 = Disable Group MDIO mode.	R/W	0	2
5	Transmit Test Clock Enable	1 = Enable output of 1000Base-T transmit clock. 0 = Disable output.	R/W	0	3
4:0	Reserved	—	—	—	—

1. If automatic speed downshift is enabled and the PHY fails to autonegotiate at 1000Base-T, the PHY will fall back to attempt connection at 100Base-TX and, subsequently, 10Base-T. This cycle will repeat. If the link is broken at any speed, the PHY will restart this process by reattempting connection at the highest possible speed (e.g., 1000Base-T).
2. If group MDIO is enabled, this port will respond to all writes to port 31. This is useful for global register programming.
3. The transmit test clock is available on pin TX_TCLK_0 for ports 0 to 3 and on pin TX_TCLK_1 for ports 4 to 7.

Register Description (continued)

Register Functions/Settings (continued)

Table 37. PHY Control Register—Address 23

PHY Control Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	IP Phone Detected	1 = IP phone detected. 0 = IP phone not detected.	RO, LH	0	1
14	IP Phone Detect Enable	1 = Enable automatic IP phone detect. 0 = Disable automatic IP phone detect.	R/W,	0	2
13	Cable Diagnostic Mode	1 = Link analysis mode. 0 = TDR mode.	R/W	$\overline{\text{TDR\_SEL}}$	3
12:11	Automatic Speed Downshift Attempts Before Downshift	00 = 1. 01 = 2. 10 = 3. 11 = 4.	R/W	01	—
10	SGMII Data Output Enable	1 = Enable SGMII data outputs. 0 = Disable SGMII data outputs.	R/W	1	—
9	SGMII RXCLK Enable	1 = Enable SGMII RXCLK. 0 = Disable SGMII RXCLK.	R/W	1	—
8	Reserved	—	—	—	—
7	Link Partner Detected	1 = Link partner detected. 0 = Link partner not detected	RO, LH	0	4
6	Reserved	—	—	—	—
5	Jabber (10Base-T)	1 = Disable jabber. 0 = Normal operation.	R/W	0	—
4	SQE (10Base-T)	1 = Enable heartbeat. 0 = Disable heartbeat.	R/W	0	—
3	TP_LOOPBACK (10Base-T)	1 = Disable TP loopback during half-duplex. 0 = Normal operation.	R/W	1	—
2	Preamble Generation Enable	1 = Enable preamble generation for 10Base-T. 0 = Disable preamble generation for 10Base-T.	R/W	1	—
1	Reserved	—	—	—	—
0	Force Interrupt	1 = Assert MDINT_N pin. 0 = Deassert MDINT_N pin.	R/W	0	—

1. This bit is only valid when the PHY in PHY standby mode (26.15 = 1) and when IP phone detect is enabled (23.14 = 1).
2. When this bit is set, the PHY performs automatic IP phone detection whenever the PHY is in standby mode. The PHY can be put in standby by disabling linking (23.13 = 0). If an IP phone is detected it is indicated in 23.15.
3. This bit sets the cable diagnostics mode. The default is link analysis mode wherein the PHY brings up a link with a remote partner. For analysis of cable faults and IP phone detection, the PHY can be put in TDR mode, which enables it to find cable faults such as opens and shorts. When the PHY is put into TDR mode, the PHY disables any active link, does not respond to link pulses from a remote link partner, and will not bring up a link. The default cable diagnostic mode is set at reset by the TDR_SEL pin.
4. When the PHY is in standby, it automatically monitors for the appearance of a link partner and sets this bit if detected. The PHY can be put in standby by disabling linking (23.13 = 0).

Register Description (continued)

Register Functions/Settings (continued)

Table 38. Interrupt Mask Register—Address 24

Interrupt Mask Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:11	Reserved	—	—	—	—
10	TDR/IP Phone	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
9	MDIO Sync Lost	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
8	Autonegotiation Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
7	CRC Error	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
6	Next Page Received	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
5	Error Counter Full	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
4	FIFO Overflow/ Underflow	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
3	Receive Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
2	Link Status Change	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
1	Automatic Speed Downshift	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—
0	Interrupt Enable	1 = Interrupt enabled. 0 = Interrupt disabled.	R/W	0	—

Register Description (continued)

Register Functions/Settings (continued)

Table 39. Interrupt Status Register—Address 25

Interrupt Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:11	Reserved	—	—	—	—
10	TDR/IP Phone	1 = Event has completed. 0 = Event has not completed.	RO, SC	0	—
9	MDIO Sync Lost	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	1
8	Autonegotiation Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
7	CRC Error	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
6	Next Page Received	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
5	Error Counter Full	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
4	FIFO Overflow/ Underflow	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
3	Receive Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
2	Link Status Change	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
1	Automatic Speed Downshift	1 = Event has occurred. 0 = Event has not occurred.	RO SC	0	—
0	MII Interrupt Pending	1 = Interrupt pending. 0 = No interrupt pending.	RO SC	0	2

1. If the management frame preamble is suppressed (MF preamble suppression, register 0, bit 6), it is possible for the PHY to lose synchronization if there is a glitch at the interface. The PHY can recover if a single frame with a preamble is sent to the PHY. The MDIO sync lost interrupt can be used to detect loss of synchronization and thus enable recovery.
2. The MII interrupt pending bit is not masked by interrupt enable bit (interrupt mask register, address 24 bit 0). This bit is inverted and provided as an output on MDINT_N, gated by interrupt enable bit.

Register Description (continued)

Register Functions/Settings (continued)

Table 40. PHY Status Register—Address 26

PHY Status Register					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	PHY in Standby Mode	1 = PHY in standby mode. 0 = PHY **not** in standby mode.	R0	1	1
14:13	Autonegotiation Fault Status	10 = Master/slave autonegotiation fault. 01 = Parallel detect autonegotiation fault. 00 = No autonegotiation fault.	RO	00	—
12	Autonegotiation Status	1 = Autonegotiation is complete. 0 = Autonegotiation not complete.	RO	0	—
11	MDI-X Status	1 = MDI-X configuration. 0 = MDI configuration.	RO	0	—
10	Polarity Status	1 = Polarity is normal (10Base-T only). 0 = Polarity is inverted (10Base-T only).	RO	1	—
9:8	Speed Status	11 = Undetermined. 10 = 1000Base-T. 01 = 100Base-TX. 00 = 10Base-T.	RO	11	—
7	Duplex Status	1 = Full duplex. 0 = Half duplex.	RO	0	—
6	Link Status	1 = Link is up. 0 = Link is down.	RO	0	—
5	Transmit Status	1 = PHY is transmitting a packet. 0 = PHY is not transmitting a packet.	RO	0	—
4	Receive Status	1 = PHY is receiving a packet. 0 = PHY is not receiving a packet.	RO	0	—
3	Collision Status	1 = Collision is occurring. 0 = Collision not occurring.	RO	0	—
2	Autonegotiation Enabled	1 = Both partners have autonegotiation enabled. 0 = Both partners do not have autonegotiation enabled.	RO	0	—
1	PAUSE Enabled	1 = Link partner advertised PAUSE mode enabled. 0 = Link partner advertised PAUSE mode disabled.	RO	0	—
0	Asymmetric Direction	1 = Link partner advertised direction is symmetric. 0 = Link partner advertised direction is asymmetric.	RO	0	—

1. This bit indicates that the PHY is in standby mode and is ready to perform IP phone detection or TDR cable diagnostics. The PHY enters standby mode when cable diagnostic TDR mode is selected (23.13 = 0) and the link is dropped. A software reset (0.15) or software power down (0.11) can be used to force the link to drop.

Register Description (continued)

Register Functions/Settings (continued)

Table 41. LED Control Register 1—Address 27

LED Control Register 1					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Two-Color Mode LEDs CD	1 = Two-color mode for LED_C and LED_D. 0 = Normal mode for LED_C and LED_D.	R/W	0	1
14	Two-Color Mode LEDs AB	1 = Two-color mode for LED_A and LED_B. 0 = Normal mode for LED_A and LED_B.	R/W	0	1
13	LED_B Extended Modes	1 = Extended modes for LED_B. 0 = Standard modes for LED_B.	R/W	0	2
12	LED_A Extended Modes	1 = Extended modes for LED_A. 0 = Standard modes for LED_A.	R/W	0	2
11	LED_D Extended Modes	1 = Extended modes for LED_D. 0 = Standard modes for LED_D.	R/W	0	2
10	LED_C Extended Modes	1 = Extended modes for LED_C. 0 = Standard modes for LED_C.	R/W	0	2
9:8	Reserved	—	—	—	—
7:4	LED Blink Pattern Pause	LED blink pattern pause cycles.	R/W	0x0	—
3:2	LED Pulse Duration	00 = Stretch LED events to 28 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00	—
1	LED Outputs Disable	1 = Direct-drive LED outputs disabled. 0 = Direct-drive LED outputs enabled.	R/W	0	—
0	Pulse Stretch 0	1 = Enable pulse stretching of LED functions: transmit activity, receive activity, and collision. 0 = Disable pulse stretching of LED functions: transmit activity, receive activity, and collision.	R/W	1	—

1. If two-color mode is enabled for pair A and B, the signal output for LED_A is equal to (LED_A and $\overline{\text{LED\_B}}$). For the case where LED_A and LED_B are not mutually exclusive (e.g., duplex and collision), this mode can simplify the external circuitry because it ensures either LED_A or LED_B is on, and not both at the same time. The same rule applies to pair C and D.
2. The LED function is programmed using this bit and register 28.

Register Description (continued)

Register Functions/Settings (continued)

Table 42. LED Control Register 2—Address 28

LED Control Register 2					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:12	LED_B	**Standard modes, (27.13 = 0)**: 0000 = 1000Base-T. 0001 = 100Base-TX. 0010 = 10Base-T. 0011 = 1000Base-T on, 100Base-TX blink. 0100 = Link established. 0101 = Transmit. 0110 = Receive. 0111 = Transmit or receive activity. 1000 = Full duplex. 1001 = Collision. 1010 = Link established (on) and activity (blink). 1011 = Link established (on) and receive (blink). 1100 = Full duplex (on) and collision (blink). 1101 = Blink. 1110 = On. 1111 = Off. **Extended modes, (27.13 = 1)**: 0000 = 10BASE-T or 100BASE-TX. 0001 = 100BASE-TX or 1000BASE-T. 0010 = 10BASE-T (on) and activity (blink). 0011 = 100BASE-TX (on) and activity (blink). 0100 = 1000BASE-T (on) and activity (blink). 0101 = 10BASE-T or 100BASE-TX (on) and activity (blink). 0110 = 100BASE-TX or 1000BASE-T (on) and activity (blink). 0111 = 10BASE-T or 1000BASE-T. 1000 = 10BASE-T or 1000BASE-T (on) and activity (blink). 1xxx = Reserved.	R/W	0111	—
11:8	LED_A	As per 15:12. (Extended modes, 27.12 = 1.)	R/W	0100	—
7:4	LED_D	As per 15:12. (Extended modes, 27.11 = 1.)	R/W	0001	—
3:0	LED_C	As per 15:12. (Extended modes, (27.10 = 1.)	R/W	0000	—

Table 43. LED Control Register 3—Address 29

LED Control Register 3					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	LED Blink Pattern Address	Select LED blink pattern register set. 00 = Select register set for LED A. 01 = Select register set for LED B. 10 = Select register set for LED C. 11 = Select register set for LED D.	R/W	00	—
13:8	LED Blink Pattern Frequency	LED blink pattern clock frequency divide ratio.	R/W	0x1f	1
7:0	LED Blink Pattern	LED blink pattern.	R/W	0x55	1

1. The default pattern is a 512 ms blink.

Register Description (continued)

Register Functions/Settings (continued)

Table 44. Cable Diagnostic Control Register (TDR Mode)—Address 30

Cable Diagnostic Control Register (TDR Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	TDR Request	11 = Automatic TDR analysis in progress. 10 = Single-pair TDR analysis in progress. 01 = TDR analysis complete, results valid. 00 = TDR analysis complete, results invalid.	R/W, SC	00	1
13:12	TDR Tx Dim	Transmit dimension for single-pair TDR analysis/ first dimension to be reported for automatic TDR analysis: 00 = TDR transmit on pair A. 01 = TDR transmit on pair B. 10 = TDR transmit on pair C. 11 = TDR transmit on pair D.	R/W	00	2
11:10	TDR Rx Dim	Receive dimension for single-pair TDR analysis: 00 = TDR receive on pair A. 01 = TDR receive on pair B. 10 = TDR receive on pair C. 11 = TDR receive on pair D.	R/W	00	3
9:0	Reserved	—	—	—	—

1. Automatic TDR analysis is enabled by setting TDR request to {11}. All ten combinations of pairs are analyzed in sequence, and the results are available in register 31. TDR analysis for a single pair combination can be enabled by setting TDR request to {10}. The PHY must be in cable diagnostic TDR mode (23.13 = 0) and IP phone detect must be disabled (23.14 = 0) to do TDR operations. Bit 15 self-clears when the TDR operation is complete. When TDR is complete, bit 14 indicates if the results are valid.
2. The TDR transmit dimension is only valid for single-pair TDR analysis. For automatic TDR analysis, these bits specify the first dimension to be reported in register 31.
3. The TDR receive dimension is only valid for single-pair TDR analysis. It is ignored for automatic TDR analysis when all ten pair combinations are analyzed.

Register Description (continued)

Register Functions/Settings (continued)

Table 45. Cable Diagnostic Status Register (TDR Mode)—Address 31

Cable Diagnostic Status Register (TDR Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15:14	TDR Fault Type Pair X	11 = Result invalid. 10 = Open or short found on pair X. 01 = Strong impedance mismatch found on pair X. 00 = Good termination found on pair X.	R0	11	1, 2, 3
13	Short Between Pairs X and D	1 = Short between pairs X and D. 0 = No short between pairs X and D.	RO	0	4
12	Short Between Pairs X and C	1 = Short between pairs X and C. 0 = No short between pairs X and C.	RO	0	4
11	Short Between Pairs X and B	1 = Short between pairs X and B. 0 = No short between pairs X and B.	RO	0	4
10	Short Between Pairs X and A	1 = Short between pairs X and A. 0 = No short between pairs X and A.	RO	0	4
9:2	Distance to Fault	Distance to first open, short, or SIM fault on pair X.	RO	0	5, 6
1:0	Pair Indication	00 = Results are for pair A. 01 = Results are for pair B. 10 = Results are for pair C. 11 = Results are for pair D.	RO	00	7

1. The first time this register is read after automatic TDR analysis has completed, it indicates the fault type for pair A. The second time it is read, it indicates the fault type for pair B; the third, for pair C; and the fourth time, for pair D. It then cycles back to pair A. Pair indication bits 31.1:0 indicate pair to which the results correspond. Bits 30.13:12 can be used to specify a pair other than pair A as the first dimension to be reported.
2. A value of 01 indicates either an open or a short. If 31.13:10 = 0000, it is an open. For all other values of 31.13:10, each bit indicates a short to pair A, B, C and D.
3. A value of 11 indicates that the results for this pair are invalid. An invalid result usually occurs when unexpected pulses are received during the TDR operation, e.g. , from a remote PHY also doing TDR or trying to bring up a link. When an invalid result is indicated, the distance in bits 31.9:2 will be 0xff and should be ignored.
4. The first time these bits are read after automatic TDR analysis has completed, they indicate a short between pair A and pair A, B, C and D, respectively. The second time they are read, they indicate a short between pair B and pair A, B, C and D, respectively. The third time, with pair C; and the fourth time, with pair D. It then cycles back to pair A. Pair indication bits 31.1:0 indicate to which pair the results correspond. Bits 30.13:12 can be used to specify a pair other than pair A as the first dimension to be reported.
5. The first time this register is read after automatic TDR analysis has completed, it indicates the distance to the first fault on pair A. The second time it is read, it indicates the distance to the first fault on pair B; the third time, on pair C; and the fourth time, on pair D. It then cycles back to pair A. Pair indication bits 31.1:0 indicate to which pair the results correspond. Bits 30.13:12 can be used to specify a pair other than pair A as the first dimension to be reported.
6. This 8-bit integer value is the distance in meters. The value 0xff indicates an unknown result.
7. This indicates to which pair the results in register 31.15:2 correspond .

Register Description (continued)

Register Functions/Settings (continued)

Table 46. Cable Diagnostic Status Register (Link Analysis Mode)—Address 31

Cable Diagnostic Status Register (Link Analysis Mode)					
Bit	**Name**	**Description**	**Type**	**Default**	**Notes**
15	Reserved	—	—	—	—
14	Pair Swap on Pairs C and D	1 = Pairs C and D are swapped (1000Base-T only). 0 = Pairs C and D are not swapped (1000Base-T only).	RO	0	1
13	Polarity on Pair D	1 = Polarity on pair D is normal (1000Base-T only). 0 = Polarity on pair D is inverted (1000Base-T only).	RO	0	—
12	Polarity on Pair C	1 = Polarity on pair C is normal (1000Base-T only). 0 = Polarity on pair C is inverted (1000Base-T only).	RO	0	—
11	Polarity on Pair B	1 = Polarity on pair B is normal (10Base-T or 1000Base-T). 0 = Polarity on pair B is inverted (10Base-T or 1000Base-T).	RO	0	—
10	Polarity on Pair A	1 = Polarity on pair A is normal (10Base-T or 1000Base-T). 0 = Polarity on pair A is inverted (10Base-T or 1000Base-T).	RO	0	—
9:2	Cable Length	Cable length when the link is active.	RO	0	2
1	Reserved	—	—	—	—
0	Excessive Pair Skew	1 = Excessive pair skew (1000Base-T only). 0 = Not excessive pair skew (1000Base-T only).	RO	0	3

1. If this bit is set, the PHY has detected that received pair 2 (RJ-45 pins 4 and 5) and pair 3 (RJ-45 pins 7 and 8) have been crossed over.
2. This 8-bit integer value is the cable length in meters when the link is active. The value 0xff indicates an unknown result.
3. Excessive pair skew in 1000Base-T is detected by detecting that the scrambler has not acquired and a 1000Base-T link cannot be brought up. In this case, the PHY will usually fall back to 100Base-TX or 10Base-T. It is possible for other scrambler acquisition errors to be mistaken for excessive pair skew.

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 47. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	—	4.2	V
Supply Voltage (1.0 V analog)	AV_{DDL}	—	1.2	V
Supply Voltage (2.5 V digital)	DV_{DDIO}	—	4.2	V
Supply Voltage (1.0 V digital)	V_{DD}	—	1.2	V
ESD Protection	V_{ESD}	—	2000	V
Storage Temperature	T_{STORE}	–40	125	°C

Recommended Operating Conditions

Table 48. ET1081N0 Recommended Operating Conditions*

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	2.38	2.5	2.62	V
Supply Voltage (1.0 V analog)	AV_{DDL}	0.95	1.0	1.05	V
Supply Voltage (2.5 V digital)	DV_{DDIO}	2.38	2.5	2.62	V
Supply Voltage (1.0 V digital)	V_{DD}	0.95	1.0	1.05	V
Ambient Operating Temperature	T_A	0	—	70	°C
Maximum Junction Temperature	T_J	0	—	125	°C
Thermal Characteristics, 388-PBGA (JDEC 3 in. x 4.5 in. 4-layer PCB):	T_{JB} T_{JC} ψ_{JT}	— — —	10.07 5.43 5.43	— — —	°C/W
0 m/s Airflow	T_{JA}	—	16.93	—	
1 m/s Airflow	T_{JA}	—	13.63		
2.5 m/s Airflow	T_{JA}	—	12.13	—	

* The ET1081 is available in 1.0 V and 1.1 V versions.

Electrical Specifications (continued)

Recommended Operating Conditions (continued)

Table 49. ET1081N1 Recommended Operating Conditions*

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	AV_{DDH}	2.38	2.5	2.62	V
Supply Voltage (1.0 V analog)	AV_{DDL}	1.05	1.1	1.15	V
Supply Voltage (2.5 V digital)	DV_{DDIO}	2.38	2.5	2.62	V
Supply Voltage (1.0 V digital)	V_{DD}	1.05	1.1	1.15	V
Ambient Operating Temperature	T_A	0	—	70	°C
Maximum Junction Temperature	T_J	0	—	125	°C
Thermal Characteristics, 388-PBGA (JDEC 3 in. x 4.5 in. 4-layer PCB):	T_{JB} T_{JC} ψ_{JT}	— — —	10.07 5.43 5.43	— — —	°C/W
0 m/s Airflow	T_{JA}	—	16.93	—	
1 m/s Airflow	T_{JA}	—	13.63		
2.5 m/s Airflow	T_{JA}	—	12.13	—	

* The ET1081 is available in 1.0 V and 1.1 V versions.

Electrical Specifications (continued)

Device Electrical Characteristics

Device electrical characteristics refer to the behavior of the device under specified conditions imposed on the user for proper operation of the device. Unless otherwise noted, the parameters below are valid for the conditions described in the previous section, Recommended Operating Conditions.

Table 50. Device Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage Range (LVDS input pins)	V_I	—	675	—	1725	mV
Input Differential Threshold (LVDS input pins)	V_{IDTH}	—	–50	—	+50	mV
Output Low Voltage (LVDS output pins)	V_{OL}	—	875	—	—	mV
Output High Voltage (LVDS output pins)	V_{OH}	—	—	—	1525	mV
Output Differential Voltage (LVDS output pins)	$\|V_{OD}\|$	—	150	—	400	mV
Output Ringing (LVDS output pins)	V_{RING}	—	—	—	10	%
Output Offset Voltage (LVDS output pins)	V_{OS}	—	1075	—	1325	mV
Output Impedance (differential)	R_O	—	80	—	120	Ω
Input Low Voltage (all other digital input pins)	V_{IL}	—	–0.2	—	0.7	V
Input High Voltage (CLK_LVDS, RESET_N, and TDR_SEL pins)	V_{IH}	—	1.7	—	2.7	V
Input High Voltage (all other digital input pins)	V_{IH}	—	1.7	—	3.6	V
Output Low Voltage (all other digital output pins)	V_{OL}	—	—	—	0.4	V
Output High Voltage (all other digital output pins)	V_{OH}	—	2.0	—	—	V
Differential Output Voltage (analog MDI pins 1000BaseT-T)	V_{ODIFF}	—	0.67	0.75	0.82	V
Differential Output Voltage (analog MDI pins 100Base-TX)	V_{ODIFF}	—	0.95	1.0	1.05	V
Differential Output Voltage (analog MDI pins 10Base-T)	V_{ODIFF}	—	2.2	2.5	2.8	V
Bias Voltage	V_{BIAS}	—	—	1.2	—	V

Table 51. ET1081N0 Current Consumption SGMII 1000Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 52. ET1081N0 Current Consumption SGMII 100Base-TX

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Table 53. ET1081N0 Current Consumption SGMII 10Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Table 54. ET1081N1 Current Consumption SGMII 1000Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Electrical Specifications (continued)

Device Electrical Characteristics (continued)

Table 55. ET1081N1 Current Consumption SGMII 100Base-TX

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Table 56. ET1081N1 Current Consumption SGMII 10Base-T

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage (2.5 V analog)	I_{AVDDH}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V analog)	I_{AVDDL}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (2.5 V digital)	I_{DVDDIO}	Tx/Rx random data	—	TBD	—	mA
Supply Voltage (1.0 V digital)	I_{VDD}	Tx/Rx random data	—	TBD	—	mA
Center Tap Voltage (1.8 V analog)	I_{CTAP}	Tx/Rx random data	—	TBD	—	mA

Timing Specification

SGMII 1000Base-T Receive Timing

Receive timing covers SGMII data launched from the PHY and captured by the MAC. The ET1081 implements a 6-pin interface with source synchronous clocking on the receive pair.

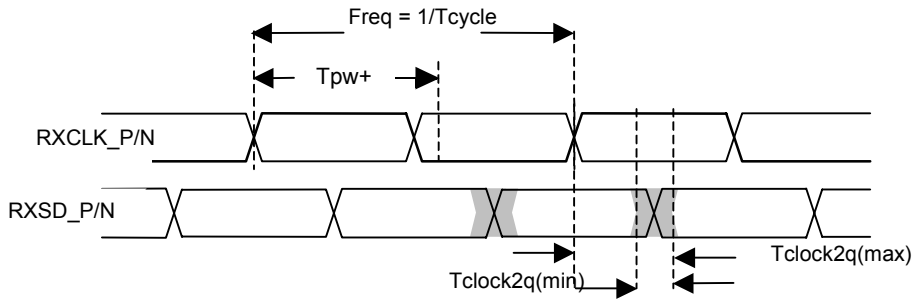


Figure 14. SGMII 1000Base-T Receive Timing

Table 57. SGMII 1000Base-T Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
Freq	RXCLK Frequency (center = 625 MHz)	–100	—	100	ppm
Freq	Data Frequency (1250 Mbits/s nominal)	–100	—	100	ppm
Clock	RXCLK Duty Cycle (Tpw+/Tcycle)	48	—	52	%
Trise	Trise (20%—80%)	100	—	200	ps
Tfall	Tfall (80%—20%)	100	—	200	ps
Tskew1	Skew Between P and N of Differential Signal	—	—	50	ps
Tclock2q	Skew Between Clock and Data	250	—	550	ps
RXSD_P/N$_{JITTER}$	RXSD_P/N Timing Jitter (inclusive of P/N skew)	—	140	—	ps
RXCLK_P/N$_{JITTER}$	RXCLK_P/N Timing Jitter (inclusive of P/N skew)	—	140	—	ps

Timing Specification (continued)

SGMII 1000Base-T Transmit Timing (continued)

Transmit timing covers SGMII data launched from the MAC and captured by the PHY. The ET1081 implements a 6-pin interface using a CDR to self-align the data and extract the clock from the MAC, resulting in only a transmit data input with no transmit clock input.

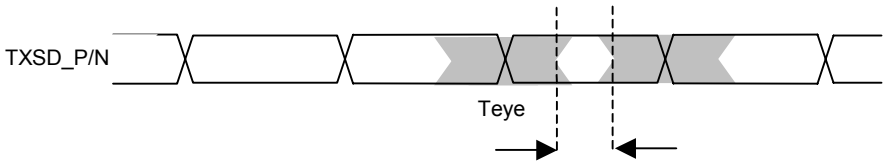


Figure 15. SGMII 1000Base-T Transmit Timing

Table 58. SGMII 1000Base-T Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Data Frequency (1250 Mbits/s nominal)	–100	—	100	ppm
Teye	Valid Data Eye*	—	—	300	ps

* The PHY is guaranteed to properly recover the MAC transmit data with a valid data-eye opening of no more than 300 ps.

Timing Specification (continued)

Serial Management Interface Timing

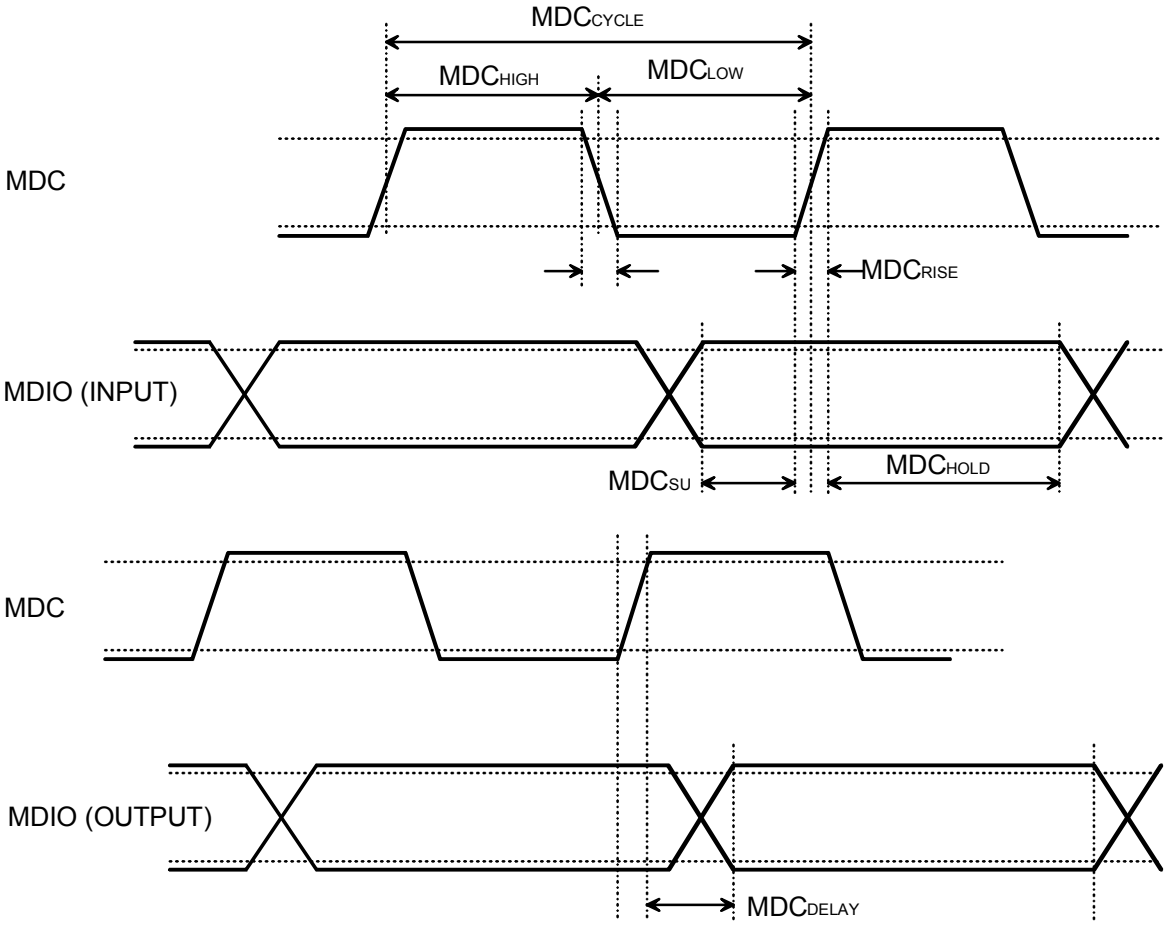


Figure 16. Serial Management Interface Timing

Table 59. Serial Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
MDC_{CYCLE}	MDC Cycle Time	125	—	—	ns
MDC_{HIGH}	MDC High Time	50	—	—	ns
MDC_{LOW}	MDC Low Time	50	—	—	ns
MDC_{RISE}	MDC Rise Time	—	—	5	ns
MDC_{FALL}	MDC Fall Time	—	—	5	ns
MDC_{SU}	MDIO Signal Setup Time to MDC	10	—	—	ns
MDC_{HOLD}	MDIO Signal Hold Time to MDC	10	—	—	ns
MDC_{DELAY}	MDIO Delay Time from MDC	—	—	80	ns

Timing Specification (continued)

Reset Timing

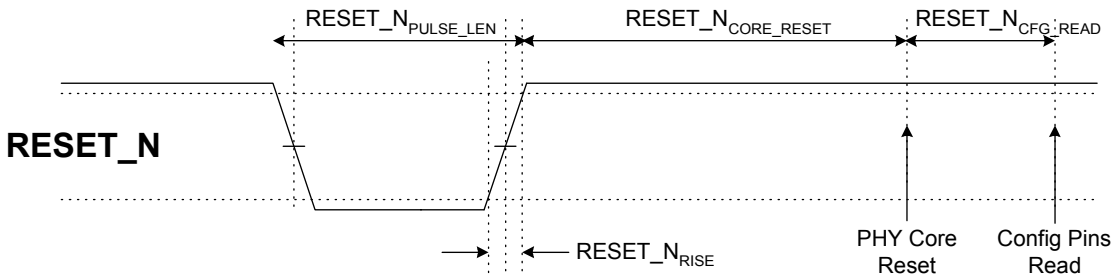


Figure 17. Reset Timing

Table 60. Reset Timing

Symbol	Parameter	Min	Typ	Max	Unit
RESET_N$_{PULSE_LEN}$	RESET_N Pulse Length	20	—	—	µs
RESET_N$_{RISE}$	RESET_N Rise Time	—	1.0	—	ns
RESET_N$_{CORE_RESET}$	RESET_N Deassertion to PHY Core Reset	—	—	5.0	ms
RESET_N$_{CFG_READ}$	PHY Core Reset to Configuration Read	576	—	1008	ns

Timing Specification (continued)

Input Clock Timing

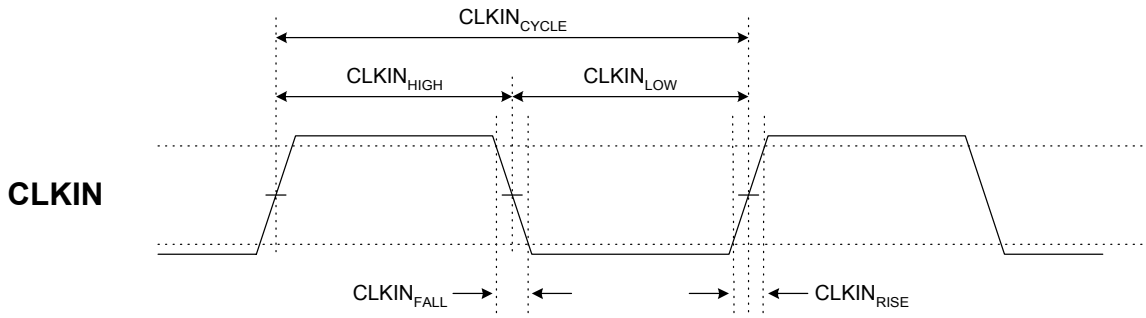


Figure 18. Input Clock Timing

Table 61. Input Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit
CLKINCYCLE	CLKIN Cycle Time	39.998	40	40.002	ns
CLKINHIGH	CLKIN High Time	15	20	25	ns
CLKINLOW	CLKIN Low Time	15	20	25	ns
CLKINRISE	CLKIN Rise Time	—	—	3	ns
CLKINFALL	CLKIN Fall Time	—	—	3	ns
—	CLKIN Input Clock Jitter (RMS)	—	—	20	ps
—	CLKIN Input Clock Frequency	—	25	—	MHz
—	CLKIN Input Clock Accuracy	—	—	50	ppm

Timing Specification (continued)

JTAG Timing

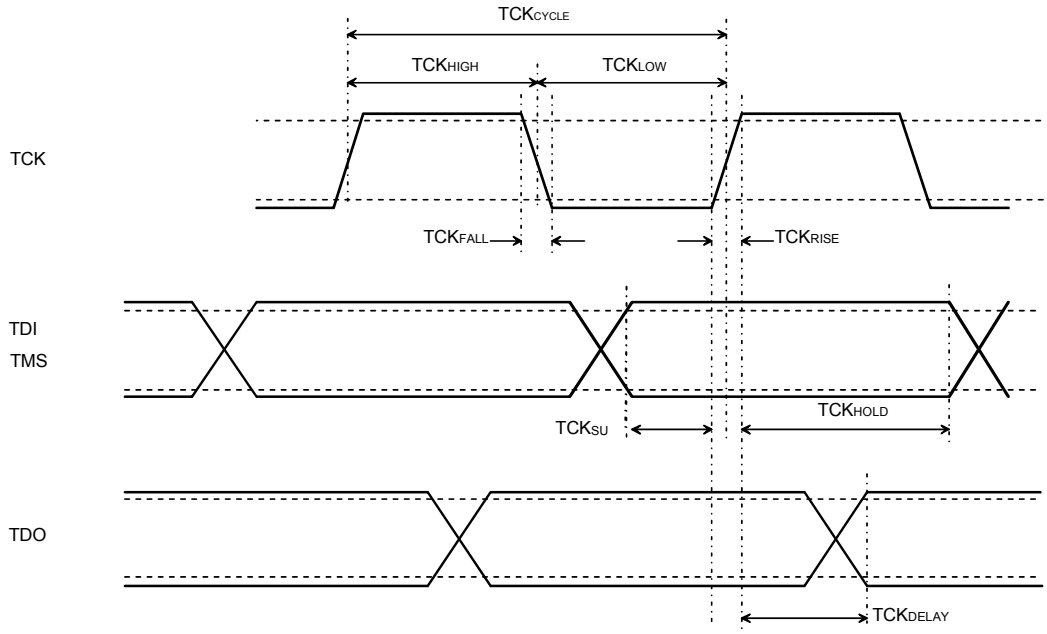
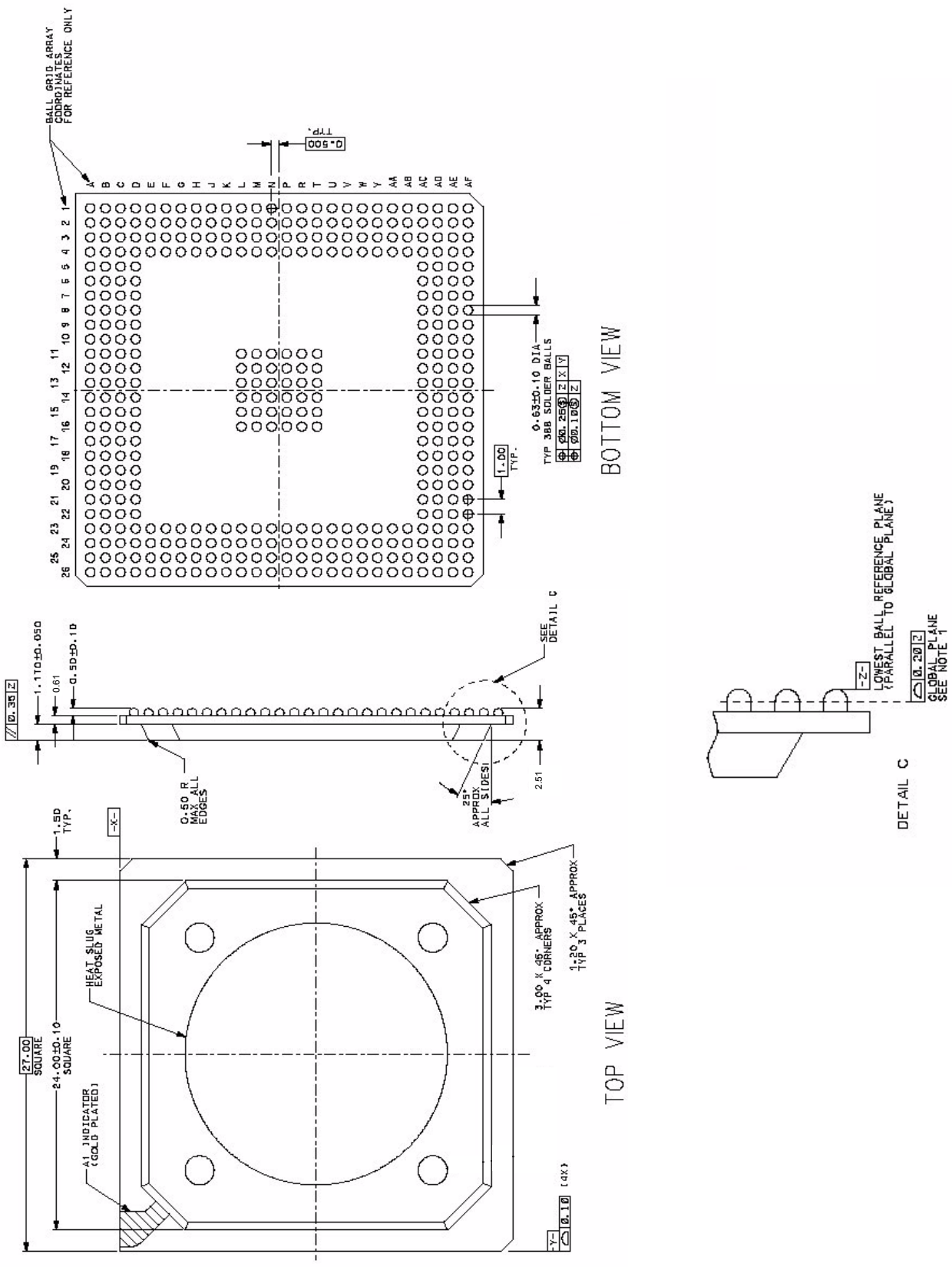


Figure 19. JTAG Timing

Table 62. JTAG Timing

Symbol	Parameter	Min	Typ	Max	Unit
TCK_{CYCLE}	TCK Cycle Time	20	—	—	ns
TCK_{HIGH}	TCK High Time	10	—	—	ns
TCK_{LOW}	TCK Low Time	10	—	—	ns
TCK_{RISE}	TCK Rise Time	—	1	—	ns
TCK_{FALL}	TCK Fall Time	—	1	—	ns
TCK_{SU}	TDI, TMS Setup Time to TCK	2.7	—	—	ns
TCK_{HOLD}	TDI, TMS Hold Time to TCK	0.8	—	—	ns
TCK_{DELAY}	TDO Delay Time from TCK	—	—	8.1	ns

Package Diagram (Package outlines are unofficial and for reference only. Unless otherwise specified, all dimensions are in millimeters.)



Ordering Information

Table 63. Ordering Information

Device	Description	Package	Part Number	Comcode
ET1081	Lead-Free Gigabit Ethernet Octal PHY (1.1 V Core)	388-pin PBGA	L-ET1081N1C-B-DB	711009618
	Octal Evaluation Board	—	ET1081B-EVB	700079682

Related Documentation

Table 64. Related Documentation

Device	Description	Document Type
ET1011	Gigabit Ethernet Transceiver	Product Brief Data Sheet Application Note
ET1310	Gigabit Ethernet Controller	
ET1081	Gigabit Ethernet Octal PHY	Product Brief Data Sheet
ET2008-50	Gigabit Ethernet Octal Switch and PHY	Data Sheet
ET2008-50/40/30	Gigabit Ethernet Octal Switch and PHY	Product Brief
ET2005-50/40/30	Gigabit Ethernet Five-Port Switch and PHY	Product Brief
ET3028-50	Single-Chip 28 x 1 Gbit/s Layer 2 Ethernet Switch	Product Brief Data Sheet Application Note
ET3048-50	Single-Chip 48 x 1 Gbit/s Layer 2 Ethernet Switch	
ET4028-50	Single-Chip 28 x 1 Gbit/s Layer 2+ Ethernet Switch	
ET4048-50	Single-Chip 48 x 1 Gbit/s Layer 2+ Ethernet Switch	
ET4128-50	Single-Chip 28 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	
ET4148-50	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2+ Ethernet Switch	
ET5028-50	Single-Chip 28 x 1 Gbit/s Layer 2/3 Ethernet Switch	Product Brief
ET5048-50	Single-Chip 48 x 1 Gbit/s Layer 2/3 Ethernet Switch	
ET5128-50	Single-Chip 28 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	
ET5148-50/60/70	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	
ET5148-50	Single-Chip 48 x 1 Gbit/s + 2 x 10 Gbits/s Layer 2/3 Ethernet Switch	Data Sheet

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