3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications of the 21040. The test conditions for the specified values are as follows unless otherwise indicated:

- Temperature (Ta): 70°C
- Power supply voltage (VDD): 3.3 V
- Power supply voltage (VDDAC): 3.3 V
- Reference voltage (VDD_CLAMP): 3.3 V or 5.0 V
- Ground (VSS): 0 V

3.1 Voltage Limit Ratings

Table 9 lists the voltage limit ratings.

Table 9 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.135 V	+3.465 V
VDD_CLAMP (5.0 V)	+4.75 V	+5.25 V
VDD_CLAMP (3.3 V)	+3.135 V	+3.465 V
ESD protection voltage	–	2000 V

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21040. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21040.

3.2 Temperature Limit Ratings

Table 10 lists the temperature limit ratings.

Table 10 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21040. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21040.

3.3 Supply Current and Power Dissipation

The values in Table 11 are estimates based on a PCI clock frequency of 33 megahertz and a network clock frequency of 10 megahertz.

Table 11 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	VDD=3.465 V, Ta=70 C	160	210	mA
Power	VDD=3.465 V, Ta=70 C	0.52	0.72	Watts

3.4 PCI Bus Electrical Specifications

This section contains information about electrical characteristics for the 21040 PCI.

3.4.1 PCI I/O Voltage Specifications

The 21040 meets the I/O voltage specifications listed in Table 12.

Table 12 I/O Voltage Specifications for 5.0-Volt Levels

Category	PCI I/O	PCI Output	PCI Input
Vil	O.8 V	Not applicable	0.8 V
Vih	2.0 V	Not applicable	2.0 V
Vol[1]	0.55 V	0.55 V	Not applicable
Voh	2.4 V	2.4 V	Not applicable
Ioh	–2 mA	–2 mA	Not applicable
Ioz	+/–10 µA	+/–10 µA	Not applicable
Max Vin	5.6 V	Not applicable	5.6 V
Cap[2]	8 pF	8 pF	8 pF

[1]Signals without pullup resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l**) must have 6 milliamps.

[2]Parameter design guarantee.

3.4.2 PCI Reset

PCI reset (RST) is an asynchronous signal that must be active for at least 10 PCI CLK cycles. Figure 3 shows the PCI reset timing characteristics, and Table 13 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

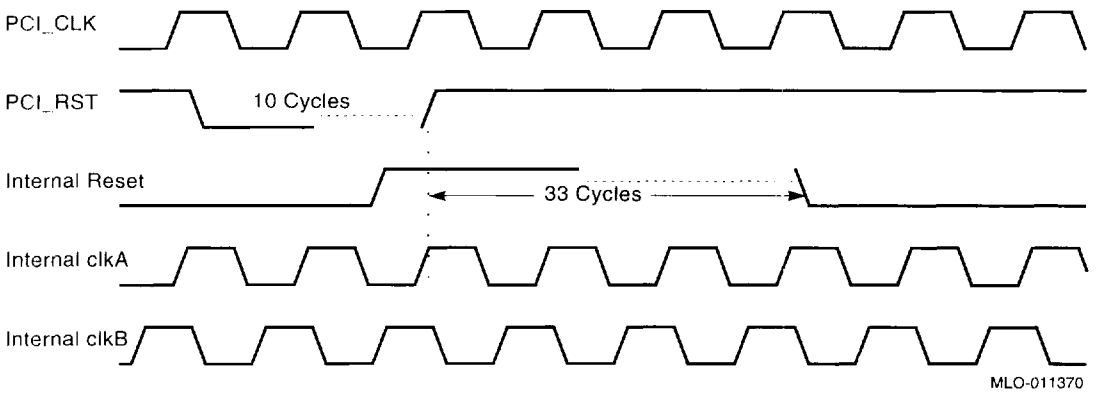


Table 13 PCI Reset Timing

Symbol	Parameter	Minimum	Maximum	Notes
Trst	RST pulse width	10*Tcycle	Not applicable	CLK active

3.4.3 PCI Clock Specifications

The standard clock frequency range for the PCI is between 16 megahertz and 33 megahertz. Figure 4 shows the PCI clock specification timing characteristics, and Table 14 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Specifications Timing Diagram

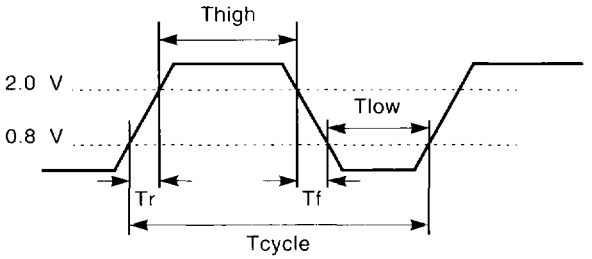


Table 14 PCI Clock Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Tcycle	Cycle time	30 ns	62.5 ns	–
Thigh	CLK high time	0.4*Tcycle	0.6*Tcycle	At 2 V
Tlow	CLK low time	0.4*Tcycle	0.6*Tcycle	At 0.8 V
Tr/Tf	CLK slew rate[1]	1 V/ns	4 V/ns	–

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.4.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 15 lists the other PCI signals.

Figure 5 Timing Diagram for Other PCI Signals

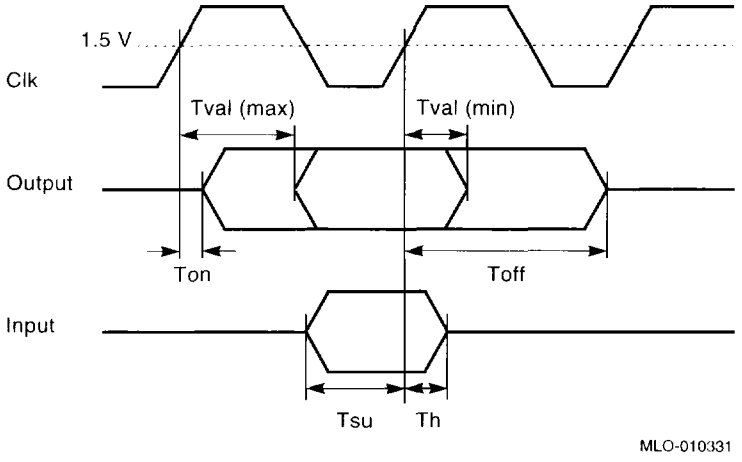


Table 15 Other PCI Signals

Symbol	Parameter	Minimum	Maximum	Conditions
Tval	CLK-to-signal valid delay	2 ns	11 ns	Cload = 50 pF
Ton[1]	Float-to-active delay from CLK	2 ns	–	–
Toff[1]	Active-to-float delay from CLK	Tval (minimum)	28 ns	–
Tsu	Input signal valid setup time before CLK	7 ns	–	–
Th	Input signal hold time from CLK	0 ns	–	–
Tr[1]	Unloaded output rise time	–	2 ns	0.4 V to 2.4 V
Tf[1]	Unloaded output fall time	–	2 ns	2.4 V to 0.4 V

[1]Parameter design guarantee.

3.5 Serial Interface Attachment DC Specifications

Table 16 lists the dc specifications for the external SIA, AUI, and twisted-pair parts of the SIA.

Table 16 SIA DC Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
External SIA Interface Pins					
V_{oh}	Output high voltage	I_{oh} = –4mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_{oz}	Maximum tristate output leakage current	V_{out} = V_{dd} or V_{ss}	–10	10	μA
AUI Pins					
V_{od}	Transmit differential output voltage (AUI_TD±)	78Ω termination	±550	±1200	mV
V_{odi}[1]	Transmit differential output idle voltage (AUI_TD±)	78Ω termination	–40	+40	mV
I_{odi}[1]	Transmit differential output idle current (AUI_TD±)	78Ω termination	–1	+1	mA

[1]Parameter design guarantee.

(continued on next page)

Table 16 (Cont.) SIA DC Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
AUI Pins					
V_{asq+}[1]	Differential positive squelch threshold (AUI_RD±)	–	175	275	mV
V_{asq-}[1]	Differential negative squelch threshold (AUI_RD± and AUI_CD±)	–	–275	–175	mV
V_{odu}[1]	Transmit differential output undershoot voltage on return to zero (AUI_TD±)	78Ω termination	–	–100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (TP_TD± and TP_TD±±)	I_{oh} = –25 mA	V_{dd} –0.2	V_{dd}	V
V_{tol}	Output low voltage (TP_TD± and TP_TD±±)	I_{ol} = 25 mA	V_{ss}	V_{ss} + 0.2	V
V_{tsq+}[1]	Differential positive squelch threshold (TP_RD±)	–	300	520	mV
V_{tsq-}[1]	Differential negative squelch threshold (TP_RD±)	–	–520	–300	mV
V_{tdif}[1]	Differential input voltage range (TP_RD±)	–	–3.1	3.1	V

[1]Parameter design guarantee.

3.6 Serial Interface Attachment Timing

This section describes the SIA timing limits.

3.6.1 External SIA Mode Timing—Transmit

Figure 6 shows the external SIA transmit timing characteristics, and Table 17 lists the external SIA transmit timing limits.

Figure 6 External SIA Mode Timing Diagram—Transmit

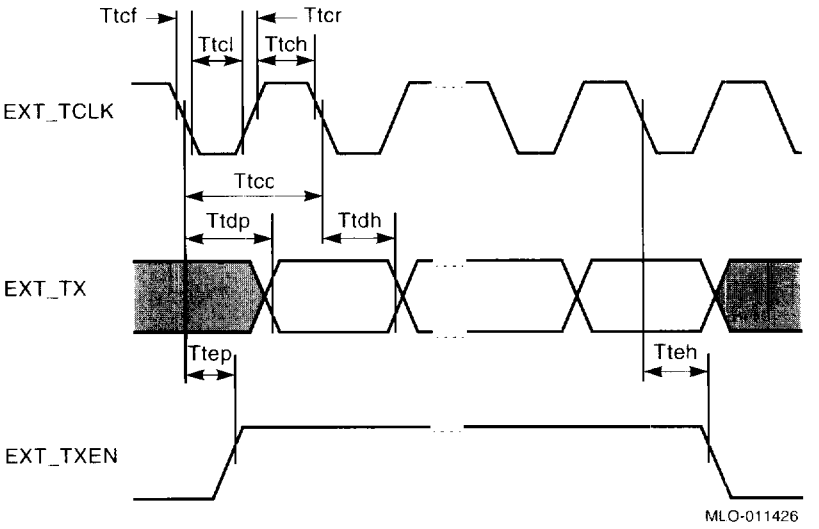


Table 17 External SIA Mode Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Ttcc	EXT_TCLK cycle time	99	101	ns
Ttcl	EXT_TCLK low time	45	55	ns
Ttch	EXT_TCLK high time	45	55	ns
Ttcr[1]	EXT_TCLK rise time	–	4	ns
Ttcf[1]	EXT_TCLK fall time	–	4	ns
Ttdp	EXT_TCLK rise to EXT_TX valid	–	40	ns
Ttdh	EXT_TX hold after EXT_TCLK rise	5	–	ns
Ttep	EXT_TCLK rise to EXT_TXEN valid	–	40	ns
Tteh	EXT_TXEN hold after EXT_TCLK fall	5	–	ns

[1]Parameter design guarantee.

3.6.2 External SIA Mode Timing—Collision

Figure 7 shows the external SIA collision timing characteristics, and Table 18 lists external SIA collision timing limits.

Figure 7 External SIA Mode Timing Diagram—Collision

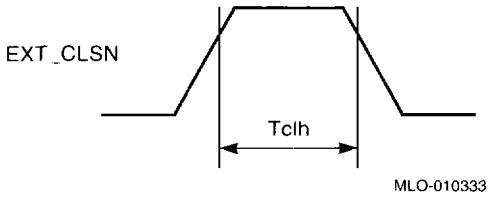


Table 18 External SIA Mode Timing—Collision

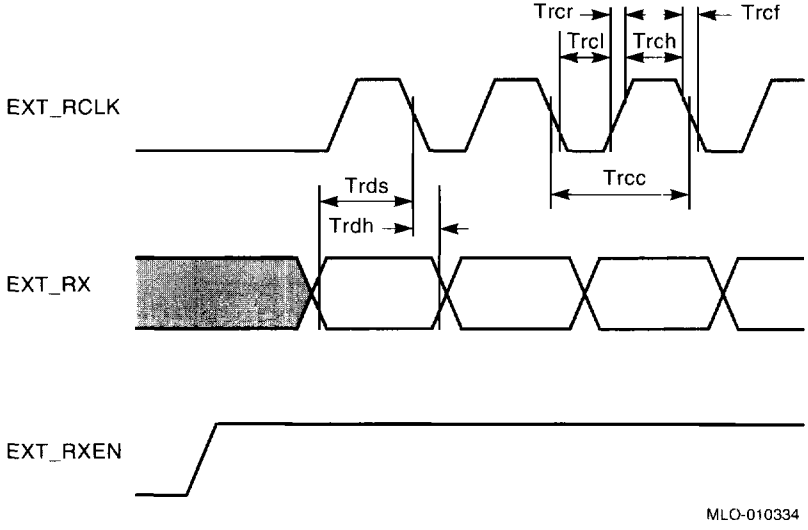
Symbol	Definition	Minimum	Maximum	Units
Tclh[1]	EXT_CLSN high time	40	–	ns

[1]Parameter design guarantee.

3.6.3 External SIA Mode Timing—Receive, Start of Packet

Figure 8 shows the external SIA timing characteristics in receive mode, start of packet.

Figure 8 External SIA Mode Timing Diagram—Receive, Start of Packet



3.6.4 External SIA Mode Timing—Receive, End of Packet

Figure 9 shows the external SIA timing characteristics in receive mode, end of packet; and Table 19 lists the external SIA timing limits in receive mode, end of packet.

Figure 9 External SIA Mode Timing Diagram—Receive, End of Packet

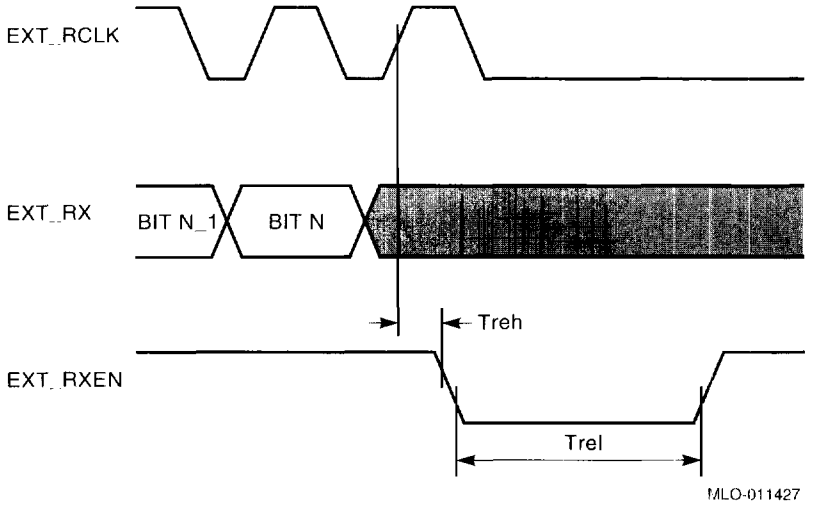


Table 19 External SIA Mode Timing—Receive, Start and End of Packet

Symbol	Definition	Minimum	Maximum	Units
Trcc	EXT_RCLK cycle time	90	118	ns
Trcl	EXT_RCLK low time	38	–	ns
Trch	EXT_RCLK high time	38	–	ns
Trcr[1]	EXT_RCLK rise time	–	4	ns
Trcf[1]	EXT_RCLK fall time	–	4	ns
Trds	EXT_RX setup to EXT_RCLK fall	10	–	ns
Trdh	EXT_RX hold after EXT_RCLK fall	5	–	ns
Treh	EXT_RXEN hold after EXT_RCLK rise	40	–	ns
Trel	EXT_RXEN low time	120	–	ns

[1]Parameter design guarantee.

3.6.5 Internal SIA Mode AUI Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the AUI, and Table 20 lists the internal SIA transmit timing limits for the AUI.

Figure 10 Internal SIA Mode AUI Timing Diagram—Transmit

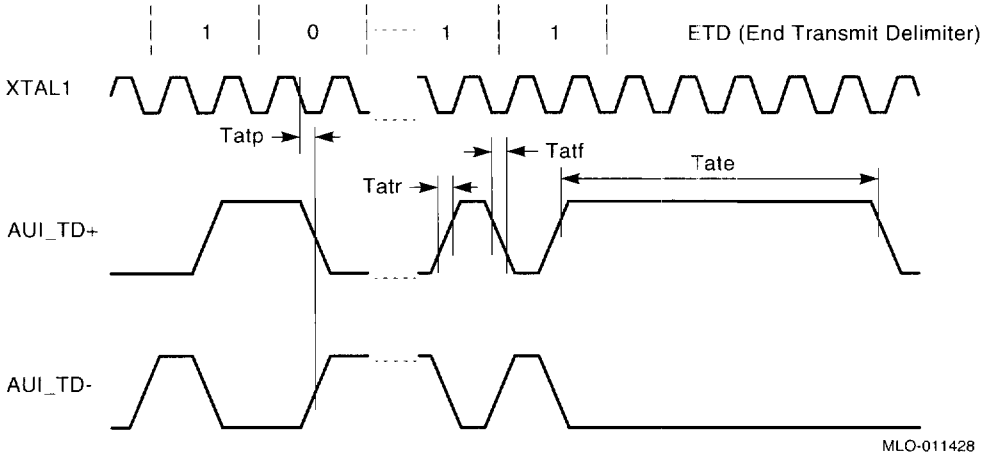


Table 20 Internal SIA Mode AUI Timing—Transmit

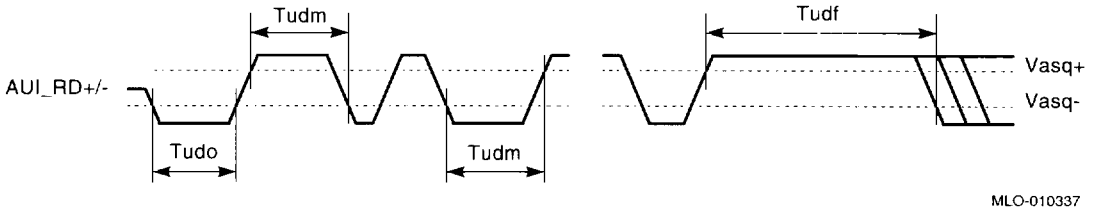
Symbol	Definition	Minimum	Maximum	Units
Tatp	AUI_TD+, AUI_TD– propagation delay from XTAL1 fall	–	30	ns
Tatr[1]	AUI_TD+, AUI_TD– rise time	2	8	ns
Tatf[1]	AUI_TD+, AUI_TD– fall time	2	8	ns
Tatm[1]	AUI_TD+, AUI_TD– rise and fall time mismatch (not shown)	–	1	ns
Tate	AUI_TD+/– end transmit delimiter length	345	405	ns

[1]Parameter design guarantee.

3.6.6 Internal SIA Mode AUI Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the AUI.

Figure 11 Internal SIA Mode AUI Timing Diagram—Receive



3.6.7 Internal SIA Mode AUI Timing—Collision

Figure 12 shows the internal SIA collision timing characteristics for the AUI, and Table 21 lists the internal SIA collision timing limits for the AUI.

Figure 12 Internal SIA Mode AUI Timing Diagram—Collision

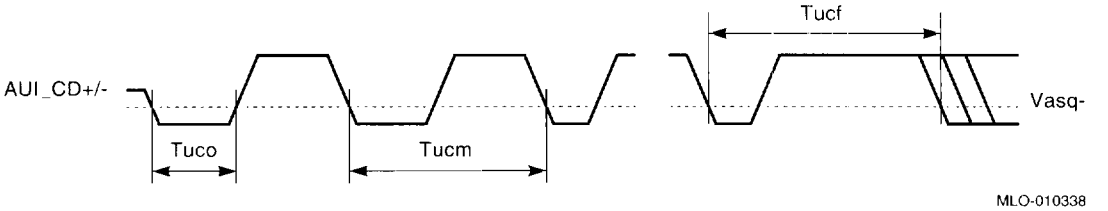


Table 21 Internal SIA Mode AUI Timing—Receive and Collision

Symbol	Definition	Minimum	Maximum	Units
Tudo	AUI_RD+/– start of frame pulse width	20	25	ns
Tudm	AUI_RD+/– delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tudf	AUI_RD+/– delay from last squelch crossing recognized as end of packet	150	–	ns
Tuco	AUI_CD+/– start of collision pulse width	20	25	ns
Tucm	AUI_CD+/– delay between squelch crossings not recognized as end of collision	–	140	ns
Tucf	AUI_CD+/– delay from last squelch crossing recognized as end of collision	150	–	ns

3.6.8 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 13 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA transmit limits.

Figure 13 Internal SIA Mode 10BASE-T Interface Timing Diagram— Transmit

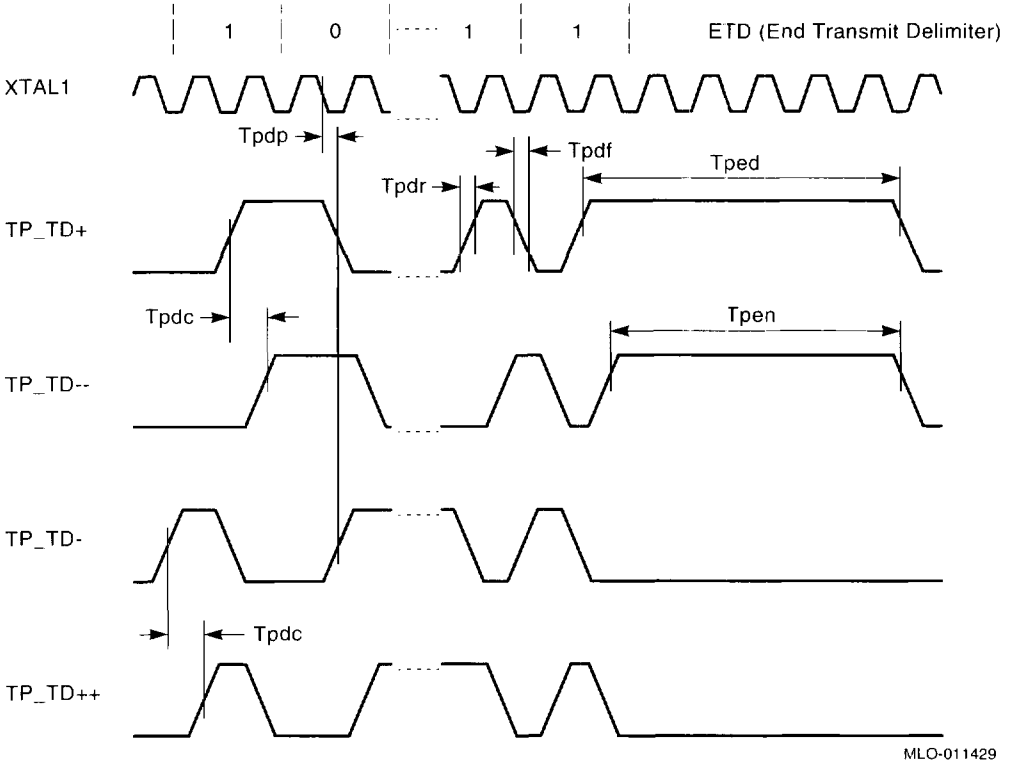


Table 22 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Symbol	Definition	Minimum	Maximum	Units
Tpdp	TP_TD+, TP_TD– propagation delay from XTAL1 fall	–	30	ns
Tpdr[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – rise time	2	8	ns
Tpdf[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – fall time	2	8	ns
Tpdm[1]	TP_TD+, TP_TD++, TP_TD–, TP_TD– – rise and fall time mismatch (not shown)	–	1	ns
Tpdc	TP_TD+ to TP_TD– – and TP_TD– to TP_TD++ delay	46	54	ns
Tped	TP_TD+/– end transmit delimiter length	295	355	ns
Tpen	TP_TD++/– – end transmit delimiter length	245	305	ns

[1]Parameter design guarantee.

3.6.9 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 14 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 14 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive

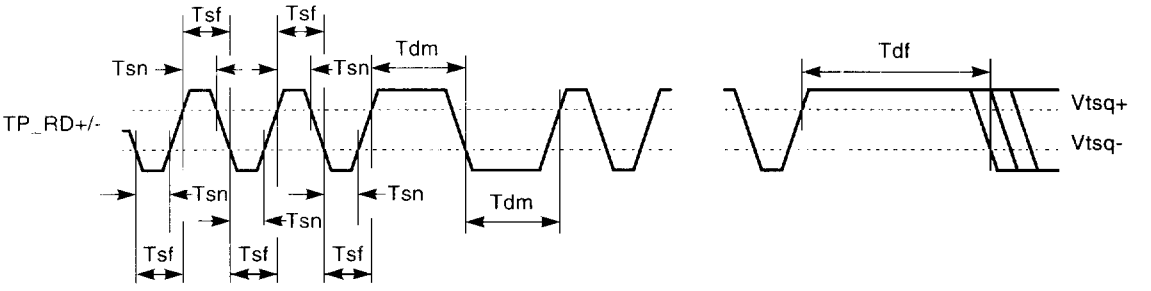


Table 23 Internal SIA Mode 10BASE-T Interface Timing—Receive

Symbol	Definition	Minimum	Maximum	Units
Tsn	TP_RD+/– start of frame pulse width during smart squelch operation	15	20	ns
Tsf	TP_RD+/– maximum delay between opposite squelch crossings to not turn smart squelch off	140	150	ns
Tdm	TP_RD+/– delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tdf	TP_RD+/– delay from last squelch crossing recognized as end of packet	150	–	ns

3.6.10 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 15 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 15 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

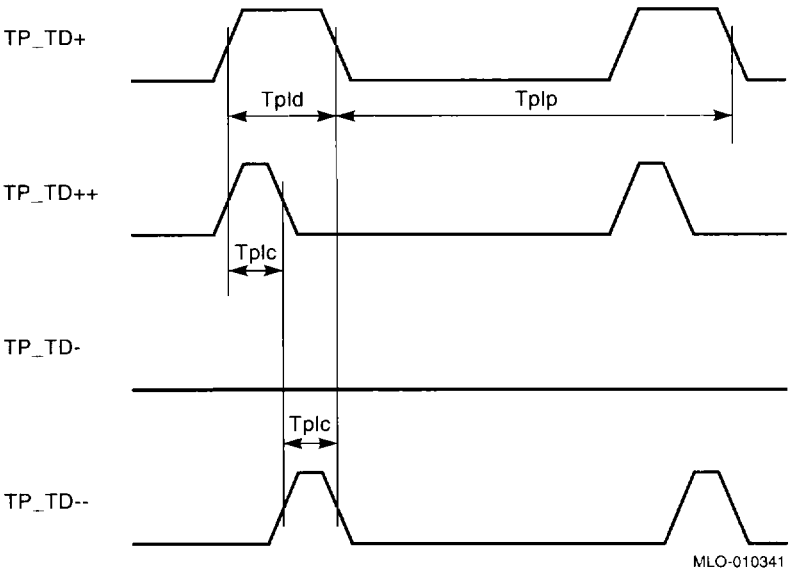


Table 24 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Units
Tpld	TP_TD+ idle link pulse width	80	120	ns
Tplc	TP_TD++ and TP_TD– – idle link pulse width	40	60	ns
Tplp	Idle link pulse period	8	24	ms

3.7 Ethernet ID Port Timing

Figure 16 shows the Ethernet ID port timing, and Table 25 lists the Ethernet ID port limits.

Figure 16 Ethernet ID Port Timing Diagram

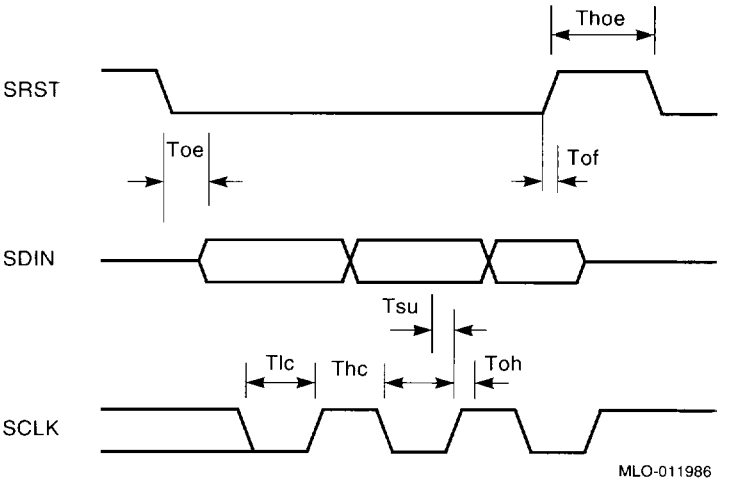


Table 25 Ethernet ID Port Timing Characteristics

Symbol	Definition	Minimum	Maximum	Units
Tlc	SCLK low time	4*Tcycle[1]	4*Tcycle[1]	ns
Thc	SCLK high time	4*Tcycle[1]	4*Tcycle[1]	ns
Toh	SDIN hold from SCLK	0	--	ns
Tsu	SDIN setup time from SCLK	Tcycle[1]	--	ns
Tof[2]	SRST to SDIN float delay	0	--	ns
Thoe	SRST high time	4*Tcycle[1]	--	ns
Toe	SRST to SDIN valid	–	3*Tcycle[1]	ns

[1]Refer to Table 14 for PCI clock specifications.

[2]Parameter design guarantee.

3.8 JTAG Boundary Scan Timing

Figure 17 shows the JTAG boundary scan timing, and Table 26 lists the interface signal timing relationships.

Figure 17 JTAG Boundary Scan Timing Diagram

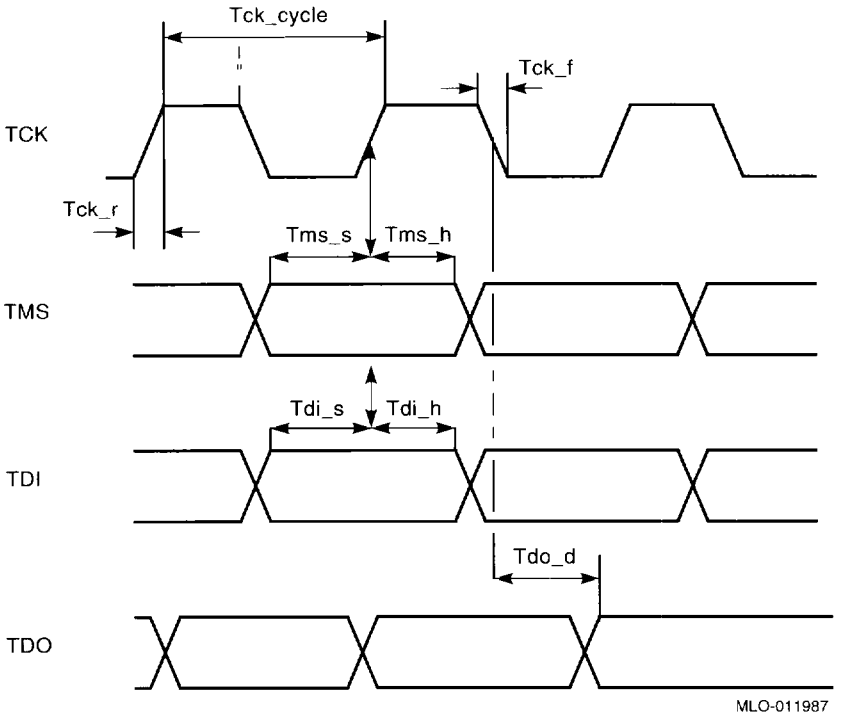


Table 26 JTAG Interface Signal Timing Relationships

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	TMS setup time	20	–	ns
Tms_h	TMS hold time	5	–	ns
Tdi_s	TDI setup time	20	–	ns
Tdi_h	TDI hold time	5	–	ns
Tdo_d	TDO delay time	–	20	ns
Tck_r[1]	TCK rise time	–	3	ns
Tck_f[1]	TCK fall time	–	3	ns
Tck_cycle	TCK cycle time	90	–	ns

[1]Parameter design guarantee.

4 Mechanical Specifications

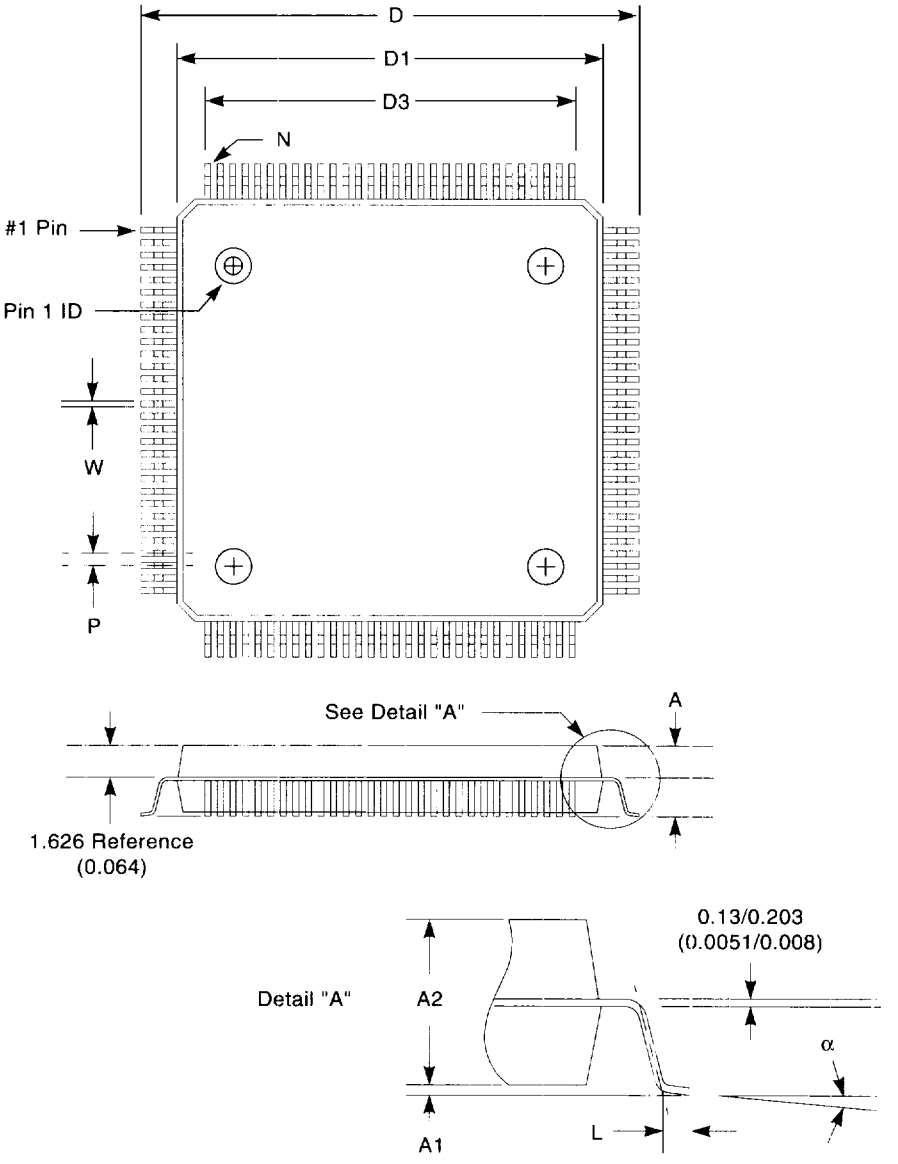
The 21040 is contained in a 120-pin plastic quad flat pack (PQFP). Table 27 lists the mechanical specifications, and Figure 18 shows the mechanical layout of the 21040.

Table 27 Mechanical Features

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	–	–	4.07
A1	0.05	–	–
A2	3.17	3.37	3.67
D	30.90	31.20	31.50
D1	27.80	28.00	28.20
D3	23.20 Reference	23.20 Reference	23.20 Reference
L	0.65	0.80	0.95
N	–	120	–
P	0.80 BSC	0.80 BSC	0.80 BSC
W	0.30	0.35	0.45
α	0°	–	7°

[1]All dimensions are in millimeters.

Figure 18 Mechanical Layout of the DECchip 21040



Note: All dimensions are in millimeters.

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