

Am54S/74S181

Four-Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics

- Advanced Schottky technology
- Performs 16 arithmetic operations including add, subtract, double and compare.
- Performs all 16 possible logic operations of two variables in typically 11ns.
- Typical 4-bit add time is 11ns and carry time is 6ns
- Full look-ahead capability for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

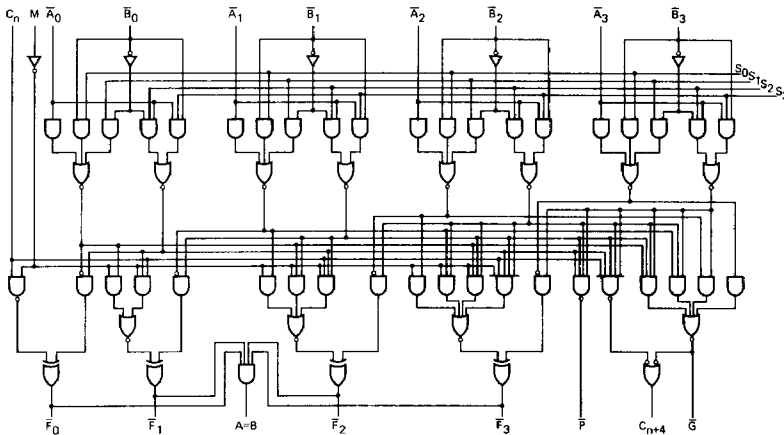
The Am54S/74S181 is a 4-bit, high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is LOW the 16 arithmetic operations are performed under the control of the four select inputs. When the mode control is HIGH the sixteen logic operations are performed on an individual bit basis between the two 4-bit parallel words under the control of the four select inputs.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate (P) and carry generate (G) outputs.

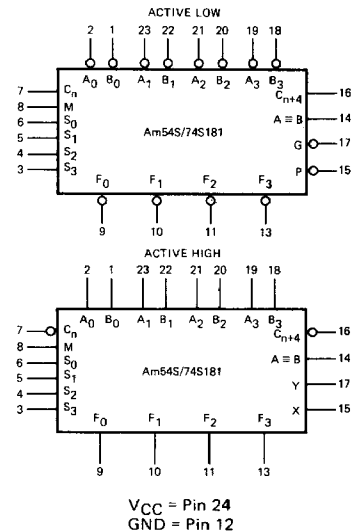
An open collector output $A = B$ is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wired-AND connection for larger word lengths.

In many systems, the carry output C_{n+4} is connected to the next higher C_n to provide ripple block arithmetic. The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

LOGIC DIAGRAM



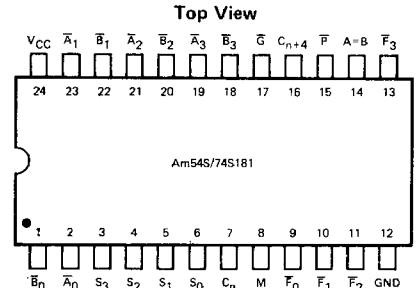
LOGIC SYMBOLS



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	SN74S181N
Hermetic DIP	0°C to +70°C	SN74S181J
Dice	0°C to +70°C	SN74S181X
Hermetic DIP	-55°C to +125°C	SN54S181J
Hermetic Flat Pak	-55°C to +125°C	SN54S181W
Dice	-55°C to +125°C	SN54S181X

CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	-0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	-0.5V to +V _{CC} max.
DC Input Voltage	-0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am74S181	T _A = 0°C to +70°C	V _{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54S181	T _A = -55°C to +125°C	V _{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Output HIGH Voltage (Except A=B Output)	V _{CC} = MIN., I _{OH} = -1mA V _{IN} = V _{IH} or V _{IL}	54S	2.5	3.4	Volts
			74S	2.7	3.4	
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 20mA V _{IN} = V _{IH} or V _{IL}			0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA			-1.2	Volts
I _{OH}	Output HIGH Current for A=B Output	V _{CC} = MIN., V _{OH} = 5.5V V _{IN} = V _{IH} or V _{IL}			250	μA
I _{IL} (Note 3)	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5V	M		-2	mA
			A _i or B _i		-6	
			S _i		-8	
			C _n		-10	
I _{IH} (Note 3)	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V	M		50	μA
			A _i or B _i		150	
			S _i		200	
			C _n		250	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V			1	mA
I _{SC}	Output Short Circuit Current (Note 4) (Except A = B Output)	V _{CC} = MAX.	-40		-100	mA
I _{CC}	Power Supply Current (Note 5)	V _{CC} = MAX.		120	180	mA
		V _{CC} = MAX., T _A = 125°C Am54S Flat Package (W) Only			159	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured under two conditions - typ. and max. apply to both.
A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open.
B. S_i, M at 4.5V; all other inputs grounded; outputs open.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15$ pF, $R_L = 280\Omega$)

Parameter	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	C_n	C_{n+4}			5	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	C_n	\bar{F}_i	$M = 0V$		7	12	ns
t_{PHL}			(SUM or DIFF mode)		6	12	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{G}	$M = 0V, S_0 = S_3 = 4.5V,$		8	12	ns
t_{PHL}			$S_1 = S_2 = 0V$ (SUM mode)		7	12	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{G}	$M = 0V, S_0 = S_3 = 0V,$		10	15	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		10	15	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{P}	$M = 0V, S_0 = S_3 = 4.5V,$		7.5	12	ns
t_{PHL}			$S_1 = S_2 = 0V$ (SUM mode)		7.5	12	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{P}	$M = 0V, S_0 = S_3 = 0V,$		10	15	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		10.5	15	
t_{PLH}	\bar{A}_i or \bar{B}_i	$F_j(j > i)$	$M = 0V, S_0 = S_3 = 4.5V,$		10	16.5	ns
t_{PHL}			$S_1 = S_2 = 0V$ (SUM mode)		7	16.5	
t_{PLH}	\bar{A}_i or \bar{B}_i	$F_j(j > i)$	$M = 0V, S_0 = S_3 = 0V,$		12	20	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		9	22	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_{i+1}	$M = 0V, S_0 = S_3 = 4.5V,$		11	16.5	ns
t_{PHL}			$S_1 = S_2 = 0V$ (SUM mode)		11	16.5	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_{i+1}	$M = 0V, S_0 = S_3 = 0V,$		14	20	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		14	22	
t_{PLH}	\bar{A}_i or \bar{B}_i	\bar{F}_i	$M = 4.5V$ (LOGIC mode)		12	20	ns
t_{PHL}					9	22	
t_{PLH}	\bar{A}_i or \bar{B}_i	C_{n+4}	$M = 0V, S_0 = S_3 = 4.5V,$		12.5	18.5	ns
t_{PHL}			$S_1 = S_2 = 0V$ (SUM mode)		12.5	18.5	
t_{PLH}	\bar{A}_i or \bar{B}_i	C_{n+4}	$M = 0V, S_0 = S_3 = 0V,$		14	23	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		15	23	
t_{PLH}	\bar{A}_i or \bar{B}_i	$A = B$	$M = 0V, S_0 = S_3 = 0V,$		15	23	ns
t_{PHL}			$S_1 = S_2 = 4.5V$ (DIFF mode)		19	30	

OPERATION TABLE

CONTROL INPUTS				ACTIVE LOW INPUTS AND OUTPUTS		ACTIVE HIGH INPUTS AND OUTPUTS	
S_0	S_1	S_2	S_3	Arithmetic ($M = L, C_n = L$)	Logic ($M = H$)	Arithmetic ($M = L, \bar{C}_n = H$)	Logic ($M = H$)
L	L	L	L	A minus 1	\bar{A}	A	\bar{A}
H	L	L	L	AB minus 1	\bar{AB}	A + B	$\bar{A} + \bar{B}$
L	H	L	L	\bar{AB} minus 1	$\bar{A} + B$	A + \bar{B}	$\bar{A}\bar{B}$
H	H	L	L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus [A + \bar{B}]	$\bar{A} + \bar{B}$	A plus $\bar{A}\bar{B}$	$\bar{A}\bar{B}$
H	L	H	L	AB plus [A + \bar{B}]	\bar{B}	$\bar{A}\bar{B}$ plus [A + B]	\bar{B}
L	H	H	L	A minus B minus 1	$A \oplus \bar{B}$	A minus B minus 1	$A \oplus B$
H	H	H	L	A + \bar{B}	A + \bar{B}	$\bar{A}\bar{B}$ minus 1	$\bar{A}\bar{B}$
L	L	L	H	A plus [A + B]	$\bar{A}\bar{B}$	A plus AB	$\bar{A} + \bar{B}$
H	L	L	H	A plus B	$A \oplus B$	A plus B	$A \oplus \bar{B}$
L	H	L	H	AB plus [A + B]	\bar{B}	AB plus [A + \bar{B}]	\bar{B}
H	H	L	H	A + B	A + B	AB minus 1	AB
L	L	H	H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $\bar{A}\bar{B}$	$\bar{A}\bar{B}$	A plus [A + B]	A + \bar{B}
L	H	H	H	A plus $\bar{A}B$	$\bar{A}B$	A plus [A + \bar{B}]	A + B
H	H	H	H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

DEFINITION OF FUNCTIONAL TERMS

$\bar{A}_0, \bar{A}_1, \bar{A}_2, \bar{A}_3$ The A data inputs.

$\bar{B}_0, \bar{B}_1, \bar{B}_2, \bar{B}_3$ The B data inputs.

S_0, S_1, S_2, S_3 The control inputs used to determine the arithmetic or logic function performed.

$\bar{F}_0, \bar{F}_1, \bar{F}_2, \bar{F}_3$ The data outputs of the ALU.

M The mode control inputs used to select either the arithmetic or logic operations.

C_n The carry-in input of the ALU.

C_{n+4} The carry-look-ahead output of the four-bit input field.

G The carry-generate output for use in multi-level look-ahead schemes.

P The carry-propagate output for use in multi-level look-ahead schemes.

A = B The open collector comparator output that can be used to determine equivalence. This output is HIGH whenever the four \bar{F} outputs are HIGH.

USER NOTES

1. Throughout this data sheet, the active LOW input and output terminology has been used. For the active HIGH definition, the nomenclature shown under the active HIGH logic symbol should be substituted.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in ($C_n = \text{HIGH}$) for the active LOW case and ($\bar{C}_n = \text{LOW}$) for the active HIGH case.
6. The **A = B** output only indicates that the four \bar{F} outputs are all HIGH.

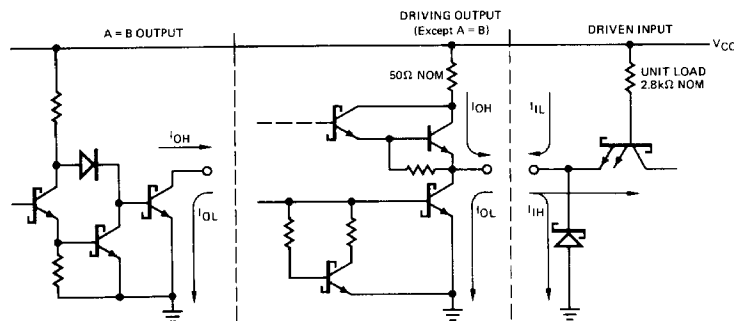
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Output HIGH	Output Drive Output LOW
\bar{B}_0	1	3	—	—
\bar{A}_0	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
\bar{F}_0	9	—	20	10
\bar{F}_1	10	—	20	10
\bar{F}_2	11	—	20	10
GND	12	—	—	—
\bar{F}_3	13	—	20	10
A = B	14	—	O/C	10
P	15	—	20	10
C_{n+4}	16	—	20	10
G	17	—	20	10
\bar{B}_3	18	3	—	—
\bar{A}_3	19	3	—	—
\bar{B}_2	20	3	—	—
\bar{A}_2	21	3	—	—
\bar{B}_1	22	3	—	—
\bar{A}_1	23	3	—	—
VCC	24	—	—	—

O/C = Open Collector

A Schottky unit load is defined as 50 μ A measured at 2.7V HIGH and -2.0 mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5V, S_1 = S_2 = M = 0V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	$\bar{F}_{i(i>1)}$	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	$\bar{F}_{i(i>1)}$	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	\bar{B}_i	None	C_n	Remaining \bar{A} and \bar{B}	\bar{F}_{i+1}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	C_n	Remaining \bar{A} and \bar{B}	\bar{F}_{i+1}	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A}, C_n	\bar{G}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A}, C_n	\bar{G}	In-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A}, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A}, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}							

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5V, S_0 = S_3 = M = 0V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	$\bar{F}_{i(i>1)}$	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	$\bar{F}_{i(i>1)}$	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}, C_n	Remaining \bar{A}	\bar{F}_{i+1}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{B}, C_n	Remaining \bar{A}	\bar{F}_{i+1}	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	$A = B$	In-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	$A = B$	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All \bar{A} and \bar{B}	None	Any \bar{F} or C_{n+4}	In-Phase
t_{PHL}							

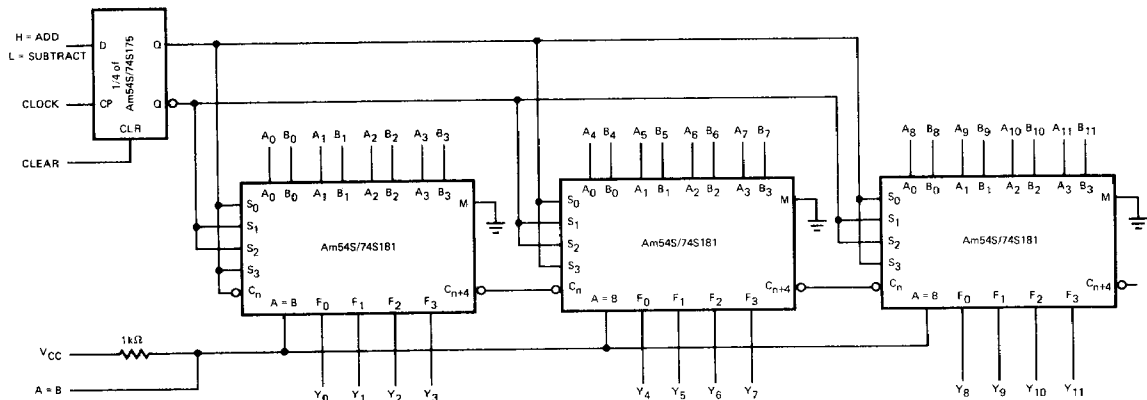
LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5V, S_0 = S_3 = 0V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{F}_i	Out-of-Phase
t_{PHL}							
t_{PLH}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{F}_i	Out-of-Phase
t_{PHL}							

APPLICATIONS

12-Bit Adder/Subtractor (2's Complement)



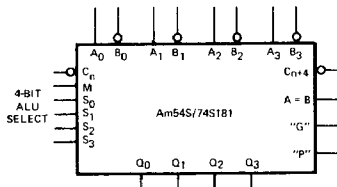
Function Table

A = Active HIGH B = Active LOW

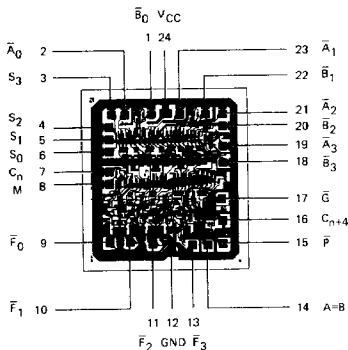
S ₀	S ₁	S ₂	S ₃	Arithmetic (M = L, C _n = H)	Logic (M = H)
L	L	L	L	A	\bar{A}
H	L	L	L	A + \bar{B}	$\bar{A}\bar{B}$
L	H	L	L	A + B	$\bar{A}\bar{B}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus [A + \bar{B}]	B
L	H	H	L	A plus B	$A \oplus B$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $\bar{A}\bar{B}$	$\bar{A} + \bar{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$\bar{A}\bar{B}$ plus [A + B]	\bar{B}
H	H	L	H	$\bar{A}\bar{B}$ minus 1	$\bar{A}\bar{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus [A + \bar{B}]	A + B
L	H	H	H	A plus [A + B]	A + \bar{B}
H	H	H	H	A minus 1	A

L = Low Voltage Level
H = High Voltage Level

If one input is defined active-HIGH and the second input is defined active-LOW, the sixteen arithmetic and logic functions of the ALU are reordered as shown in the function table.



Metallization and Pad Layout



DIE SIZE: = 0.083" X 0.091"