55107A • 75107A • 55108A • 75108A

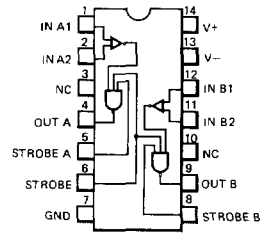
DUAL LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55107A/75107A and 55108A/75108A are high speed, two-channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3V but can be increased to ±15V by the use of input attenuators. Separate or common strobes are available. The 55107A/75107A circuit features an active pull-up (totem pole output). The 55108A/75108A circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the 55109/75109 and 55110/75110 line drivers. The 55107A/75107A and 55108A/75108A line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY**
- **HIGH DC NOISE MARGINS**
- **STROBE INPUT CLAMP DIODES**

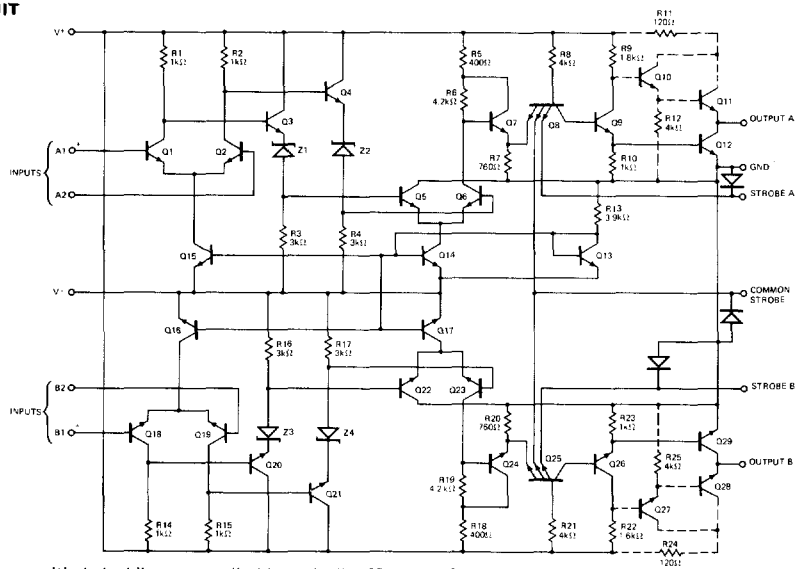
CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
55107A	SN55107AJ
75107A	SN75107AJ
75107A	SN75107AN
55108A	SN55108AJ
75108A	SN75108AJ
75108A	SN75108AN

EQUIVALENT CIRCUIT



NOTE: Components shown with dashed lines are applicable to the 55107A and 75107A only.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	±7V
Internal Power Dissipation (Note 3)	670 mW
Differential Input Voltage (Note 2)	±6V
Common Mode Input Voltage (Note 1)	±5V
Strobe Input Voltage (Note 1)	5.5V
Operating Temperature Range	
55107A/108A	−55°C to +125°C
75107A/108A	0°C to +70°C
Storage Temperature Range	
Hermetic DIP (SN55/75107AJ, SN55/75108AJ)	−65°C to +150°C
Molded DIP (SN75107AN, SN75108AN)	−55°C to +125°C
Lead Temperature	
Hermetic DIP (Soldering, 60 Seconds) SN55/75107AJ, SN55/75108AJ	300°C
Molded DIP (Soldering, 10 Seconds) SN75107AN, SN75108AN	260°C

Notes on the following page

55107A • 75107A

ELECTRICAL CHARACTERISTICS [+4.5 V ≤ V_S ≤ ±5.5 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted, (Note 4)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	V_{DIFF} = 0.5V, V_{CM} = −3V to +3V		30	75	μA
Input LOW Current	V_{DIFF} = −2V, V_{CM} = −3V to +3V			−10	μA
Gate Input HIGH Current	V_{GATE} = 2.4V			40	μA
	V_{GATE} = V^+			1.0	mA
Gate Input LOW Current	V_{GATE} = 0.4V			−1.6	mA
Strobe Input HIGH Current	V_{STROBE} = 2.4V			80	μA
	V_{STROBE} = V^+			2.0	mA
Strobe Input LOW Current	V_{STROBE} = 0.4V			−3.2	mA
Output HIGH Voltage	I_L = −400μA, V_{CM} = −3V to +3V	2.4			V
Output LOW Voltage	I_{SINK} = 16mA, V_{CM} = −3V to +3V			0.4	V
Short-Circuit Output Current	V_O = 0 (Note 5)	−18		−70	mA
Positive Supply Current	V_O = V_{OH}, I_L = 0, T_A = 25°C		18	30	mA
Negative Supply Current	V_O = V_{OH}, I_L = 0, T_A = 25°C		−8.4	−15	mA
AC CHARACTERISTICS (V^+ = +5V, V^- = −5V, R_L = 390Ω, C_L = 50pF, T_A = 25°C See Test Circuit)					
t_{PLH} (D)			17	25	ns
t_{PHL} (D)			17	25	ns
t_{PLH} (S)			10	15	ns
t_{PHL} (S)			10	15	ns

55108A • 75108A

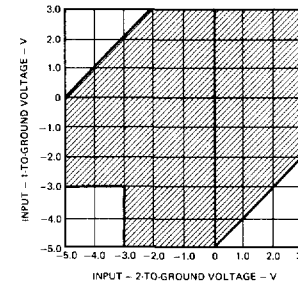
ELECTRICAL CHARACTERISTICS [±4.5 V ≤ V_S ≤ ±5.5 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted, (Note 4)]

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input HIGH Current	V_{DIFF} = 0.5V, V_{CM} = −3V to +3V		30	75	μA
Input LOW Current	V_{DIFF} = −2V, V_{CM} = −3V to +3V			−10	μA
Gate Input HIGH Current	V_{GATE} = 2.4V			40	μA
	V_{GATE} = V^+			1.0	mA
Gate Input LOW Current	V_{GATE} = 0.4V			−1.6	mA
Strobe Input HIGH Current	V_{STROBE} = 2.4V			80	μA
	V_{STROBE} = V^+			2.0	mA
Strobe Input LOW Current	V_{STROBE} = 0.4V			−3.2	mA
Output LOW Voltage	I_{SINK} = 16mA, V_{CM} = −3V to +3V			0.4	V
Output HIGH Current	V_{OUT} = V^+			250	μA
Positive Supply Current	V_O = V_{OH}, I_L = 0, T_A = 25°C		18	30	mA
Negative Supply Current	V_O = V_{OH}, I_L = 0, T_A = 25°C		−8.4	−15	mA
AC CHARACTERISTICS (V^+ = +5V, V^- = −5V, R_L = 390Ω, C_L = 15pF, T_A = 25°C See Test Circuit)					
t_{PLH} (D)			19	25	ns
t_{PHL} (D)			19	25	ns
t_{PLH} (S)			13	20	ns
t_{PHL} (S)			13	20	ns

TRUTH TABLE

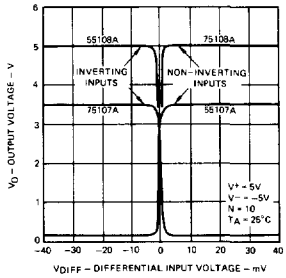
DIFFERENTIAL INPUTS 1–2	STROBES A or B	STROBES COM	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
−25 mV < V_{ID} <25 mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS

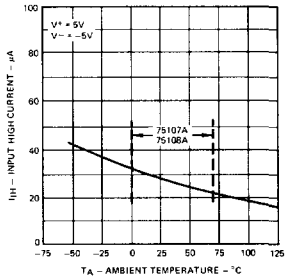


TYPICAL PERFORMANCE CURVES

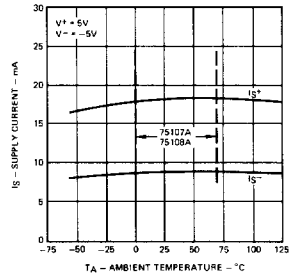
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



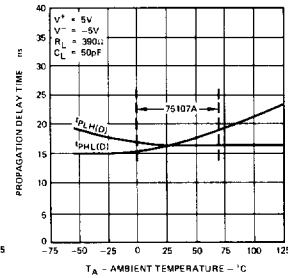
INPUT HIGH CURRENT INTO 1A OR 2A AS A FUNCTION OF AMBIENT TEMPERATURE



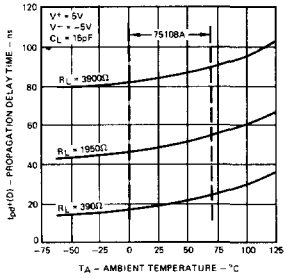
HIGH LOGIC LEVEL SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



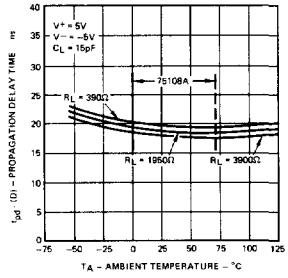
55107A, 75107A PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



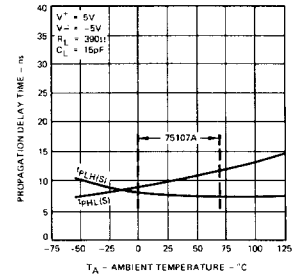
55108A, 75108A PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



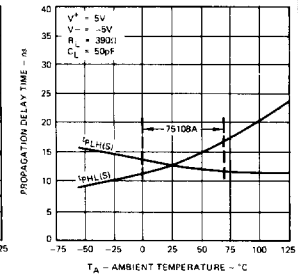
55108A, 75108A PROPAGATION DELAY TIME HIGH-TO-LOW LEVEL (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



55107A, 75107A PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



55108A, 75108A PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



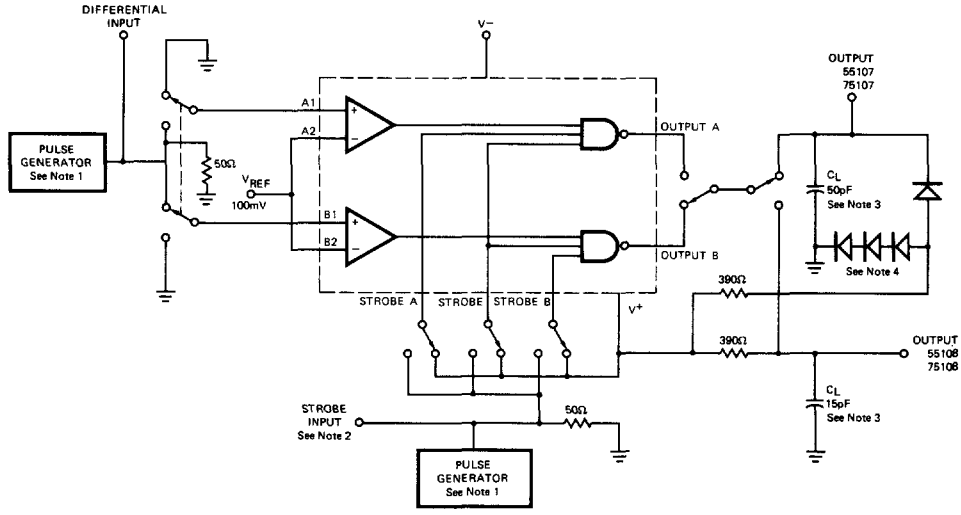
NOTES:

1. These voltages are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (—) terminal.
3. Rating applies to 70°C ambient temperature. Above 70°C derate at 8.3 mW/°C.
4. Specifications apply from 0°C to 70°C for 75107A and 75108A. Guaranteed supply voltage range is from ±4.75 V to ±5.25 V for 75107A and 75108A.
5. Note more than one (1) output should be shorted at a time.

6

SWITCHING CHARACTERISTICS

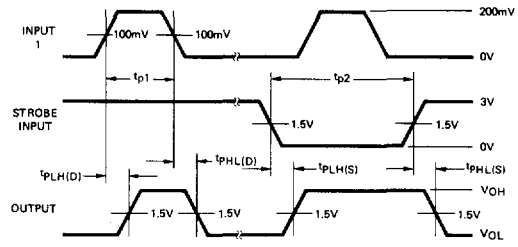
AC TEST CIRCUIT



NOTES:

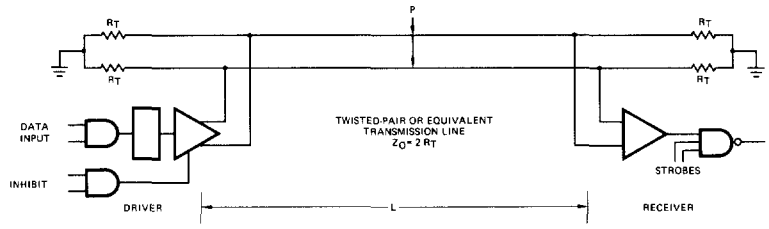
1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = t_f = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz t_{p2} = 1 μs, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested, to Strobe when inputs A1-A2 or B1-B2 are being tested, and to Strobe B when inputs B1-B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

VOLTAGE WAVEFORMS



APPLICATION

BASIC BALANCED-LINE TRANSMISSION SYSTEM



The 55107A/75107A dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30+1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

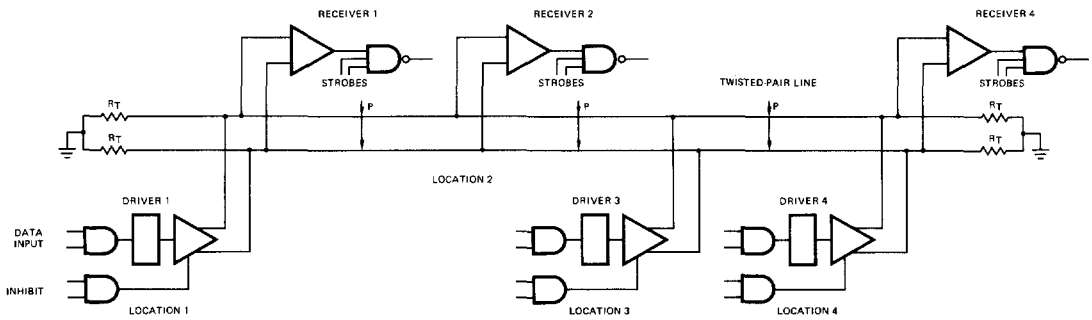
$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{O(on)} \cdot R_T$$

DATA-BUS OR PARTY-LINE SYSTEM

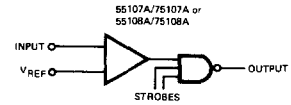


The strobe feature of the receivers and the inhibit feature of the drivers allow the 55107A/75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The 55107A/75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

6

APPLICATION (Cont'd)

UNBALANCED OR SINGLE-LINE SYSTEMS



The 55107A/75107A dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

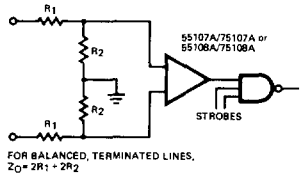
The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

PRECAUTIONS IN THE USE OF 55/75107A AND 55/75108A DUAL LINE RECEIVERS

The following precaution should be observed when using or testing 55107A/75107A line circuits:

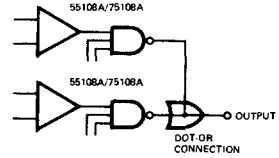
When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER



The 55107A/75107A and 55108A/75108A line receivers feature a common-mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

55108A/75108A DOT-OR OUTPUT CONNECTIONS



The 55108A/75108A line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other 55108A/75108A outputs. This allows a level of logic to be implemented without additional logic delay.