

54164, 54LS164 Shift Registers

8-Bit Serial-In Parallel-Out Shift Registers

Product Specification

Military Logic Products

FEATURES

- Gated serial data inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered clock and data inputs

DESCRIPTION

The 54164 and 54LS164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input

can be used as an Active-High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A Low-level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

ORDERING INFORMATION

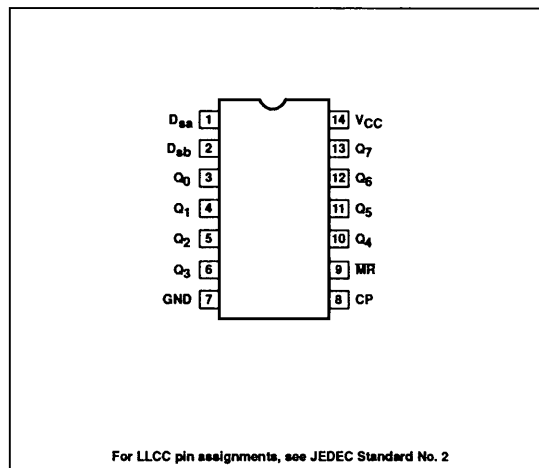
| DESCRIPTION | ORDER CODE |
|-------------------|---------------------------|
| Ceramic DIP | 54LS164/BCA, 54164/BCA |
| Ceramic Flat Pack | 54LS164/BDA |
| Ceramic LLCC | 54LS164/B2A |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

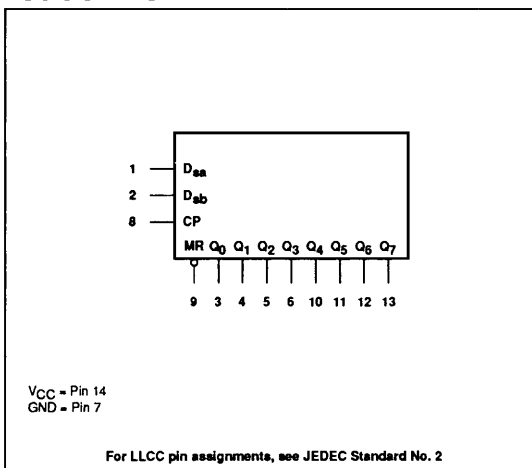
| PINS | DESCRIPTION | 54 | 54LS |
|------|-------------|-----|--------|
| All | Inputs | 1UL | 1LSUL |
| All | Outputs | 5UL | 10LSUL |

NOTE: Where a 54 Unit Load (UL) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54LS Unit Load (LSUL) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

PIN CONFIGURATION



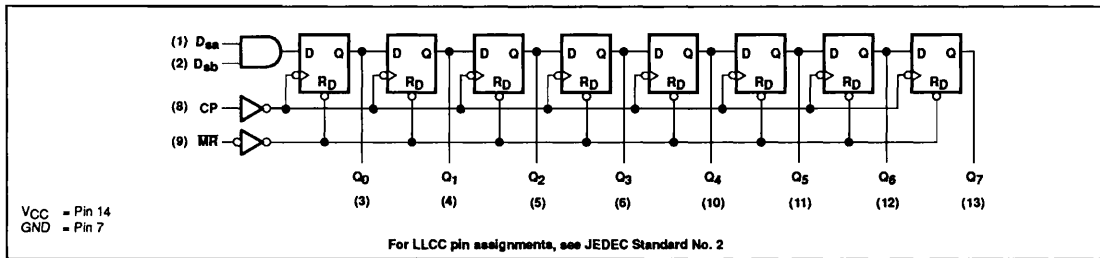
LOGIC SYMBOL



Shift Registers

54164, 54LS164

LOGIC DIAGRAM



MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | | |
|----------------|--------|----|-----------------|-----------------|----------------|---------------------------------|----------------|
| | MR | CP | D _{aa} | D _{ab} | Q ₀ | Q ₁ — Q ₆ | Q ₇ |
| Reset | L | X | X | X | L | L | L |
| Shift | H | ↑ | l | l | L | q ₀ — q ₆ | q ₆ |
| | H | ↑ | l | h | L | q ₀ — q ₆ | q ₆ |
| | H | ↑ | h | l | L | q ₀ — q ₆ | q ₆ |
| | H | ↑ | h | h | H | q ₀ — q ₆ | q ₆ |

- H = High voltage level
- h = High voltage level one set-up time prior to the Low-to-High Clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High Clock transition
- q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition
- X = Don't care
- ↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | 54164 | 54LS164 | UNIT |
|------------------|--|--------------------------|--------------------------|------|
| V _{CC} | Supply voltage | 7.0 | 7.0 | V |
| V _I | Input voltage range | -0.5 to +5.5 | -0.5 to +7.0 | V |
| I _I | Input current range | -30 to +5.0 | -30 to +1 | mA |
| V _O | Voltage applied to output in High output state range | -0.5 to +V _{CC} | -0.5 to +V _{CC} | V |
| T _{STG} | Storage temperature range | -65 to +150 | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 54164 | | | 54LS164 | | | UNIT |
|-----------------|--------------------------------------|-------|-----|------|---------|-----|------|------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | +0.8 | | | +0.7 | V |
| I _{IK} | Input clamp current | | | -12 | | | -18 | mA |
| I _{OH} | High-level output current | | | -400 | | | -400 | μA |
| I _{OL} | Low-level output current | | | 8 | | | 4 | mA |
| T _A | Operating free-air temperature range | -55 | | +125 | -55 | | +125 | °C |

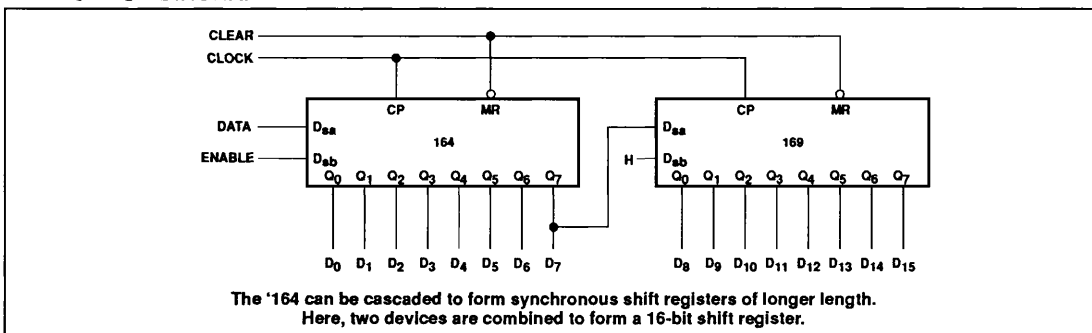
Shift Registers

54164, 54LS164

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | 54164 | | | 54LS164 | | | UNIT |
|------------------|---|--|-------|------------------|-------|---------|------------------|------|------|
| | | | Min | Typ ² | Max | Min | Typ ² | Max | |
| V _{OH} | High-level output voltage | V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max | 2.4 | 3.4 | | 2.5 | 3.4 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OL} = Max | | 0.2 | 0.4 | | 0.25 | 0.4 | V |
| V _{IK} | Input clamp voltage | V _{CC} = Min, I _I = I _{IK} | | | -1.5 | | | -1.5 | V |
| I _{IH2} | Input current at maximum input voltage | V _{CC} = Max V _I = 5.5V V _I = 7.0V | | | 1.0 | | | 0.1 | mA |
| I _{IH1} | High-level input current | V _{CC} = Max V _I = 2.4V V _I = 2.7V | | | 40 | | | 20 | μA |
| I _{IL} | Low-level input current | V _{CC} = Max, V _I = 0.4V | | | -1.6 | | | -0.4 | mA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = Max | -10 | | -27.5 | -20 | | -100 | mA |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = Max | | 37 | 54 | | 16 | 27 | mA |

APPLICATION DIAGRAM



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V⁵

| SYMBOL | PARAMETER | TEST CONDITIONS | 54164 | | 54LS164 | | UNIT |
|------------------|--------------------------------------|-----------------|-----------------------|-----|-----------------------|-----|------|
| | | | C _L = 15pF | | C _L = 15pF | | |
| | | | Min | Max | Min | Max | |
| f _{MAX} | Maximum shift frequency | Waveform 1 | 25 | | 25 | | MHz |
| t _{PLH} | Propagation delay Clock to output | Waveform 1 | | 27 | | 27 | ns |
| t _{PHL} | | | | 32 | | 32 | |
| t _{PHL} | Propagation delay MR to output | Waveform 2 | | 36 | | 36 | ns |

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

| SYMBOL | PARAMETER | TEST CONDITIONS | 54164 | | 54LS164 | | UNIT |
|------------------|--------------------------|-----------------|-------|-----|---------|-----|------|
| | | | Min | Max | Min | Max | |
| t _w | Clock pulse width | Waveform 1 | 20 | | 20 | | ns |
| t _w | MR pulse width | Waveform 2 | 20 | | 20 | | ns |
| t _s | Setup time data to clock | Waveform 3 | 15 | | 15 | | ns |
| t _H | Hold time data to clock | Waveform 3 | 5.0 | | 5.0 | | ns |
| t _{REC} | MR clock recovery time | Waveform 2 | 30 | | 30 | | ns |

Shift Registers

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54164 | | 54LS164 | | UNIT |
|------------------------|--------------------------------------|-----------------|---------------------|----------|---------------------|----------|----------|
| | | | $C_L = 50\text{pF}$ | | $C_L = 50\text{pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum shift frequency | Waveform 1 | 22 | | 22 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay Clock to output | Waveform 1 | | 34 41 | | 31 36 | ns ns |
| t_{PHL} | Propagation delay MR to output | Waveform 2 | | 46 | | 40 | ns |

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54164 | | 54LS164 | | UNIT |
|------------------------|--------------------------------------|-----------------|---------------------|----------|---------------------|----------|----------|
| | | | $C_L = 50\text{pF}$ | | $C_L = 50\text{pF}$ | | |
| | | | Min | Max | Min | Max | |
| f_{MAX} | Maximum shift frequency | Waveform 1 | 18 | | 20 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay Clock to output | Waveform 1 | | 31 48 | | 40 47 | ns ns |
| t_{PHL} | Propagation delay MR to output | Waveform 2 | | 55 | | 52 | ns |

AC SETUP REQUIREMENTS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

| SYMBOL | PARAMETER | TEST CONDITIONS | 54164 | | 54LS164 | | UNIT |
|-----------|--------------------------|-----------------|-------|-----|---------|-----|------|
| | | | Min | Max | Min | Max | |
| t_W | Clock pulse width | Waveform 1 | 30 | | 20 | | ns |
| t_W | MR pulse width | Waveform 2 | 50 | | 25 | | ns |
| t_S | Setup time data to clock | Waveform 3 | 15 | | 20 | | ns |
| t_H | Hold time data to clock | Waveform 3 | 10 | | 10 | | ns |
| t_{REC} | MR clock recovery time | Waveform 2 | 30 | | 30 | | ns |

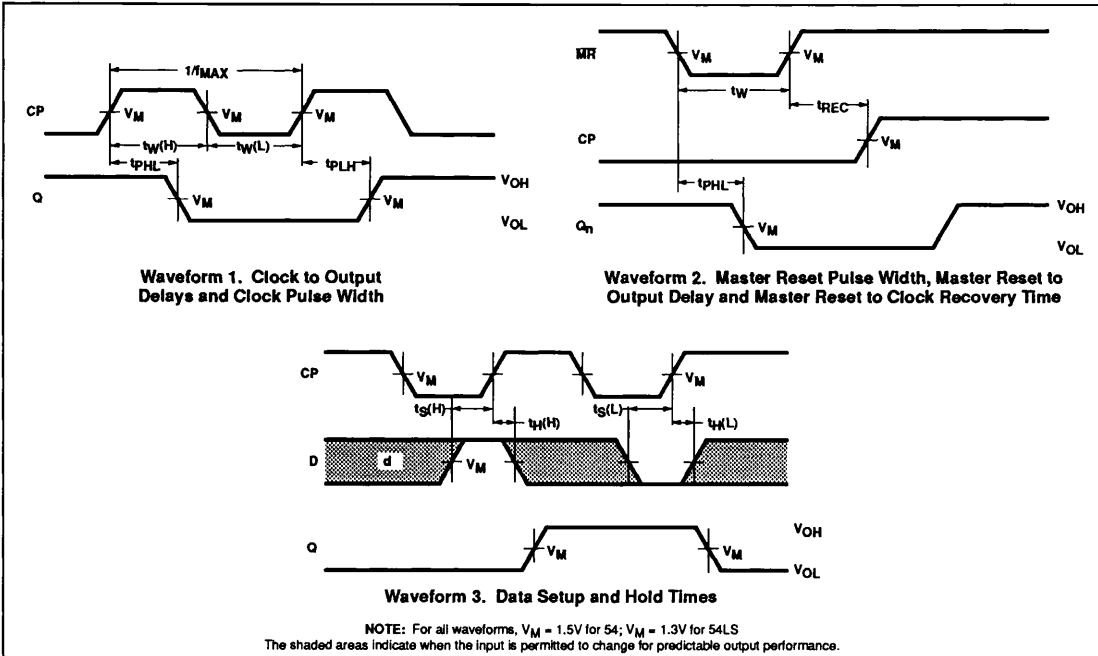
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then $\geq 4.0\text{V}$ applied to Master Reset, and all outputs open.
5. These parameters are guaranteed, but not tested.

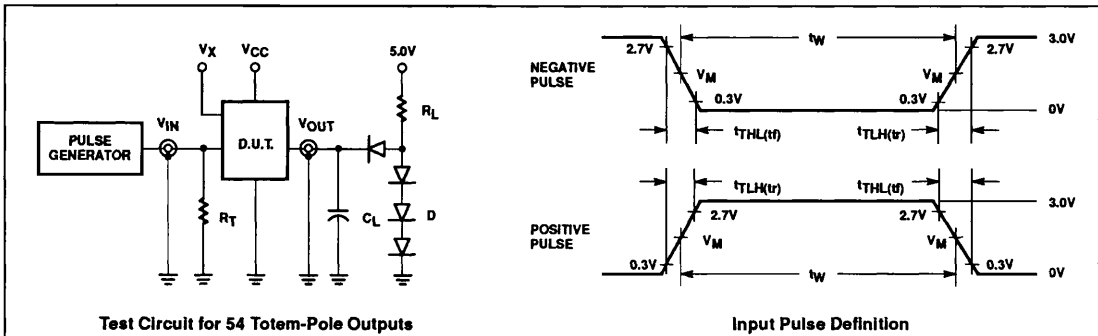
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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM



| FAMILY | INPUT PULSE CHARACTERISTICS | | | | | |
|---------|-----------------------------|-------|-----------|-------|---------------|---------------|
| | R_L | V_M | Rep. Rate | T_w | $T_{TLH}(tr)$ | $T_{THL}(tr)$ |
| 54LSXXX | 2.0k Ω | 1.3V | 1MHz | 500ns | $\leq 15ns$ | $\leq 6ns$ |
| 54XXX | 400 Ω | 1.5V | 1MHz | 500ns | $\leq 7ns$ | $\leq 7ns$ |

DEFINITIONS:

- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- V_X = Unclocked pins must be held at $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.