National Semiconductor

SCAN182373A
Transparent Latch with 25Ω Series Resistor Outputs

General Description

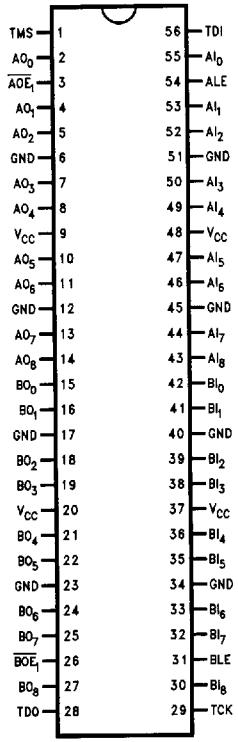
The SCAN182373A is a high performance BiCMOS transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Buffered active-low latch enable
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 11

Connection Diagram



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Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Latch Outputs

Order Number	Description
SCAN182373ASSC	SSOP in Tubes
SCAN182373ASSCX	SSOP in Tape and Reel
SCAN182373AFMQB	Military Flatpak

Truth Table

Inputs			AO (0–8)
ALE	†$\overline{AOE_1}$	AI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

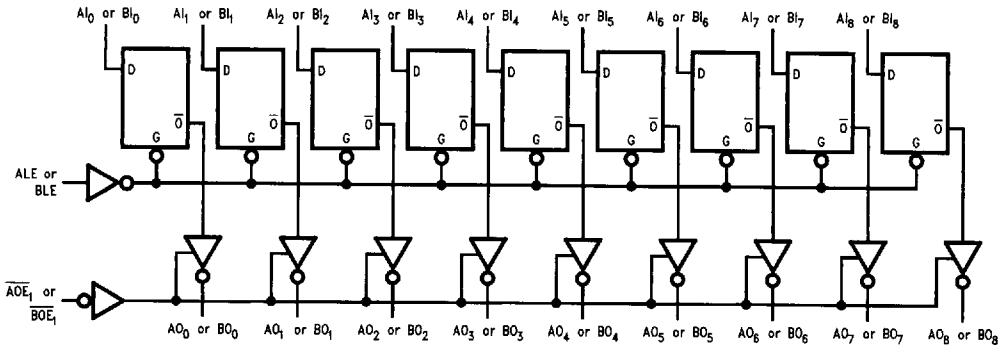
Inputs			BO (0–8)
BLE	†$\overline{BOE_1}$	BI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE
† = Inactive-to-active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182373A consists of two sets of nine D-type latches with TRI-STATE standard outputs. When the Latch Enable (ALE or BLE) input is HIGH, data on the inputs ($AI_{(0-8)}$ or $BI_{(0-8)}$) enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its input changes. When Latch Enable is LOW, the latches store the information that was present on the inputs a set-up time preceding the HIGH-to-LOW transition of the Latch Enable. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{AOE_1}$ or $\overline{BOE_1}$) input. When Output Enable is LOW, the standard outputs are in the 2-state mode. When Output Enable is HIGH, the standard outputs are in the high impedance mode, but this does not interfere with entering new data into the latches.

Logic Diagram



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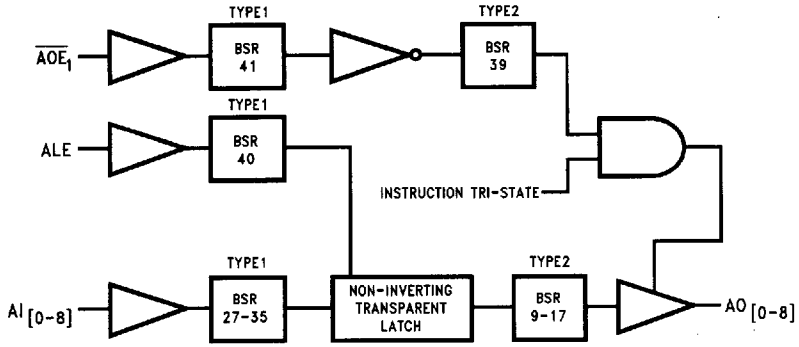
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams

Byte-A



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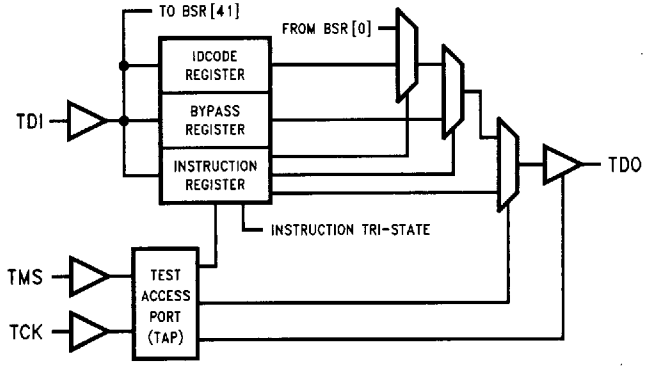
Tap Controller



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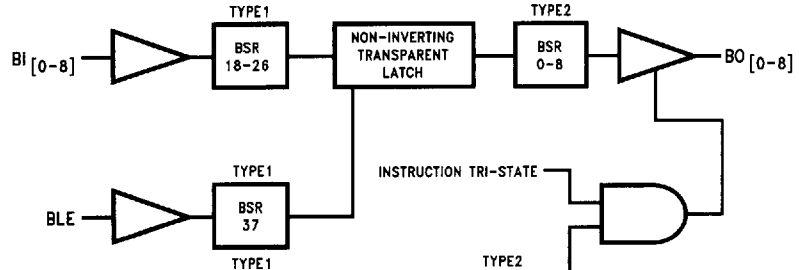
Byte-B



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Note: BSR stands for Boundary Scan Register.

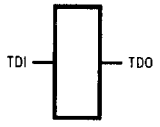
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10-11* for a further description of scan cell TYPE 1 and *Figure 10-12* for a further description of scan cell TYPE 2.)

Scan cell TYPE 1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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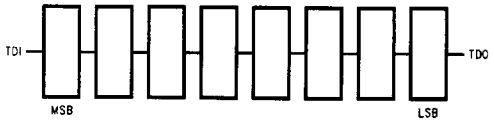
SCAN182373A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000001000	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Scan Chain Definition



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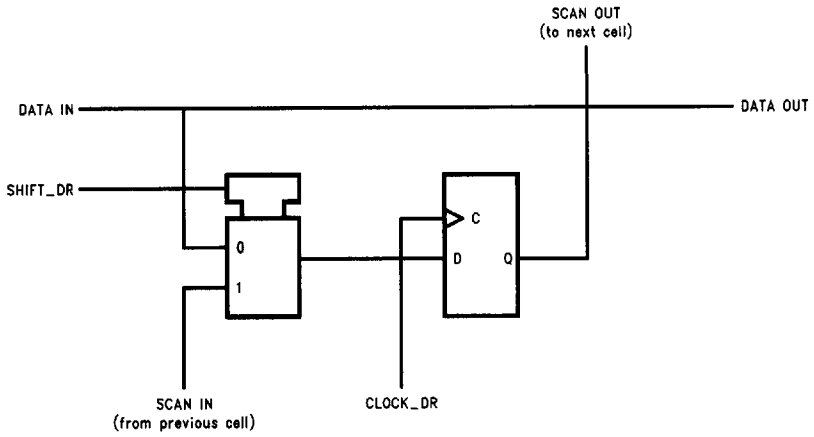
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



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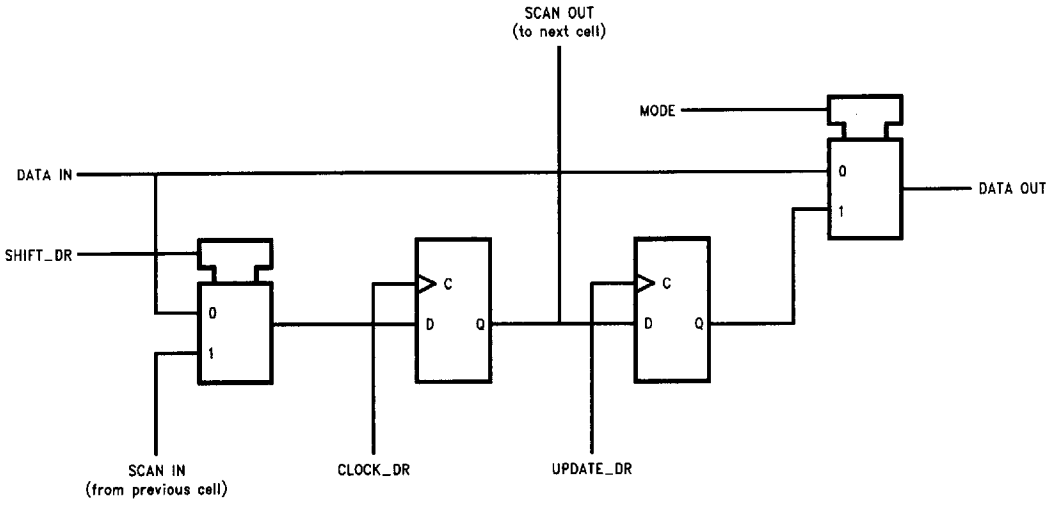
Scan Cell TYPE2



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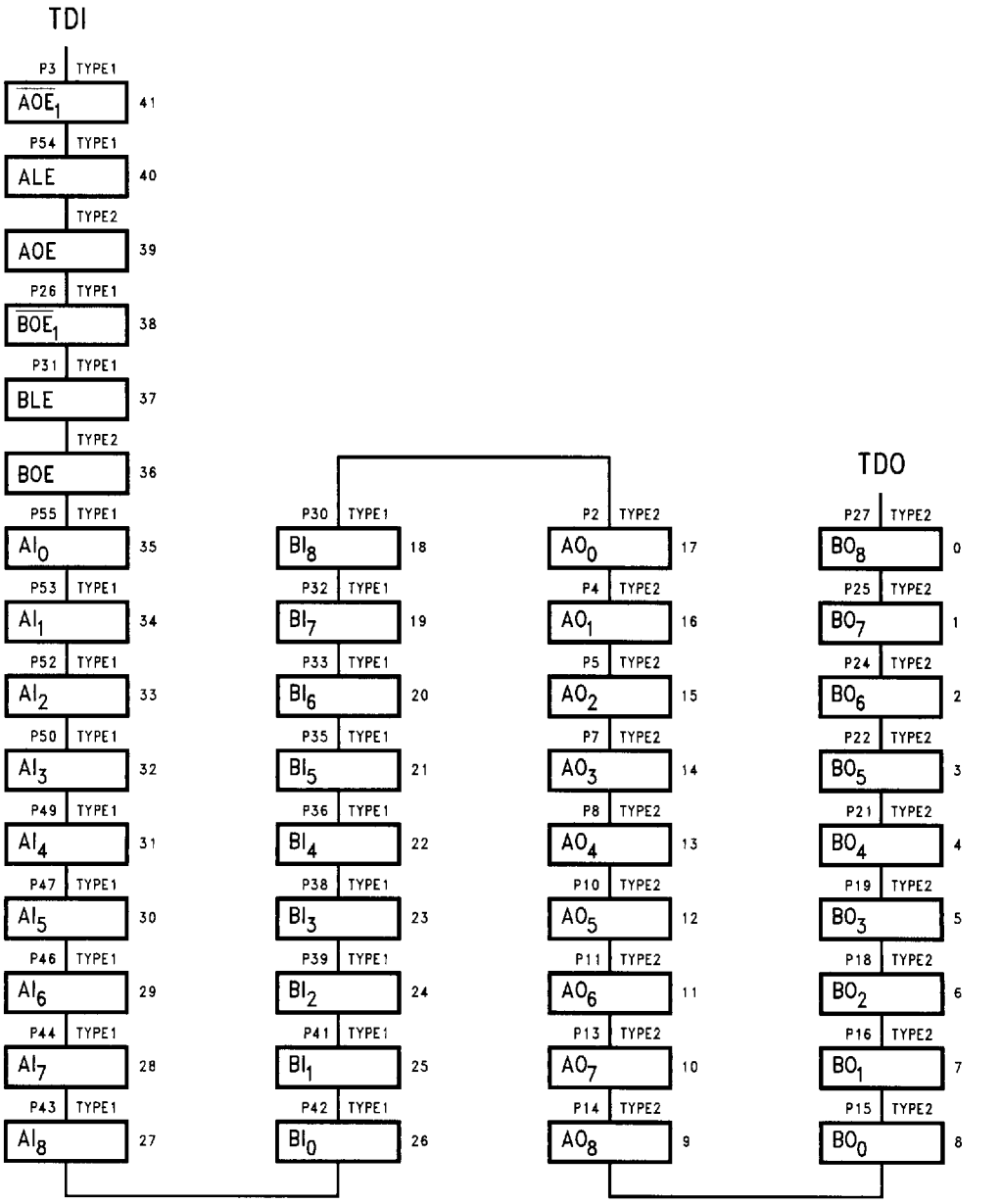
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register

Scan Chain Definition (42 Bits in Length)



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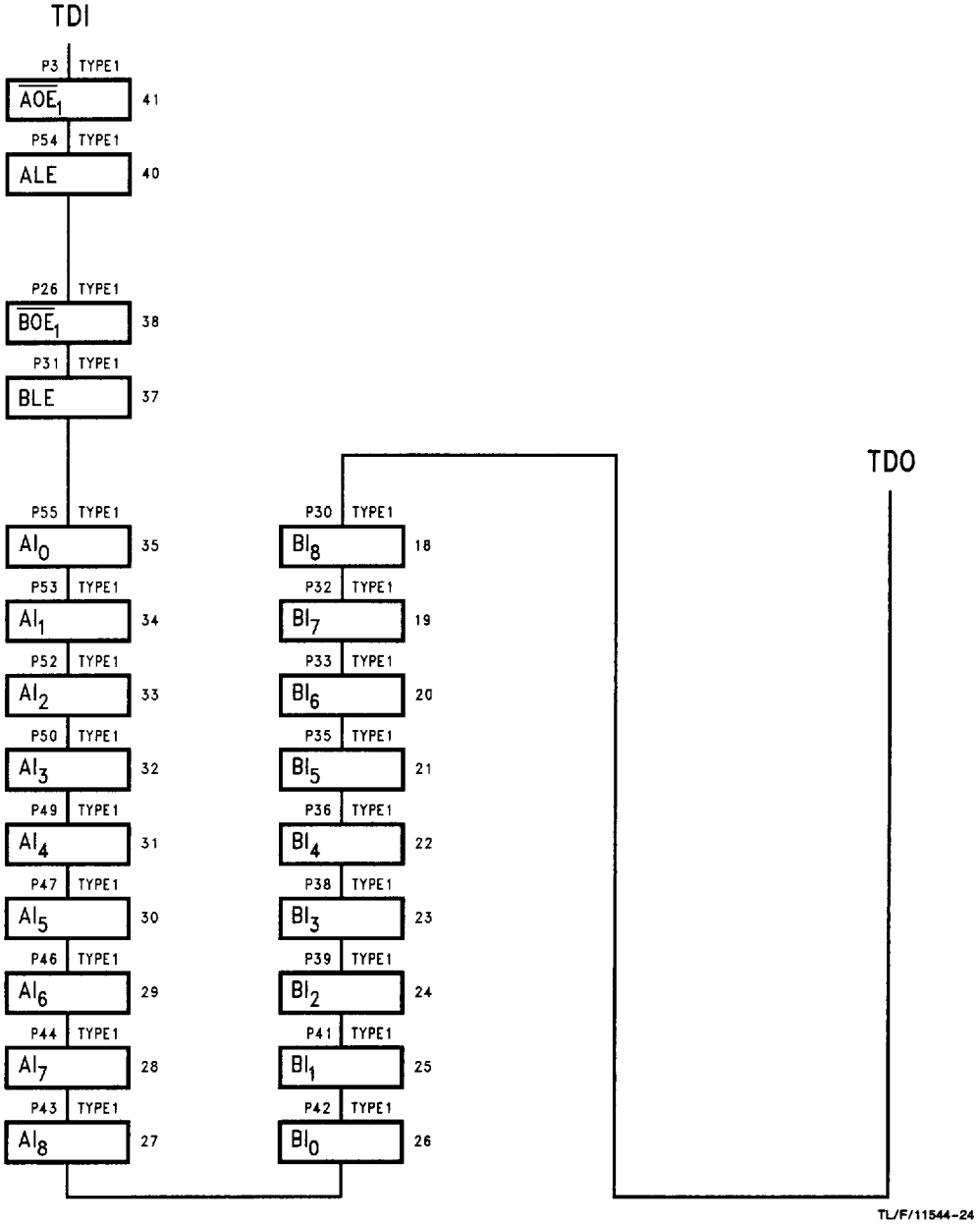
Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register

Scan Chain Definition (22 Bits in Length)
When Sample In is Active



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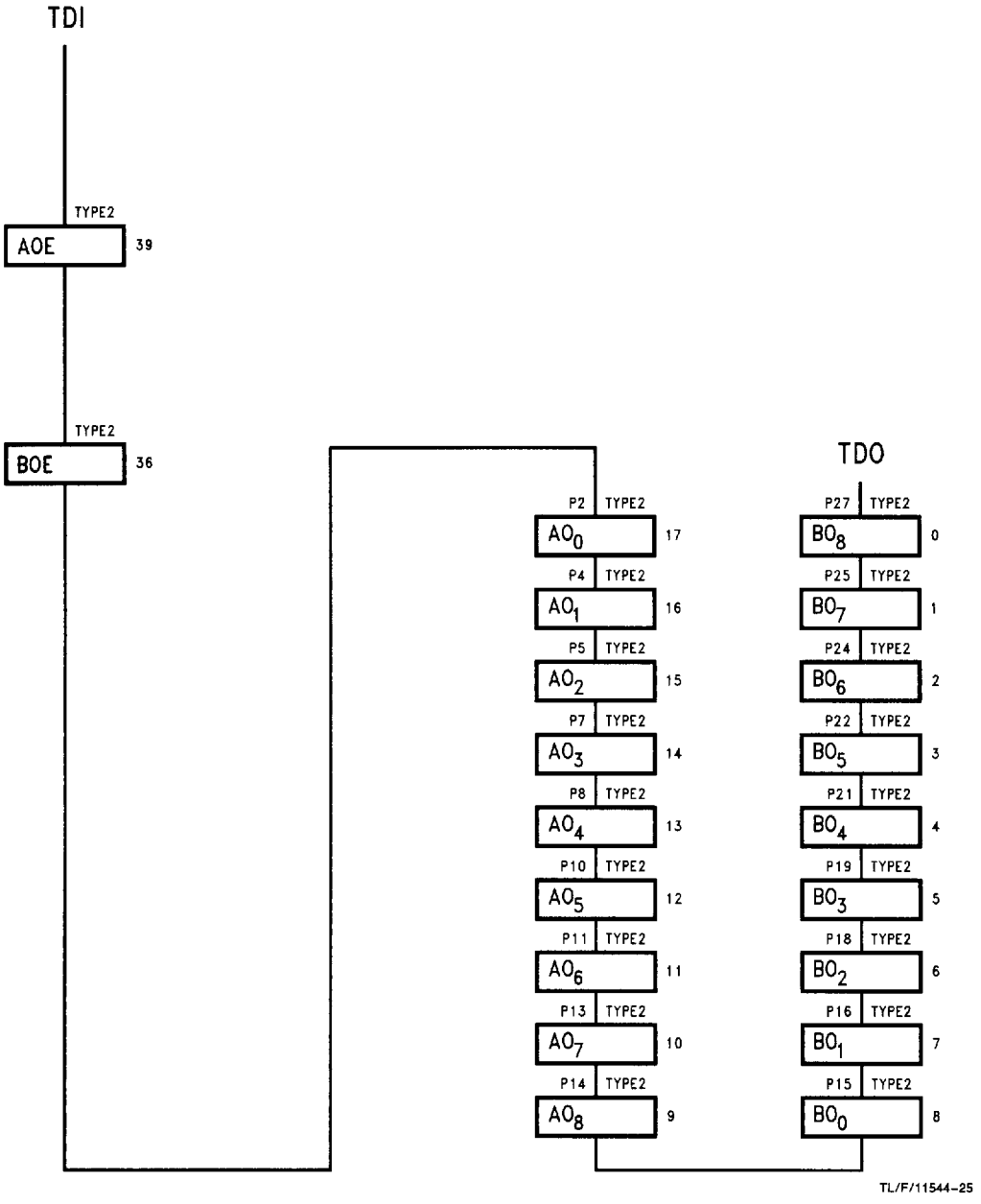
Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register

Scan Chain Definition (20 Bits in Length)
When Sample Out and Extest Out are Active



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	
40	ALE	54	Input	TYPE1	
39	AOE		Internal	TYPE2	Control
38	$\overline{BOE_1}$	26	Input	TYPE1	Signals
37	BLE	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	A-in
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	B-in
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	A-out
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	B-out
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit of current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
$I_{IL} + I_{OZL}$	Output Leakage Current		Max			−50		V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		Max	−100		−275	mA	V_{OUT} = 0.0V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
I_{CEX}	Output HIGH Leakage Current		Max			50	μA	$V_{OUT} = V_{CC}$
I_{ZZ}	Bus Drainage Test		0.0			100	μA	$V_{OUT} = 5.5V$ All Others Grounded
I_{CCH}	Power Supply Current		Max			250	μA	$V_{OUT} = V_{CC}$; TDI, TMS = V_{CC}
			Max			1.0	mA	$V_{OUT} = V_{CC}$; TDI, TMS = GND
I_{CCL}	Power Supply Current		Max			65	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
			Max			65.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current		Max			250	μA	TDI, TMS = V_{CC}
			Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input	All Other Inputs	Max			2.9	mA	$V_{IN} = V_{CC} - 2.1V$
		TDI, TMS Inputs	Max			3	mA	$V_{IN} = V_{CC} - 2.1V$
I_{CCD}	Dynamic I_{CC}	No Load	Max			0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed not tested.

AC Electrical Characteristics Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay D to Q	5.0				1.2 2.0	3.7 4.5	6.5 7.4	ns	4-1, 2
t_{PLH} t_{PHL}	Propagation Delay LE to Q	5.0				1.3 1.8	4.1 4.5	7.4 7.3	ns	4-1, 2
t_{PLZ} t_{PHZ}	Disable Time	5.0				1.6 1.8	4.9 6.0	9.0 10.7	ns	4-3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				1.6 1.0	6.0 5.0	9.5 9.3	ns	4-3, 4

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Normal Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, H or L Data to LE	5.0		1.7	ns	4-5
t_H	Hold Time, H or L LE to Data	5.0		1.6	ns	4-5
t_W	LE Pulse Width	5.0		2.3	ns	4-2

*Voltage Range 5.0V ±0.5V

AC Electrical Characteristics Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				3.6 4.8	5.8 7.4	8.6 10.6	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				2.7 4.0	5.6 7.1	9.0 10.9	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				5.2 3.6	8.6 6.6	12.5 10.1	ns	4-9, 10
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				3.9 5.1	6.4 8.0	9.5 11.6	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				4.7 5.7	7.7 9.1	11.3 13.1	ns	4-8
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				5.5 6.7	9.2 10.7	13.6 15.6	ns	4-8
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				4.1 4.7	7.7 8.4	12.1 12.7	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				4.2 4.7	8.3 9.0	13.5 14.0	ns	4-9, 10
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				5.5 6.3	10.1 10.8	15.6 16.2	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				5.8 4.3	9.6 7.7	14.2 11.7	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				6.1 4.7	11.0 9.0	16.0 13.7	ns	4-9, 10
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				7.3 5.8	12.5 10.5	18.3 15.8	ns	4-9, 10

*Voltage Range 5.0V ±0.5V

AC Operating Requirements Scan Test Operation: See Section 4

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time, Data to TCK (Note 2)	5.0		2.7	ns	4-11
t_H	Hold Time, Data to TCK (Note 2)	5.0		2.4	ns	4-11
t_S	Setup Time, H or L $\overline{AOE}_1$, $\overline{BOE}_1$ to TCK (Note 1)	5.0		5.1	ns	4-11
t_H	Hold Time, H or L TCK to $\overline{AOE}_1$, $\overline{BOE}_1$ (Note 1)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L Internal AOE, BOE, to TCK (Note 3)	5.0		3.5	ns	4-11
t_H	Hold Time, H or L TCK to Internal AOE, BOE (Note 3)	5.0		1.8	ns	4-11
t_S	Setup Time ALE, BLE (Note 4) to TCK	5.0		5.1	ns	4-11
t_H	Hold Time TCK to ALE, BLE (Note 4)	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TMS to TCK	5.0		7.9	ns	4-11
t_H	Hold Time, H or L TCK to TMS	5.0		1.8	ns	4-11
t_S	Setup Time, H or L TDI to TCK	5.0		6.0	ns	4-11
t_H	Hold Time, H or L TCK to TDI	5.0		3.0	ns	4-11
t_W	Pulse Width TCK H L	5.0		10.3 10.3	ns	4-12
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to BSR 38 and 41 only.

Note 2: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

Note 3: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

Note 4: Timing pertains to BSR 37 and 40 only.

Capacitance

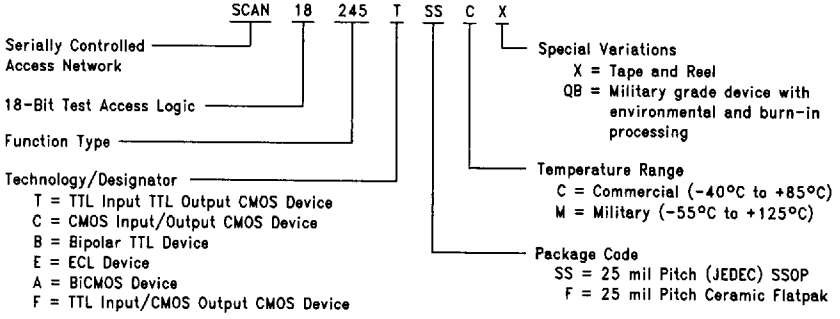
Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.8	pF	$V_{CC} = 0.0V$
C_{OUT} (Note 1)	Output Capacitance	13.8	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012

National Semiconductor

Ordering Information and Physical Dimensions

Ordering Information



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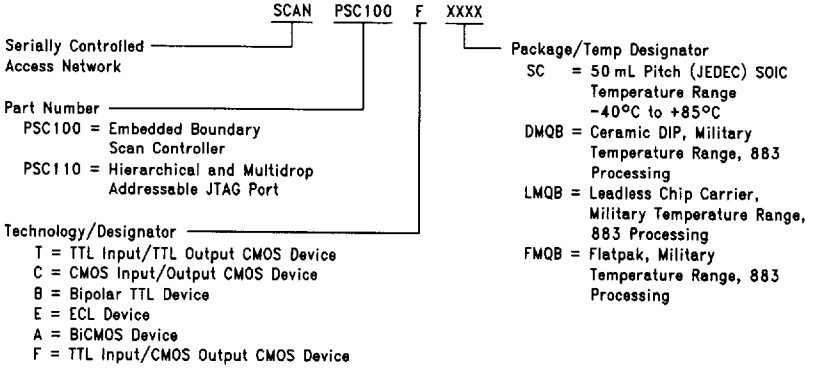


TL/F/11596–10

SSOP Package Thermal Information

THERMAL RESISTANCE FOR SSOP PACKAGES

Package	Paddle Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
20LD SSOP	110 x 144	127.0	99.4	90.1	78.5	N/A
24LD SSOP	98 x 106	117.0	91.4	82.7	73.5	N/A
24LD SSOP	120 x 150	100.8	81.3	72.1	65.7	25.7
48LD SSOP	190 x 190	75.5	58.0	51.5	44.0	21.5
56LD SSOP	190 x 190	67.8	53.0	47.4	42.1	18.5

THERMAL RESISTANCES FOR THE MILITARY FLATPAK PACKAGES

Package	Cavity Dimensions (mils)	θ_{JA} 0 LFPM (°C/W)	θ_{JA} 225 LFPM (°C/W)	θ_{JA} 500 LFPM (°C/W)	θ_{JA} 900 LFPM (°C/W)	θ_{JC}
48LD	250 x 250	74.4	58.1	50.0	43.9	6.6
56LD	250 x 250	59.8	47.9	39.0	35.1	3.4

Dry Pack

Dry Pack is moisture proof packing that is used to store SSOP devices to reduce the susceptibility of the "popcorn effect". Humidity collects inside the package by seeping through the plastic. If moisture is inside the device when the unit goes through a solder machine, the heat quickly changes the moisture to steam, and the pressurized steam pops open the package . . . thus the popcorn effect.

The Dry Pack bag is hermetically sealed and contains a small bag of desiccant which further helps to reduce moisture. All of the SCAN 56-pin SSOP devices will be shipped in Dry Pack bags. Included with the devices will be the following warning label and instructions for rebake:

Dry Pack Warning Label for Surface Mount Packages

National Semiconductor

ELECTROSTATIC SENSITIVE DEVICES
Require Proper Handling Procedures

CAUTION
This Bag Contains
MOISTURE SENSITIVE DEVICES

1. Shelf life in sealed bag: 24 months at <40°C and <90% Relative Humidity (RH).
2. Upon opening this bag, devices to be subjected to I.R., V.P.R. or equivalent process must be:
   a. Mounted within 48 hours at factory conditions of <30°C/60% RH, or
   b. Stored at <10% RH.
3. Devices require baking, before mounting, if:
   a. Humidity Indicator Card is >20% when read at 23°C ±5°C.
   b. 2a or 2b are not met.
4. If baking is required, devices may be baked for:
   a. 19 hours at 40°C +5°C/−0°C and <5% RH for low temperature device containers, or
   b. 8 hours at 125°C ±5°C for high temperature device containers.

Dry-Pack Seal Date: _____
(IF BLANK, SEE BAR CODE LABEL)

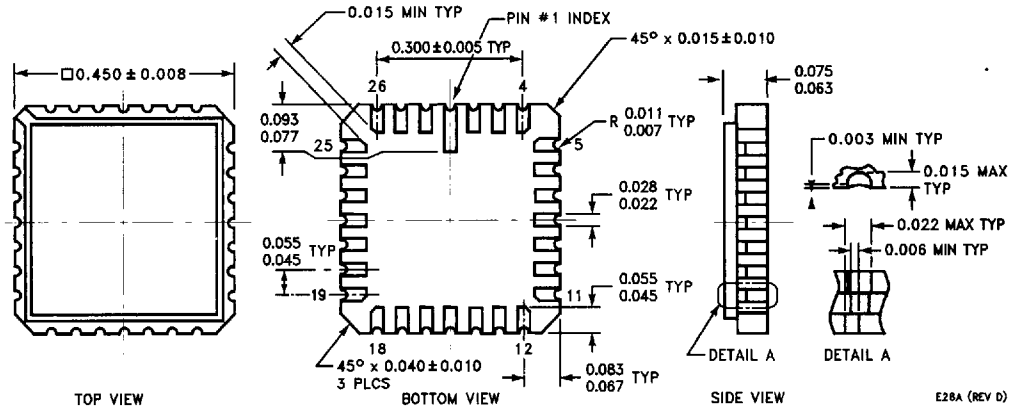
BAG SN 045317 MFR LOT No. C32729

Please follow these instructions carefully to avoid the popcorn effect.

National Semiconductor

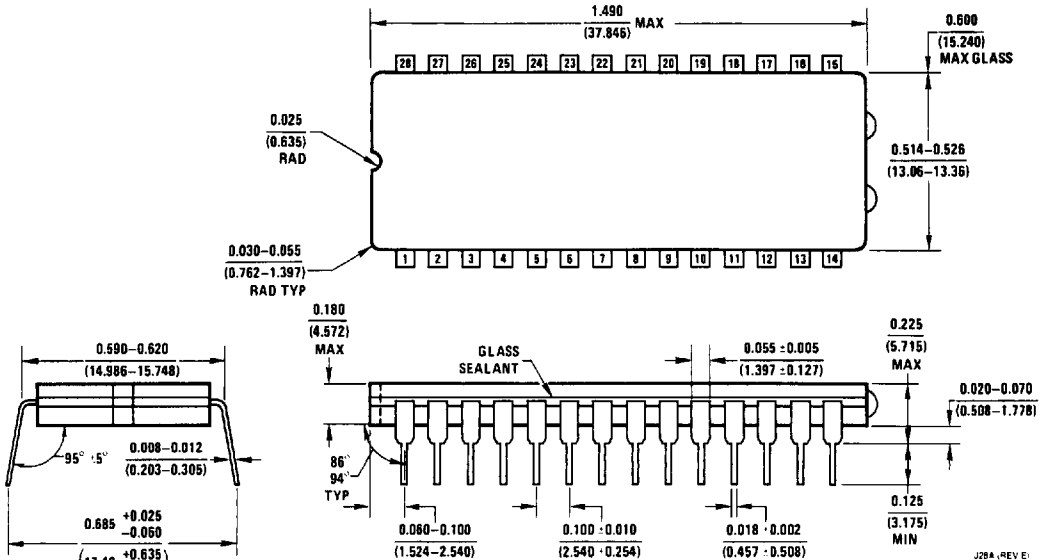
28 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A

All dimensions are in inches



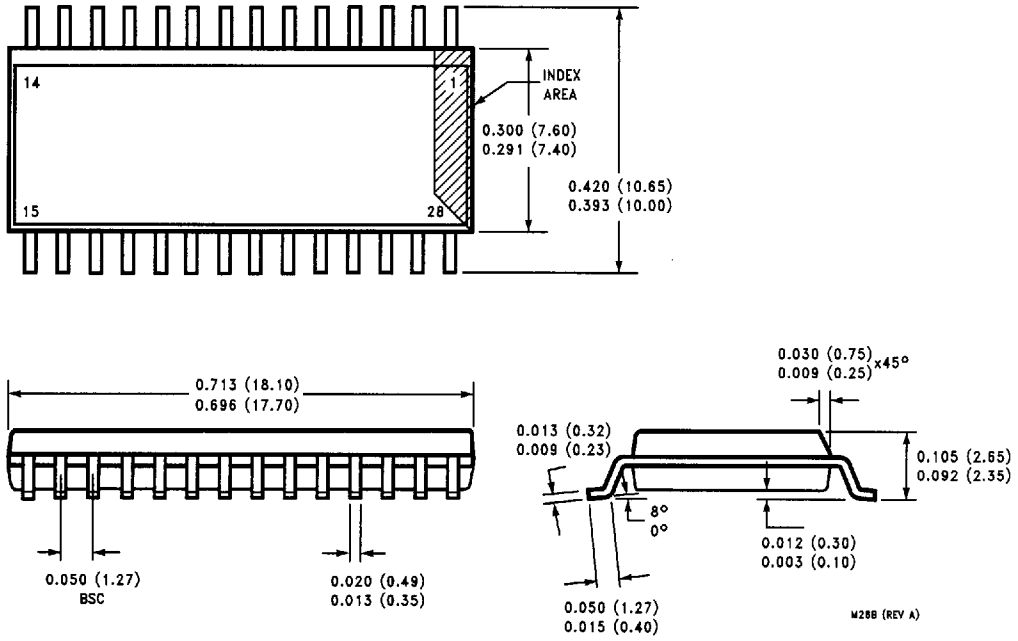
28 Lead Ceramic Dual-in-Line Package
NS Package Number J28A

All dimensions are in inches (millimeters)



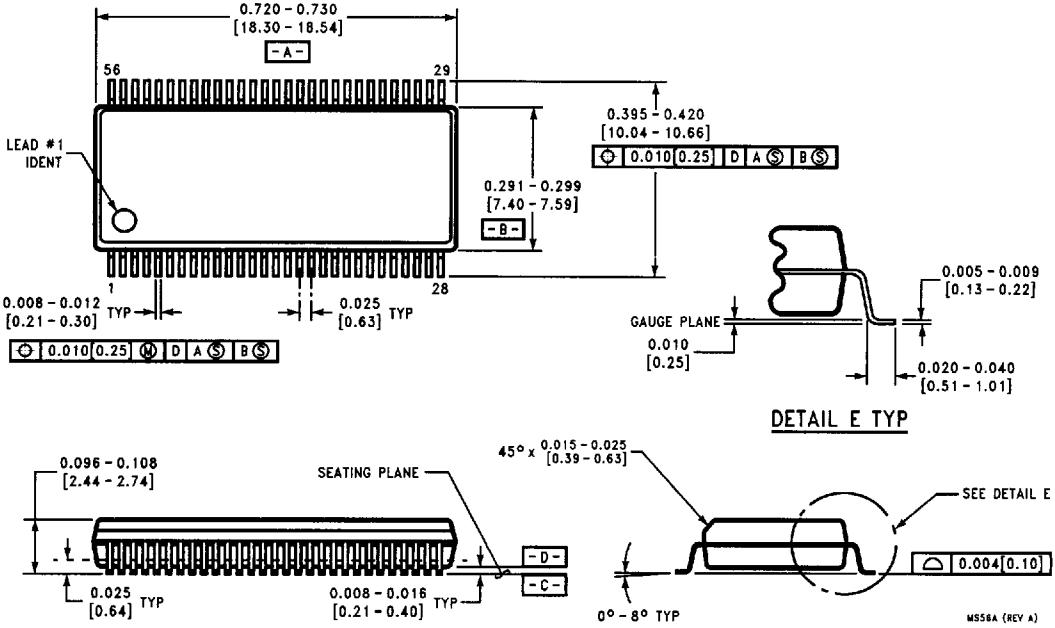
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B

All dimensions are in inches (millimeters)



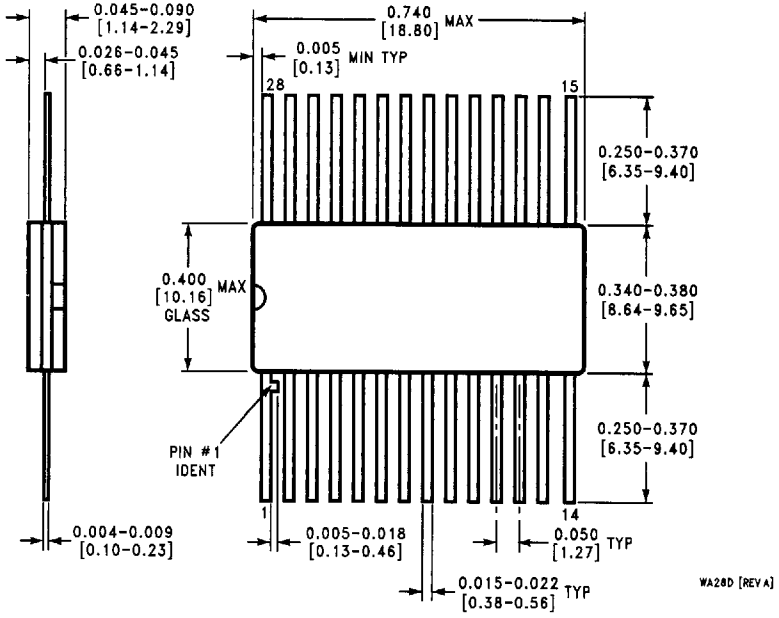
56 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS56A

All dimensions are in inches [millimeters]



28 Lead Cerpack
NS Package Number WA28D

All dimensions are in inches [millimeters]



56 Lead Cerpack
NS Package Number WA56A

All dimensions are in inches [millimeters]