

MB81C4266A-60/-70/-80/-10

CMOS 256K x 4 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 262,144 x 4 Bit Fast Page Mode with Write-Per-Bit Function Dynamic RAM

The Fujitsu MB81C4266A is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4266A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C4266A a high α -ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

PRODUCT LINE & FEATURES

Parameter	MB81C4266A-60	MB81C4266A-70	MB81C4266A-80	MB81C4266A-10
RAS Access Time	60ns max.	70ns max.	80ns max.	100ns max.
Random Cycle Time	110ns min.	125ns min.	140ns min.	170ns min.
Address Access Time	30ns max.	35ns max.	40ns max.	50ns max.
CAS Access Time	15ns max.	20ns max.	20ns max.	25ns max.
Fast Page Mode Cycle Time	40ns min.	45ns min.	45ns min.	55ns min.
Low Power Dissipation	407mW max.	374mW max.	341mW max.	297mW max.
• Operating current				
• Standby current				
	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

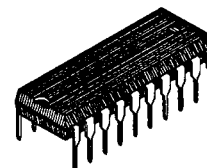
- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or \overline{OE} controlled write capability
- \overline{RAS} only, \overline{CAS} -before- \overline{RAS} , or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance
- Write-per-bit capability

ABSOLUTE MAXIMUM RATINGS (see NOTE)

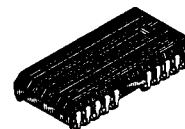
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	$^{\circ}C$

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

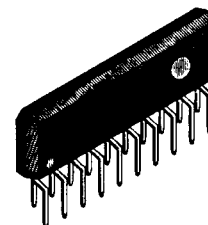
PRELIMINARY



DIP-20P-M03

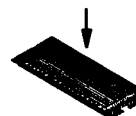
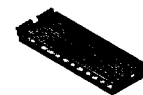


LCC-26P-M04



ZIP-20P-M02

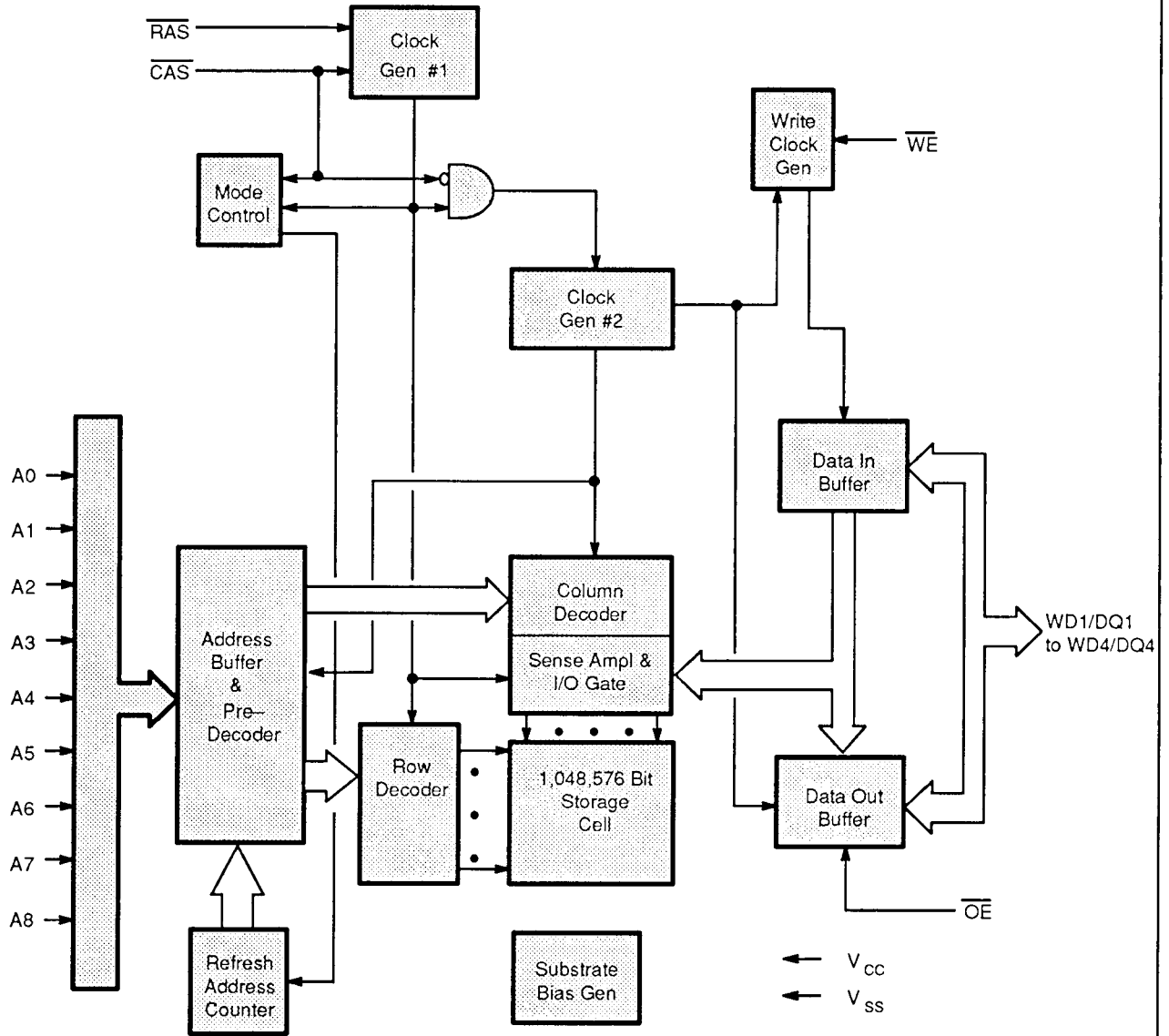
Marking side


 (Normal Bend)
*FPT-24P-M04

 Marking side
(Reverse Bend)
*FPT-24P-M05

* : Available for 70/80/100ns versions

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB81C4266A DYNAMIC RAM – BLOCK DIAGRAM

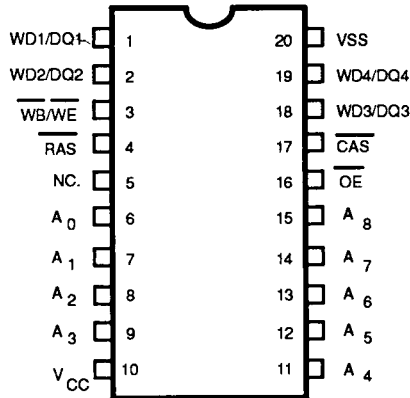


CAPACITANCE (T_A = 25°C, f = 1MHz)

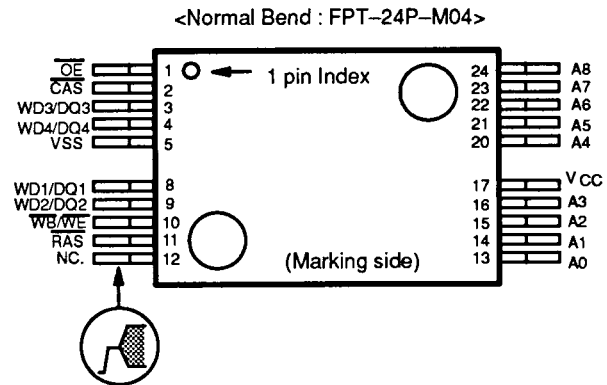
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C _{IN1}	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WB/WE}}$, $\overline{\text{OE}}$	C _{IN2}	—	5	pF
Input/Output Capacitance, WD1/DQ1 to WD4/DQ4	C _{DO}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

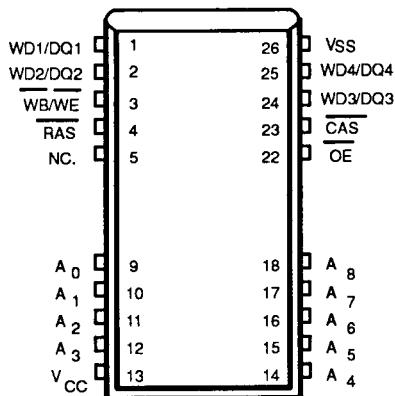
20-Pin DIP :
(TOP VIEW)



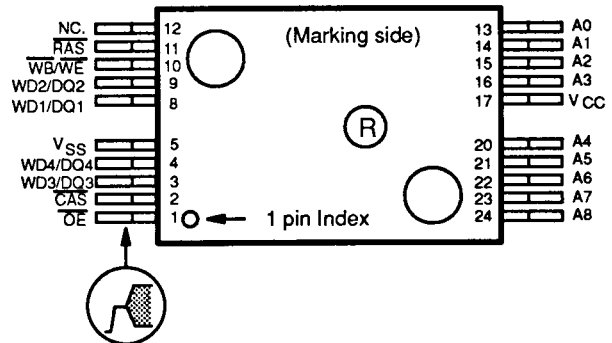
24-Pin FPT :
(TOP VIEW)



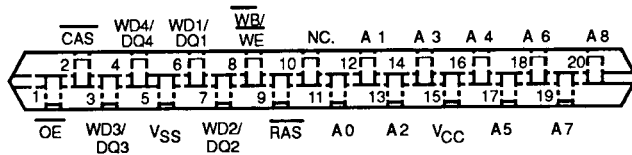
26-Pin SOJ:
(TOP VIEW)



<Reverse Bend : FPT-24P-M05>



20-Pin ZIP:
(TOP VIEW)



Designator	Function
WD1/DQ1 to WD4/DQ4	Data Input/ Output
WB/WE	Write Enable.
RAS	Row address strobe.
NC	No connection.
A ₀ to A ₈	Address inputs.
V _{CC}	+5 volt power supply.
OE	Output enable.
CAS	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V _{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V _{SS}	0	0	0		
Input High Voltage, all inputs	1	V _{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V _{IL}	-2.0	—	0.8	V	
Input Low Voltage, WD/DQ(*)	1	V _{ILD}	-1.0	—	0.8	V	

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ as shown in Figure 1. First, nine row address bits are input on pins A0 through A8 and latched with the row address strobe ($\overline{\text{RAS}}$) then, nine column address bits are input and latched with the column address strobe ($\overline{\text{CAS}}$). Both row and column addresses must be stable on or before the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_{T} is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{\text{WB/WE}}$. When $\overline{\text{WB/WE}}$ is active Low, a write cycle is initiated; when $\overline{\text{WB/WE}}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{\text{OE}}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{\text{WB/WE}}$ or $\overline{\text{CAS}}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (WD1/DQ1 to WD4/DQ4) is strobed by $\overline{\text{CAS}}$ and the setup/hold times are referenced to $\overline{\text{CAS}}$ because $\overline{\text{WB/WE}}$ goes Low before $\overline{\text{CAS}}$. In a delayed write or a read-modify-write cycle, $\overline{\text{WB/WE}}$ goes Low after $\overline{\text{CAS}}$; thus, input data is strobed by $\overline{\text{WB/WE}}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{TRAC}** : from the falling edge of $\overline{\text{RAS}}$ when t_{RCD} (max) is satisfied.
- t_{TCAC}** : from the falling edge of $\overline{\text{CAS}}$ when t_{RCD} is greater than t_{RCD} , t_{RAD} (max).
- t_{TAA}** : from column address input when t_{RAD} is greater than t_{RAD} (max).
- t_{IOEA}** : from the falling edge of $\overline{\text{OE}}$ when $\overline{\text{OE}}$ is brought Low after t_{TRAC} , t_{TCAC} , or t_{TAA} .

The data remains valid until either $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		V_{OH}	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output low voltage		V_{OL}	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	$0V \leq V_{IN} \leq 5.5V$; $4.5V \leq V_{CC} \leq 5.5V$; $V_{SS} = 0V$; All other pins under test = $0V$	-10	—	10	μA
Output leakage current		$I_{O(L)}$	$0V \leq V_{OUT} \leq 5.5V$; Data out disabled	-10	—	10	μA
Operating current (Average Power supply Current) 2	MB81C4266A-60	I_{CC1}	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C4266A-70					68	
	MB81C4266A-80					62	
	MB81C4266A-10					54	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2V$			1.0	
Refresh current #1 (Average power sup- ply current) 2	MB81C4266A-60	I_{CC3}	$\overline{\text{CAS}} = V_{IH}$, $\overline{\text{RAS}}$ cycling; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C4266A-70					68	
	MB81C4266A-80					62	
	MB81C4266A-10					54	
Fast Page Mode current 2	MB81C4266A-60	I_{CC4}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling; $t_{PC} = \text{min}$	—	—	61	mA
	MB81C4266A-70					56	
	MB81C4266A-80					56	
	MB81C4266A-10					46	
Refresh current #2 (Average power sup- ply current) 2	MB81C4266A-60	I_{CC5}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C4266A-70					68	
	MB81C4266A-80					62	
	MB81C4266A-10					54	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4266A-60		MB81C4266A-70		MB81C4266A-80		MB81C4266A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	140	—	170	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	165	—	190	—	230	—	ns
4	Access Time from \overline{RAS}	6,9	t_{RAC}	—	60	—	70	—	80	—	100	ns
5	Access Time from \overline{CAS}	7,9	t_{CAC}	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		t_{OH}	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	15	—	20	—	20	ns
10	Transition Time		t_T	2	50	2	50	2	50	2	50	ns
11	\overline{RAS} Precharge Time		t_{RP}	40	—	45	—	50	—	60	—	ns
12	\overline{RAS} Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	100	100000	ns
13	\overline{RAS} Hold Time		t_{RSH}	15	—	20	—	20	—	25	—	ns
14	\overline{CAS} to \overline{RAS} Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	\overline{RAS} to \overline{CAS} Delay Time	11,12	t_{RCD}	20	45	20	50	20	60	25	75	ns
16	\overline{CAS} Pulse Width		t_{CAS}	15	—	20	—	20	—	25	—	ns
17	\overline{CAS} Hold Time		t_{CSH}	60	—	70	—	80	—	100	—	ns
18	\overline{CAS} Precharge Time (C-B-R cycle)	19	t_{CPN}	10	—	10	—	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	10	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	15	—	15	—	ns
23	\overline{RAS} to Column Address Delay Time	13	t_{RAD}	15	30	15	35	15	40	20	50	ns
24	Column Address to \overline{RAS} Lead Time		t_{RAL}	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to \overline{RAS}	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to \overline{CAS}	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	10	—	10	—	12	—	15	—	ns
30	\overline{WE} Pulse Width		t_{WP}	10	—	10	—	12	—	15	—	ns
31	Write Command to \overline{RAS} Lead Time		t_{RWL}	15	—	15	—	20	—	25	—	ns
32	Write Command to \overline{CAS} Lead Time		t_{CWL}	12	—	12	—	15	—	20	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	10	—	10	—	12	—	15	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4266A-60		MB81C4266A-70		MB81C4266A-80		MB81C4266A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	RAS Precharge time to CAS Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	CAS Set Up Time for CAS-before-RAS Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	CAS Hold Time for CAS-before-RAS Refresh		t_{CHR}	10	—	10	—	12	—	15	—	ns
38	Access Time from OE	9	t_{OEA}	—	15	—	20	—	20	—	20	ns
39	Output Buffer Turn Off Delay from OE	10	t_{OEZ}	—	15	—	15	—	20	—	25	ns
40	OE to RAS Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	OE Hold Time Referenced to WE	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	OE to Data In Delay Time		t_{OED}	15	—	15	—	20	—	25	—	ns
43	DIN to CAS Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to OE Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	45	—	55	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	77	—	82	—	90	—	110	—	ns
52	Access Time from CAS Precharge	9,18	t_{CPA}	—	35	—	40	—	40	—	50	ns
53	Fast Page Mode CAS Precharge Time		t_{CP}	10	—	10	—	10	—	10	—	ns
54	Write Per Bit Set Up Time		t_{WBS}	0	—	0	—	0	—	0	—	ns
55	Write Per Bit Hold Time		t_{WBH}	10	—	10	—	10	—	15	—	ns
56	Write Per Bit Select Set Up Time		t_{WDS}	0	—	0	—	0	—	0	—	ns
57	Write Per Bit Select Hold Time		t_{WDH}	10	—	10	—	10	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
Icc depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
Icc4 is specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
3. An Initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μ s is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
4. AC characteristics assume $t_T = 5$ ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}(\max)$, $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}(\max)$, $t_{RAD} \geq t_{RAD}(\max)$. If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
8. If $t_{RAD} \geq t_{RAD}(\max)$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$
13. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}(\min)$ the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}(\min)$
17. Either t_{DZC} or t_{DZO} must be satisfied.

Notes: (continued)

18. t_{CPA} is access time from the selection of a new column address (that is caused by changing \overline{CAS} from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than $t_{CPA}(\max)$.

19. Assumes that \overline{CAS} -before- \overline{RAS} refresh only.

Fig. 2 - t_{RAC} vs. t_{RCD}

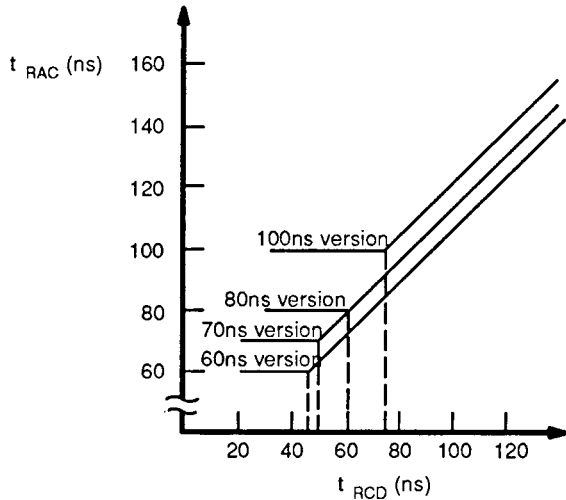
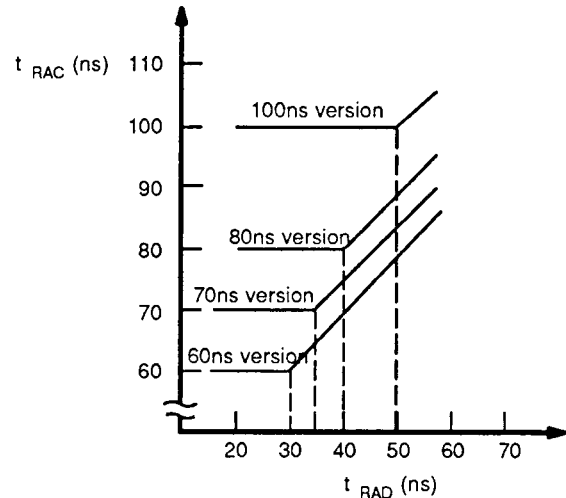


Fig. 3 - t_{RAC} vs. t_{RAD}



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	RAS	CAS	$\overline{WB/WE}$	\overline{OE}	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	Yes *	$t_{RCS} \geq t_{RCS}(\min)$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes *	$t_{WCS} \geq t_{WCS}(\min)$
Read-Modify- Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes *	
\overline{RAS} -only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
\overline{CAS} -before- \overline{RAS} Refresh Cycle	L	L	X	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{WCSR}(\min)$
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	Yes	Previous data is kept.

X; "H" or "L"

*; It is impossible in Fast Page Mode

FUNCTIONAL TRUTH TABLE FOR WRITE-PER-BIT

Input Level at falling of \overline{RAS}		Write Per Bit
$\overline{WB}/\overline{WE}$	WD1/DQ1 to WD4/DQ4	
H	X	Write enable for WD1/DQ1 to WD4/DQ4
L	H	Write enable
	L	Inhibit of writing (Mask)

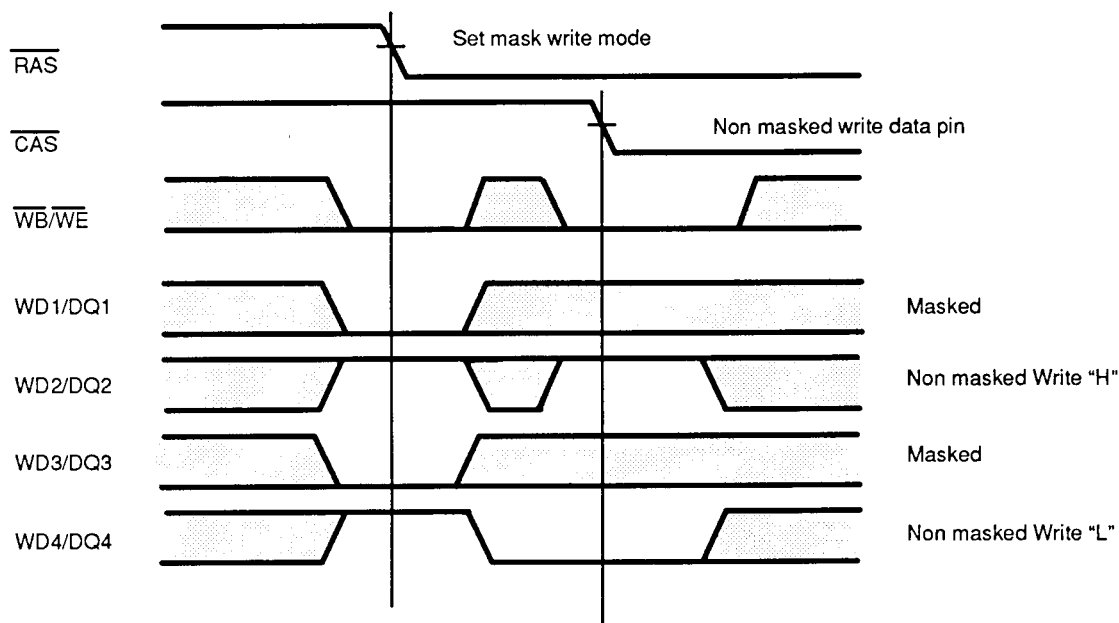
X : "H" or "L"

EXAMPLE OF WRITE-PER-BIT OPERATION

Falling edge of \overline{RAS}					Function
$\overline{WB}/\overline{WE}$	WD1 / DQ 1	WD2 / DQ 2	WD3 / DQ3	WD4 / DQ4	
H	X	X	X	X	Write enable
L	L	H	L	H	Write enable for DQ2 and DQ4 Write masked for DQ1 and DQ3

X : "H" or "L"

Fig. 4 – EXAMPLE OF WRITE-PER-BIT OPERATION



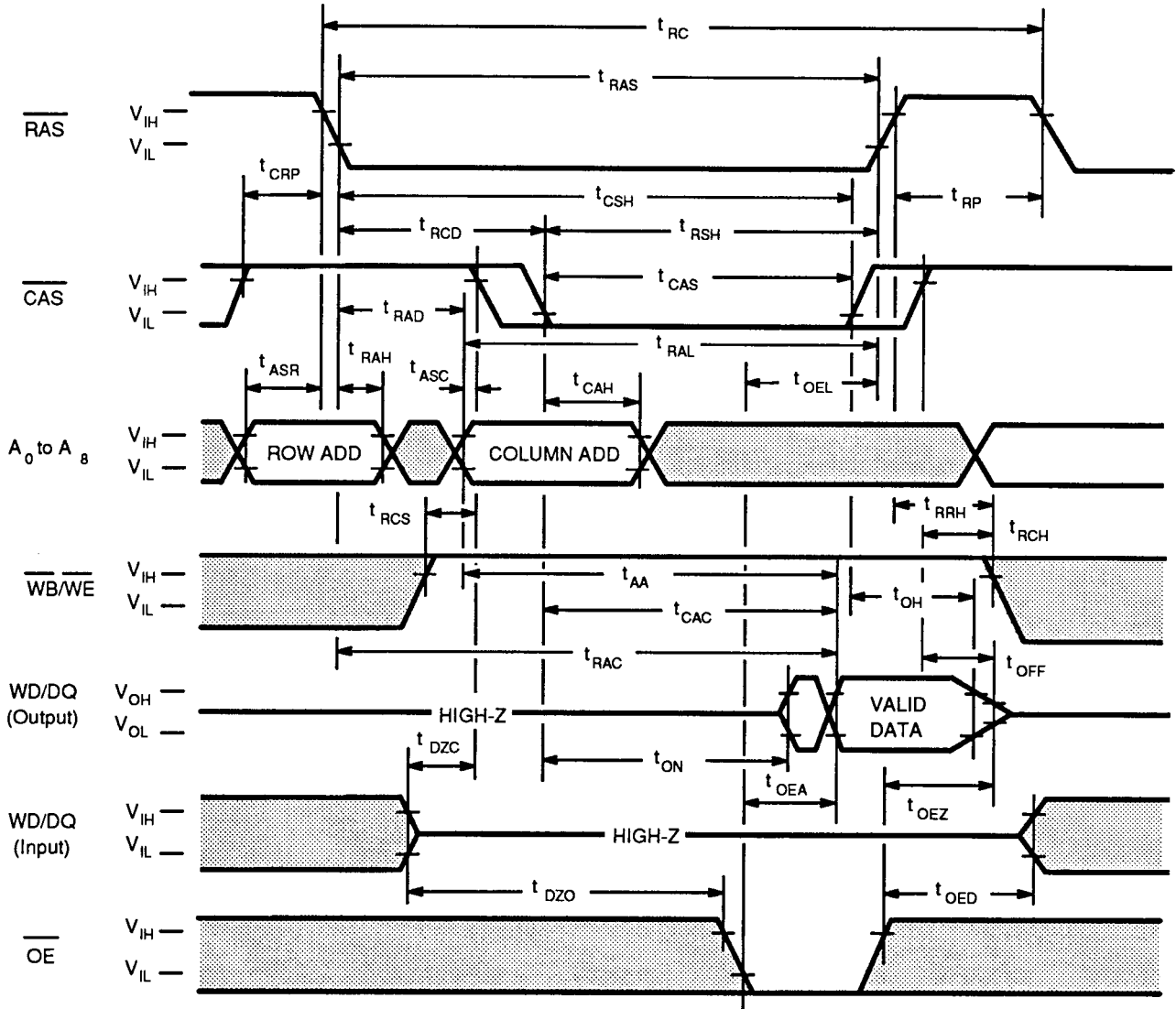
Note) A0 to A8, \overline{OE} : "H" or "L"

 "H" or "L"

DESCRIPTION

The write-per-bit function is executed by setting \overline{WE} ="L" at the falling edge of \overline{RAS} during write mode. At that time, the state of "H" or "L" on the WD/DQ pins is latched. For example, if WD1/DQ1, WD3/DQ3 and \overline{WE} are both low at the falling edge of \overline{RAS} , the new data on WD1/DQ1 and WD3/DQ3 pins are written into the cells during cycle. And if WD2/DQ2 and WD4/DQ4 are both high at the falling edge of \overline{RAS} , the data on WD2/DQ2 and WD4/DQ4 pins are written into the cells during cycle. The mask data is solved by setting \overline{RAS} ="H".

Fig. 5 – READ CYCLE



 "H" or "L"

DESCRIPTION

To implement a read operation, a valid address is latched in by the \overline{RAS} and \overline{CAS} address strobes and with $\overline{WB/WE}$ set to a High level and \overline{OE} set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}(t_{RAC})$, $\overline{CAS}(t_{CAC})$, \overline{OE} (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

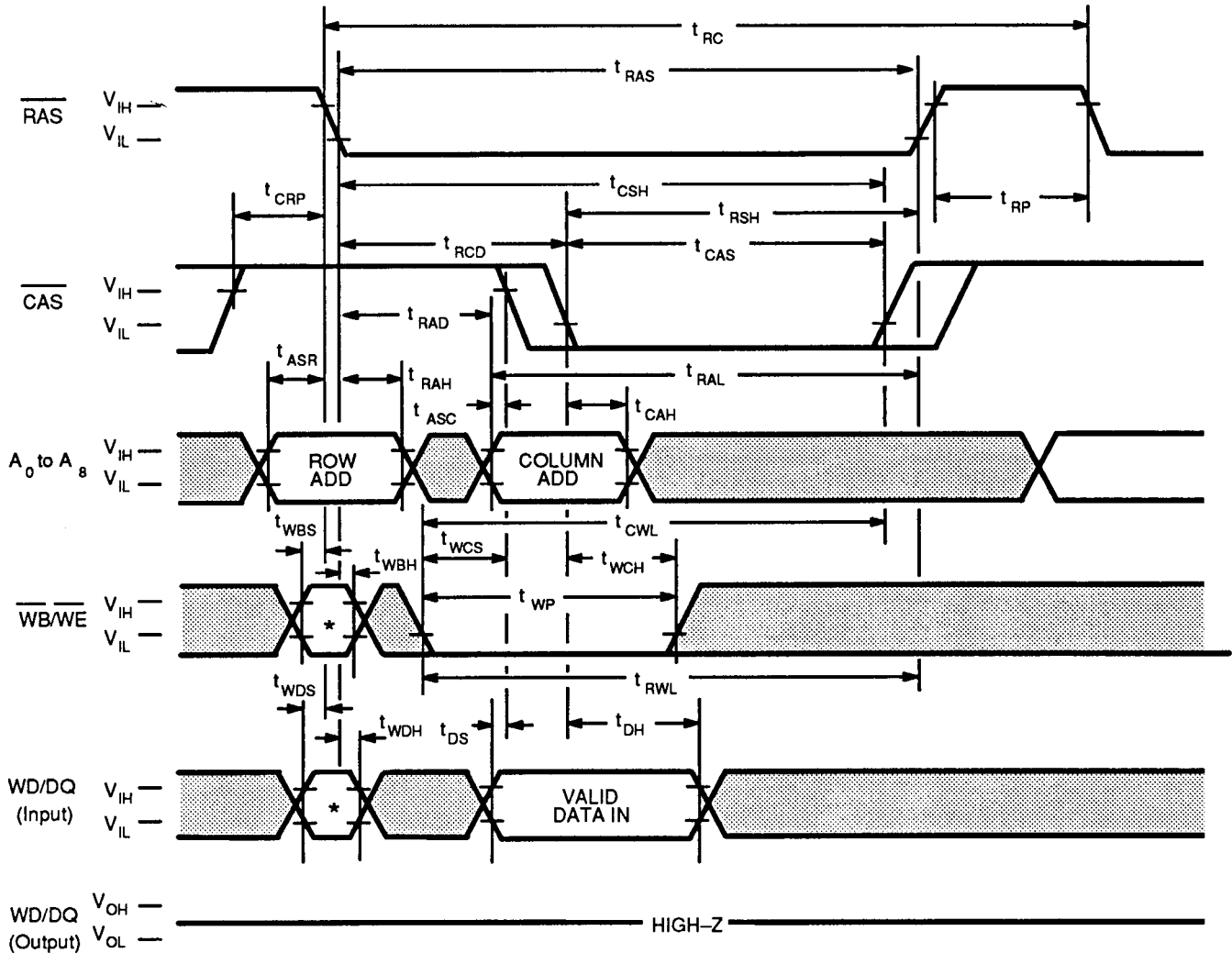
If $t_{RCD} > t_{RCD}(\text{max})$, access time = t_{CAC} .

If $t_{RAD} > t_{RAD}(\text{max})$, access time = t_{AA} .

If \overline{OE} is brought Low after t_{RAC} , t_{CAC} , or t_{AA} (which ever occurs later), access time = t_{OEA} .

However, if either \overline{CAS} or \overline{OE} goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

Fig. 6 – EARLY WRITE CYCLE ($\overline{OE} = \text{“H” or “L”}$)



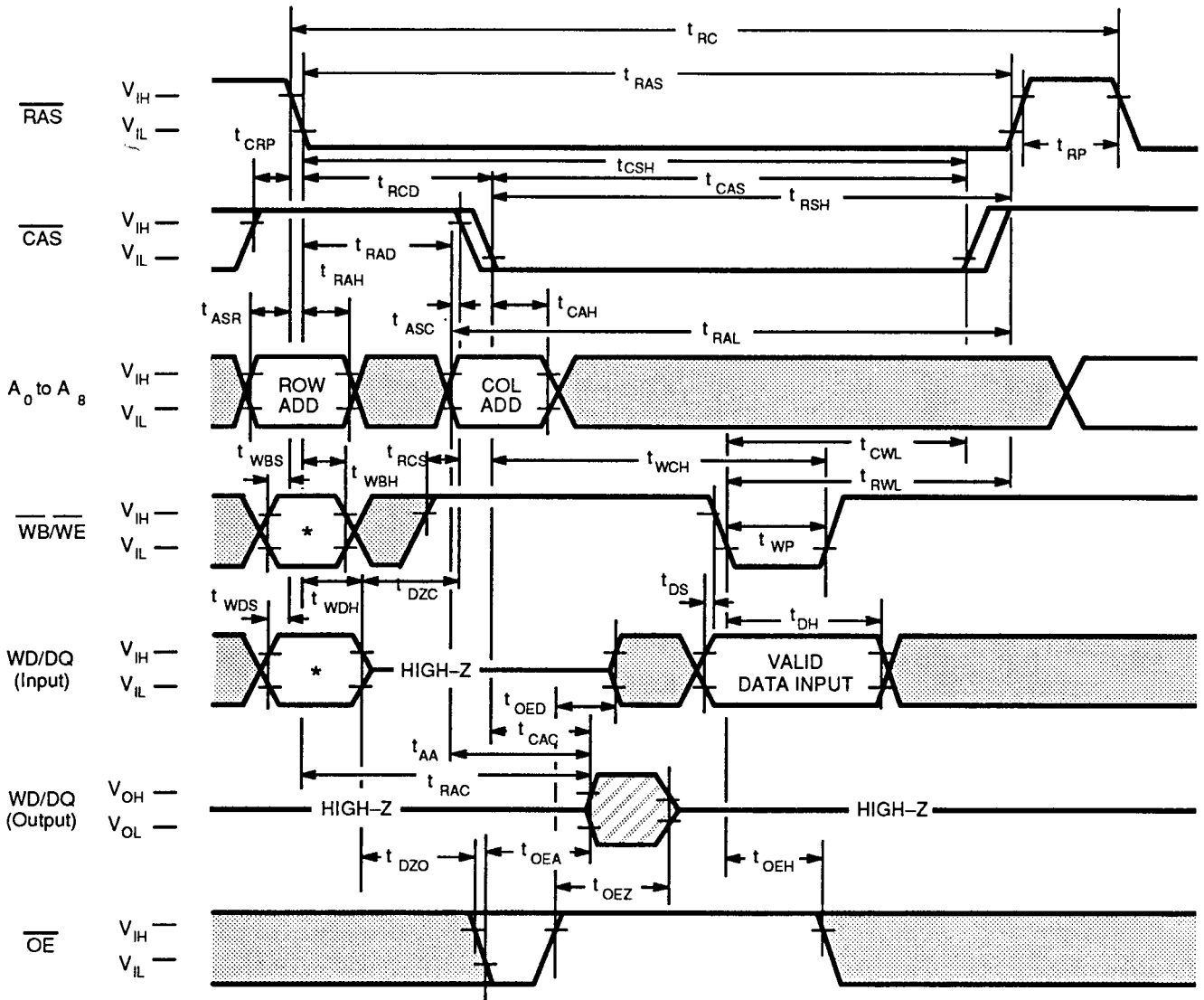
* : When $\overline{WB/WE} = \text{“H”}$, all data on the WD/DQ can be written into cell.
 When $\overline{WB/WE} = \text{“L”}$, the data on the WD/DQ are not written(masked).





DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WB/WE}$ is set to a Low state and \overline{OE} is a “H” or “L” signal. A write cycle can be implemented in either of three ways – early write, \overline{OE} write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL} , t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pin is latched with the falling edge of \overline{CAS} and written into memory.

Fig. 7 - \overline{OE} (DELAYED WRITE CYCLE)



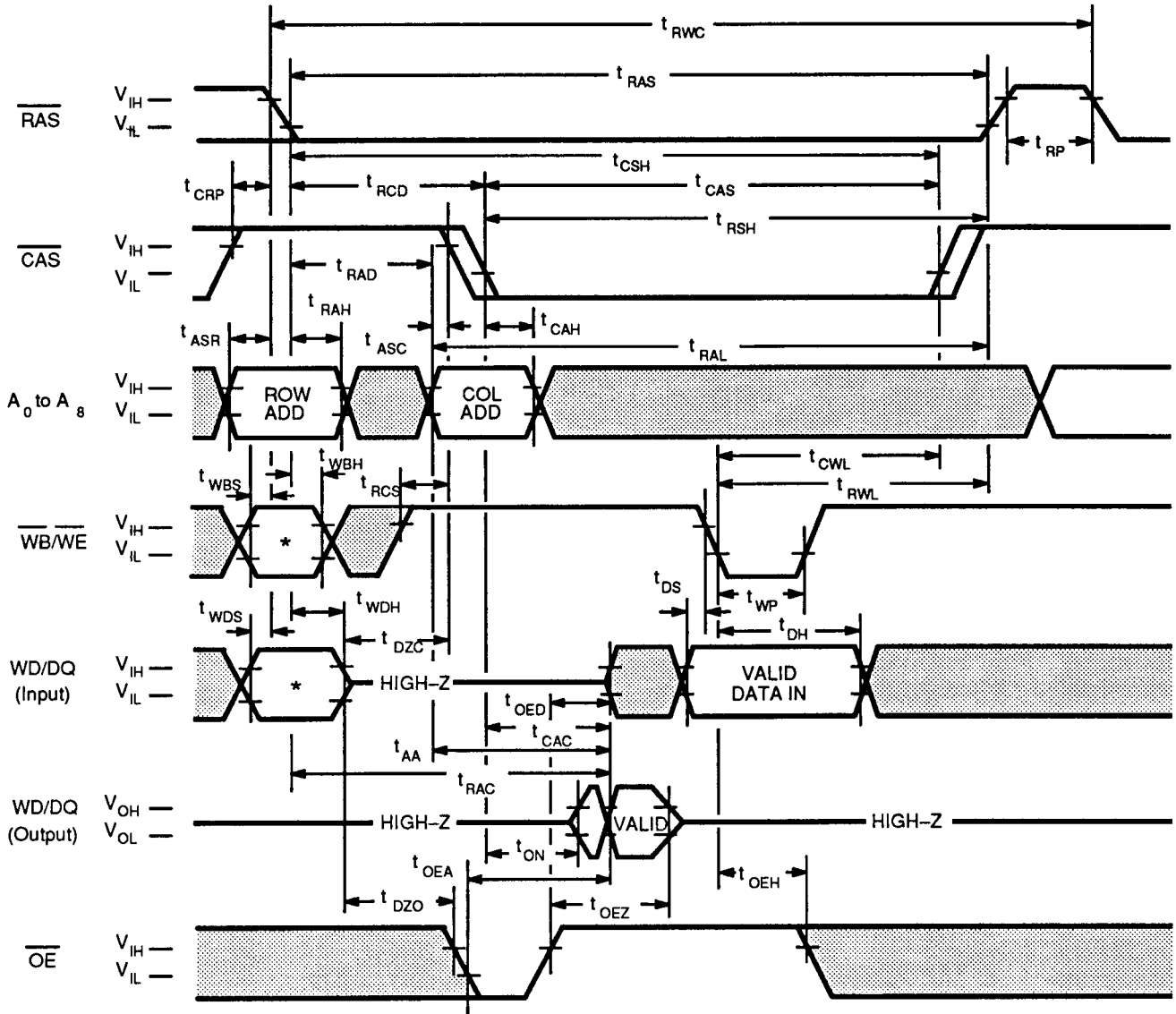
* : When $\overline{WB/WE} = "H"$, all data on the WD/DQ can be written into cell.
 When $\overline{WB/WE} = "L"$, the data on the WD/DQ are not written(masked).

 "H" or "L"
 Invalid Data

DESCRIPTION

In the \overline{OE} (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the WD/DQ pins is latched with the falling edge of $\overline{WB/WE}$ and written into memory. The Output Enable (\overline{OE}) signal must be changed from Low to High before $\overline{WB/WE}$ goes Low ($t_{OED} + t_{DS}$).

Fig. 8 – READ-MODIFY-WRITE CYCLE



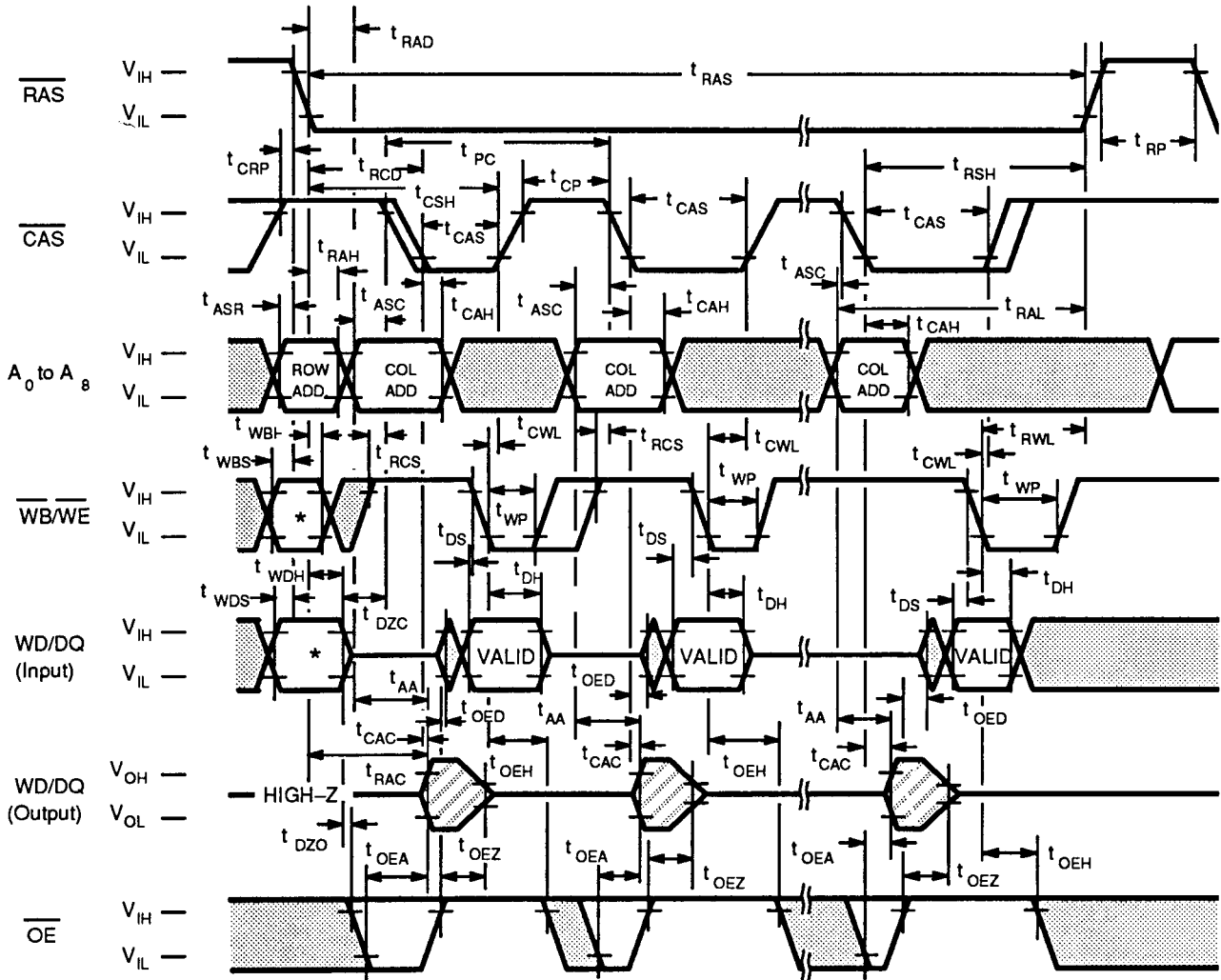
* : When $\overline{WB/WE} = \text{"H"}$, all data on the WD/DQ can be written into cell.
 When $\overline{WB/WE} = \text{"L"}$, the data on the WD/DQ are not written (masked).

 "H" or "L"

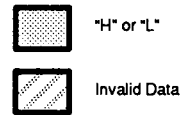
DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WB/WE}$ from High to Low after the data appears on the WD/DQ pins. In the read-modify-write cycle, \overline{OE} must be changed from Low to High after the memory access time.

Fig. 11 – FAST PAGE MODE $\overline{\text{OE}}$ WRITE CYCLE



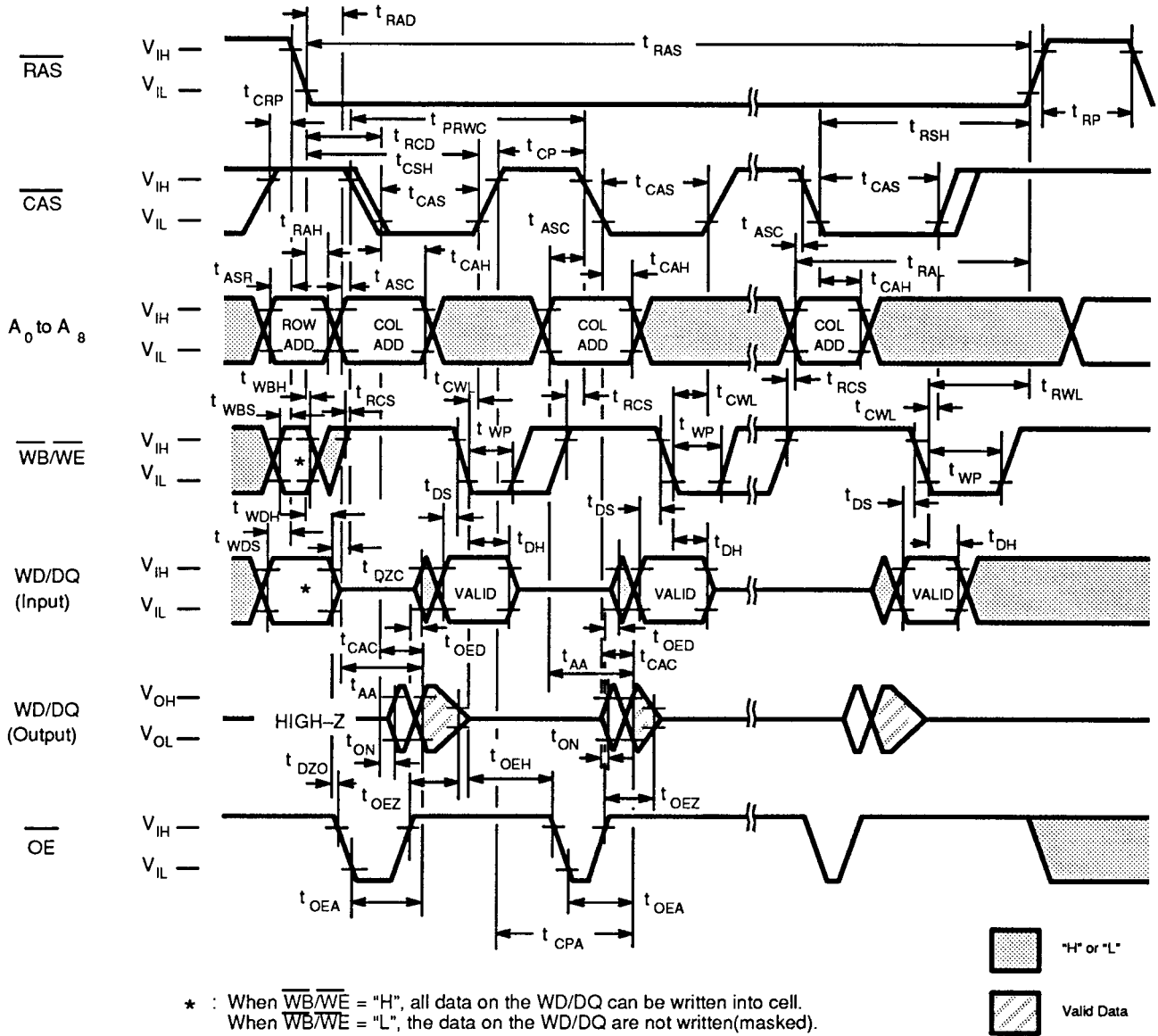
* : When $\overline{\text{WB/WE}}$ = "H", all data on the WD/DQ can be written into cell.
 When $\overline{\text{WB/WE}}$ = "L", the data on the WD/DQ are not written (masked).



DESCRIPTION

The fast page mode $\overline{\text{OE}}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{\text{WB/WE}}$ and $\overline{\text{OE}}$. Input data on the WD/DQ pins are latched on the falling edge of $\overline{\text{WB/WE}}$ and written into memory. In the fast page mode delayed write cycle, $\overline{\text{OE}}$ must be changed from Low to High before $\overline{\text{WB/WE}}$ goes Low ($t_{\text{OED}} + t_{\text{DS}}$).

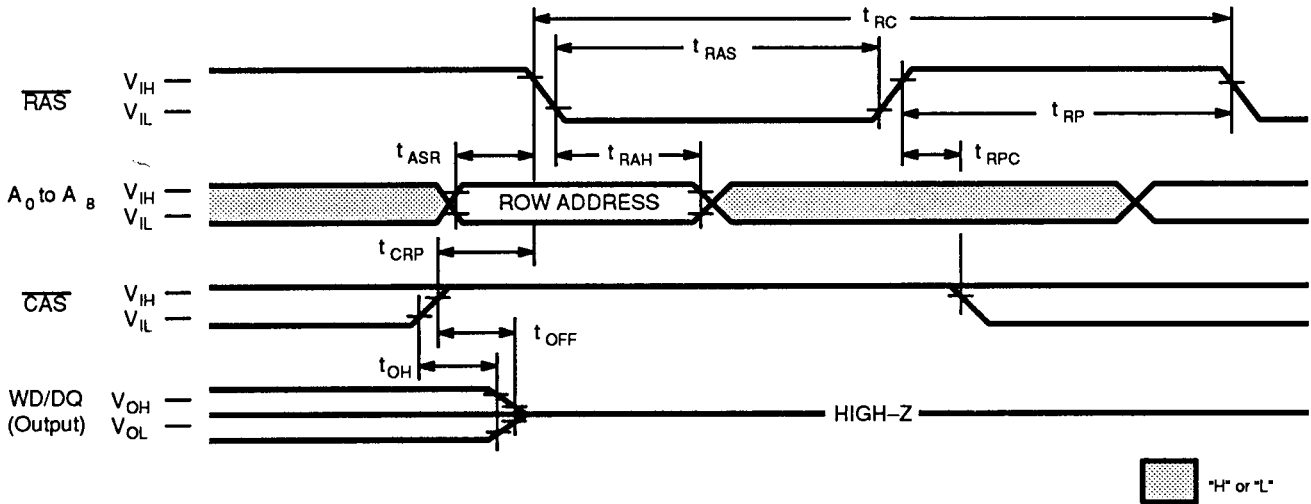
Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WB/WE}$ from High to Low after input data appears at the WD/DQ pins during a normal cycle.

Fig. 13 - $\overline{\text{RAS}}$ -ONLY REFRESH ($\overline{\text{WB}}/\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$)

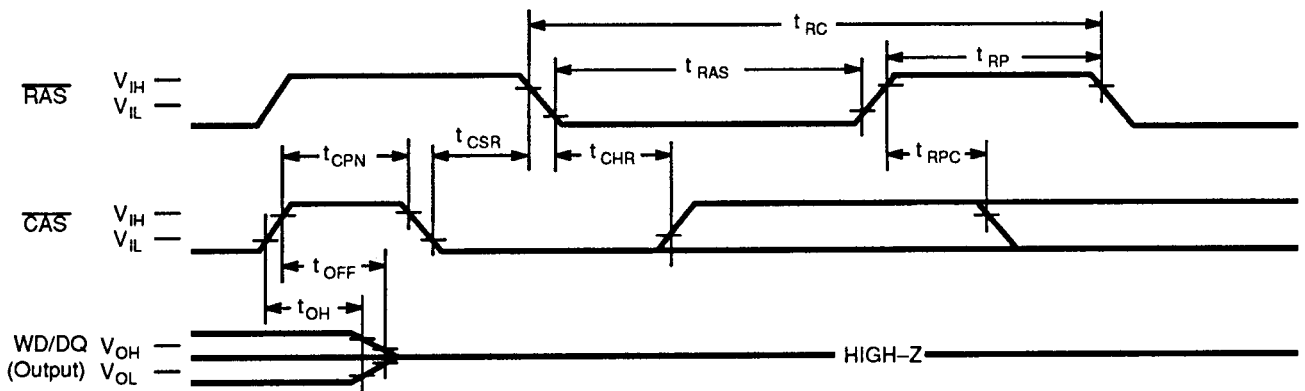


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{CAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$ -only refresh, WD/DQ pins are kept in a high-impedance state.

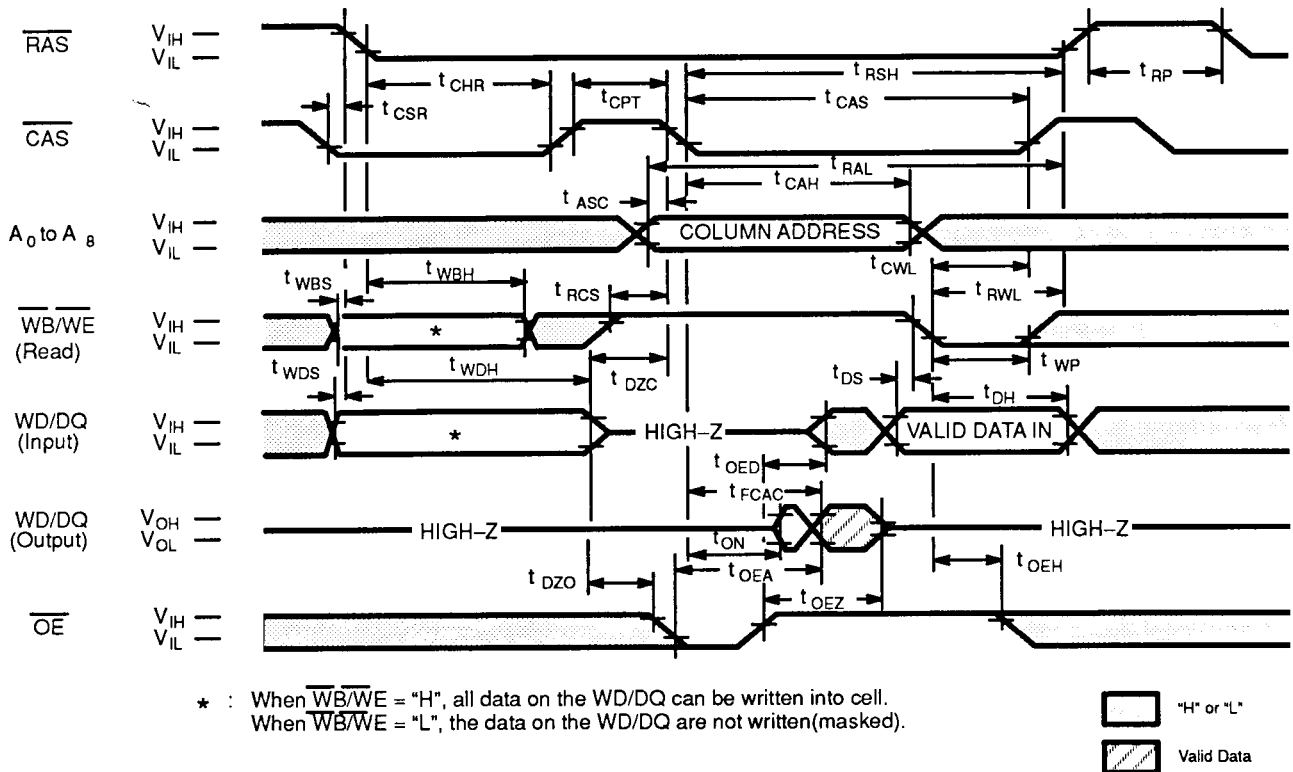
Fig. 14 - $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH (ADDRESSES = $\overline{\text{WB}}/\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$)



DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation.

Fig. 16 – $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh circuitry. If, after a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle, $\overline{\text{CAS}}$ makes a transition from High to Low while $\overline{\text{RAS}}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.

Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{\text{CAS}}$.

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test procedure is as follows ;

- 1) Initialize the internal refresh address counter by using 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 512 row addresses (WD1/DQ1 to WD4/DQ4) at the same column address by using normal write cycles.
- 4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test (read-modify-write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
- 5) Read and check data written in procedure 4) by using normal read cycle for all 512 (WD1/DQ1 to WD4/DQ4) memory locations.
- 6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

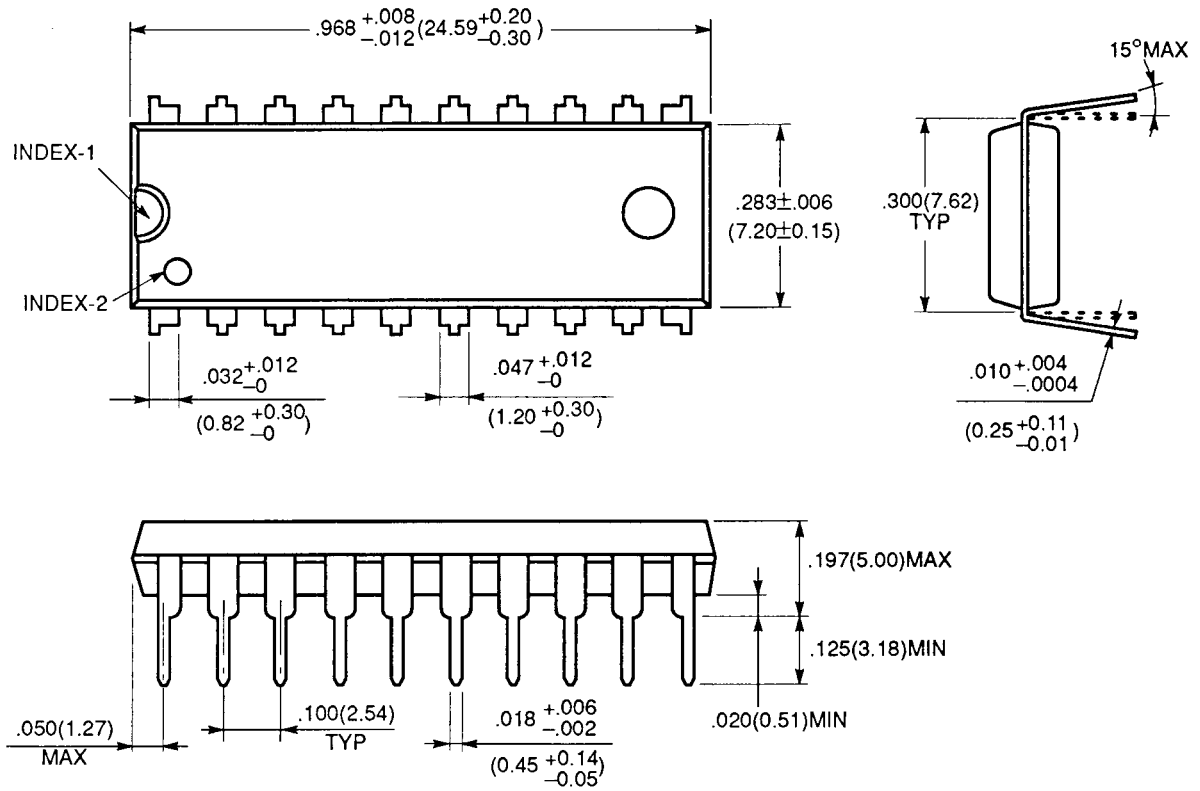
No.	Parameter	Symbol	MB81C4266A-60		MB81C4266A-70		MB81C4266A-80		MB81C4266A-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	t_{FCAC}	—	40	—	45	—	50	—	60	ns
91	$\overline{\text{CAS}}$ Precharge Time	t_{CPT}	20	—	20	—	20	—	20	—	ns

Note . Assumes that $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle only.

PACKAGE DIMENSIONS

(Suffix : -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
 (CASE No.: DIP-20P-M03)

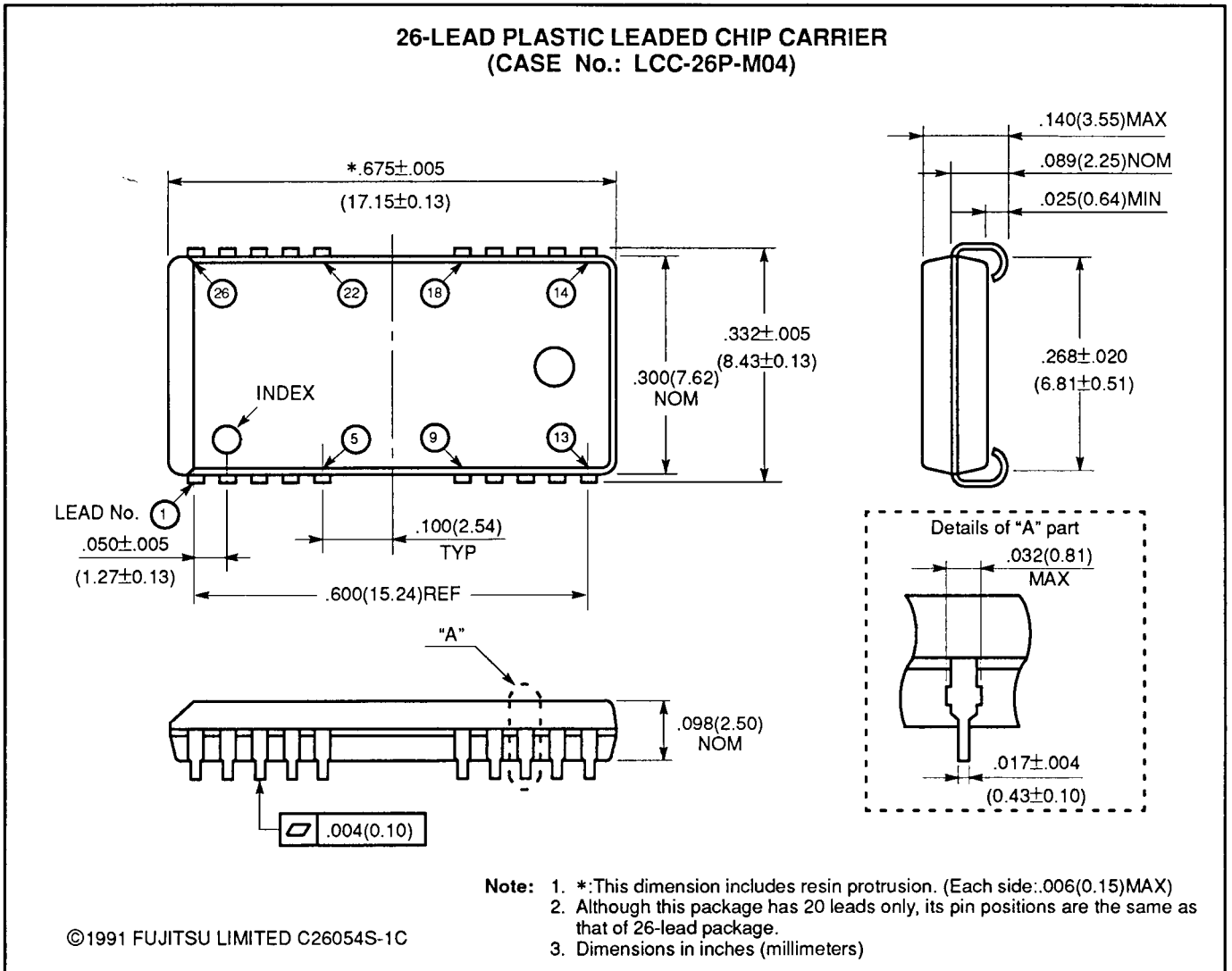


Dimensions in
 inches (millimeters)

MB81C4266A-60
 MB81C4266A-70
 MB81C4266A-80
 MB81C4266A-10

PACKAGE DIMENSIONS (Continued)

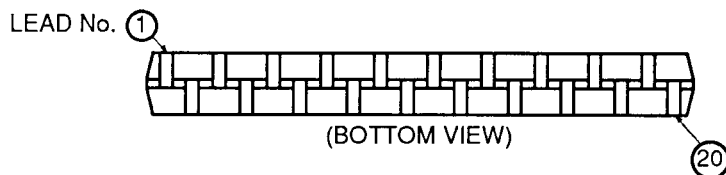
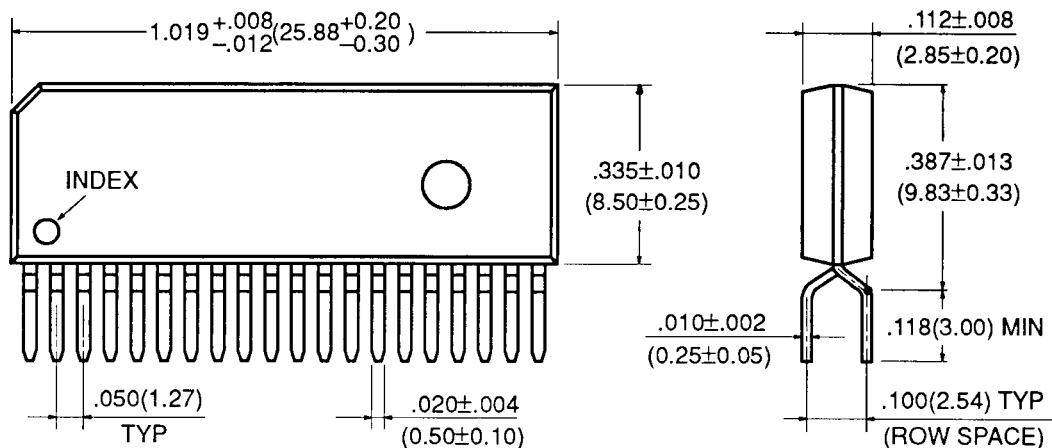
(Suffix : -PJ)



PACKAGE DIMENSIONS (Continued)

(Suffix : -PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE (CASE No.: ZIP-20P-M02)

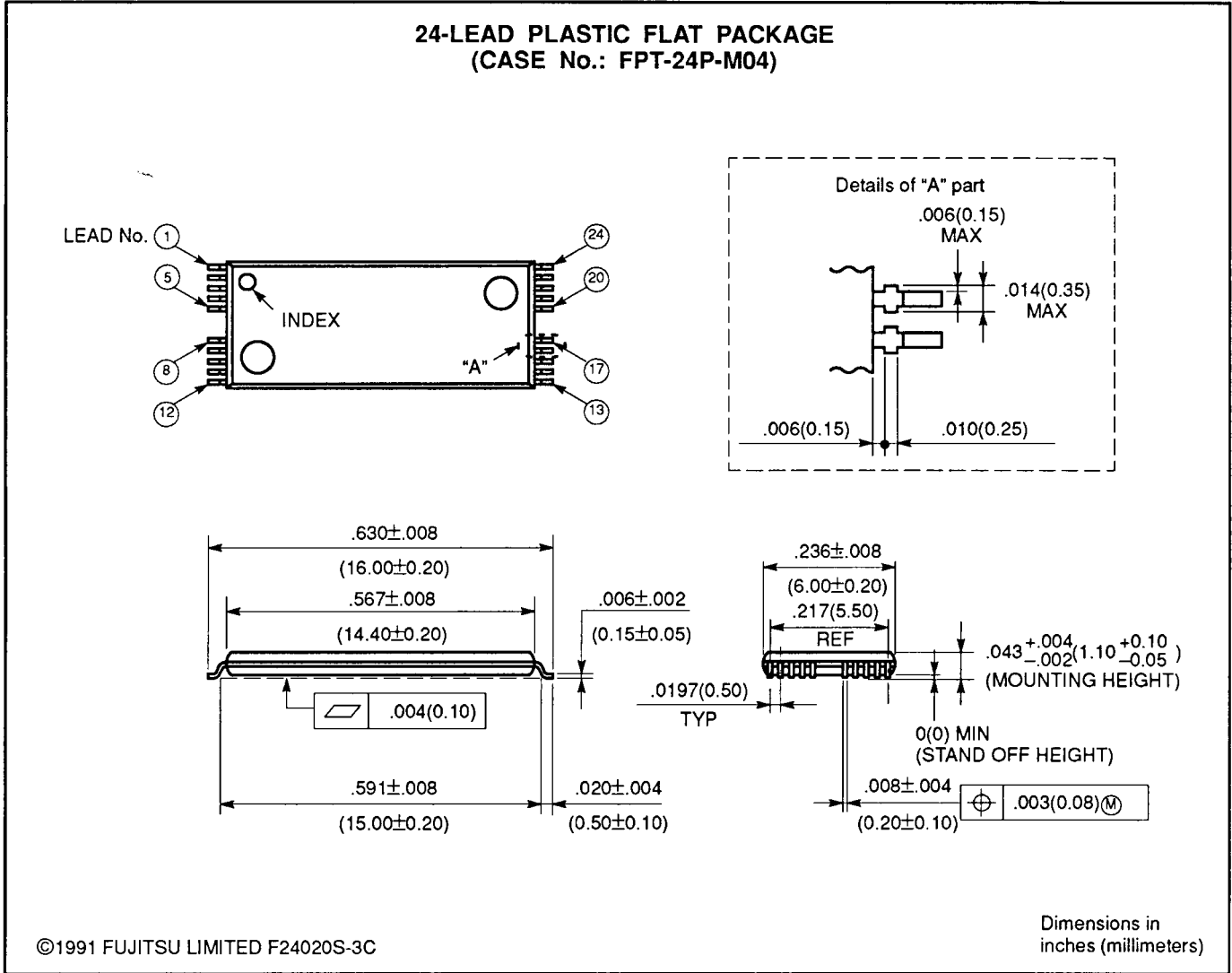


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Dimensions in
 inches (millimeters)

PACKAGE DIMENSIONS (Continued)

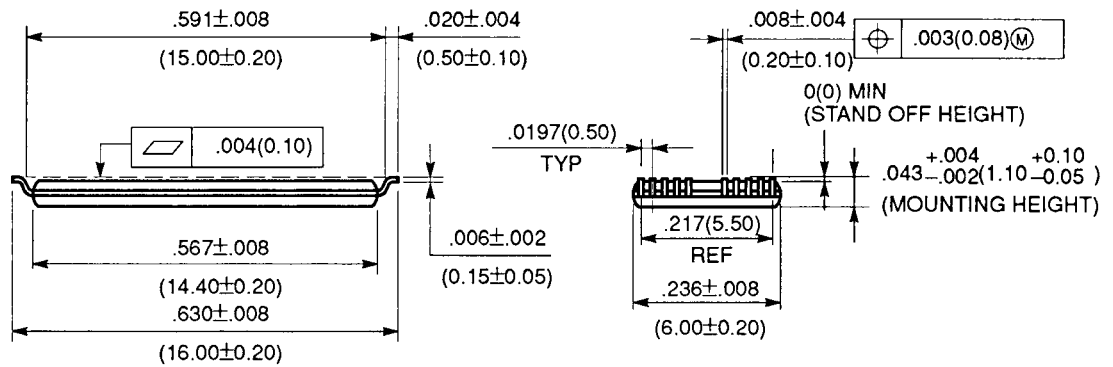
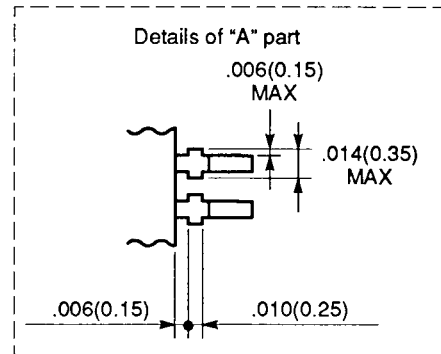
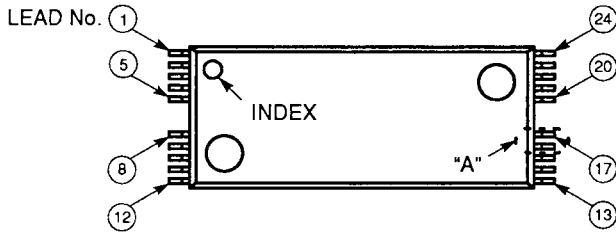
(Suffix: - PFTN)



PACKAGE DIMENSIONS (Continued)

(Suffix: - PFTR)

24-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-24P-M05)



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