SKYWORKS™

CX77129

System Smart™ PA Module for CDMA / AMPS (824–849 MHz)

The CX77129 Power Amplifier Module is a dual-mode Code Division Multiple Access (CDMA) / Advanced Mobile Phone Service (AMPS) module designed for mobile units operating in the 824–849 MHz cellular bandwidth. This device meets stringent IS95 CDMA linearity requirements to and beyond 28 dBm output power and can be driven to power output levels beyond 31 dBm for high efficiency FM mode operation. The CX77129 System Smart™ design presents a unique feature that enables exceptionally low average battery current consumption with two control pins that accept digital signals provided by the system's baseband ASIC. This digital control logic defines an RF power range of operation for the PA. The decoding logic within the PA uses this information to optimize efficiency within this power range while meeting the specification for Adjacent Channel Power Ratio (ACPR).

The two control pins (referred to as V_{CONT1} and V_{CONT2}) allow the PA to be switched into one of four states.

- State/Power-range 3—high power mode, linear up to P_{OUT} = 28 dBm, total PA current is typically 560 mA (V_{CONT1} = High, V_{CONT2} = High)
- State/Power-range 2—medium power mode, linear up to P_{OUT} = 13 dBm, total PA current is typically 130 mA (V_{CONT1} = Low, V_{CONT2} = High)
- State/Power-range 1—low power mode, linear up to P_{OUT} = –5 dBm, total PA current is typically 46 mA (V_{CONT1} = Low, V_{CONT2} = Low)
- State/Power-range 0—power-down mode, leakage current less than 5 µA (V_{CONT1} = Low, V_{CONT2} = Low, V_{REF} = 0.0 V)

The current in States 1 and 2 is much lower than that achieved in a conventional Power Amplifier.

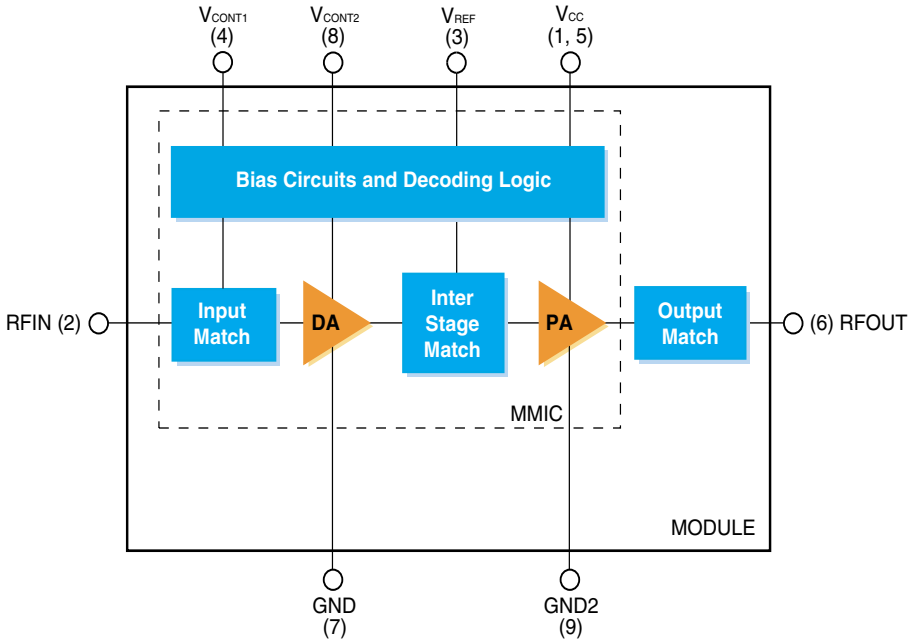
Distinguishing Features

- System Smart™ design
- Three switchable power states
- Dual digital input for setting power states
- Power down control
- Higher efficiency over large dynamic range
- 8-pin LCC package (6 x 6 x 1.5 mm)

Applications

- Digital cellular (CDMA)
- Analog cellular (AMPS)
- Wireless Local Loop (WLL)

Functional Block Diagram



Electrical Specifications

The following tables list the electrical characteristics of the CX77129 System Smart™ Power Amplifier. Table 1 lists the absolute maximum ratings while Table 2 shows the recommended operating conditions to achieve the performance characteristics listed in Table 4. Table 3 presents a truth table for the power ranges.

Table 1. Absolute Maximum Ratings(1)

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Input Power PR3 (High Power) PR2 (Medium Power) PR1 (Low Power)	 P_{IN} P_{IN} P_{IN}	 — — —	 — — —	 6.0 –5.0 –10.0	 dBm dBm dBm
Supply Voltage	V_{CC}	—	3.4	6.0	Volts
Reference Voltage	V_{REF}	—	3.0	—	Volts
Case Operating Temperature	T_C	–30	25	+110	°C
Storage Temperature	T_{TSTG}	–55	—	+125	°C

NOTE(S):
(1) No damage assumes only one parameter set at limit at a time with all other parameters set at or below nominal value.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage	V_{CC}	3.2	3.4	4.2	Volts
Reference Voltage	V_{REF}	2.95	3.0	3.05	Volts
Operating Frequency	F_O	824.0	836.5	849.0	MHz
Operating Temperature	T_O	–30	+25	+85	°C
Control Voltage (HIGH)	V_{CONT1}, V_{CONT2}	2.0	—	4.2	Volts
Control Voltage (LOW)	V_{CONT1}, V_{CONT2}	0.0	—	0.2	Volts

Table 3. Power Range Truth Table

Power Mode	V_{REF}	V_{CONT1}(1)	V_{CONT2}(1)	Range
PR3 (High Power)	3.0 V	HIGH	HIGH	13 dBm ~ 28 dBm
PR2 (Medium Power)	3.0 V	LOW	HIGH	–5 dBm ~ 13 dBm
PR1 (Low Power)	3.0 V	LOW	LOW	≤ –5 dBm
Shut Down	0.0 V	LOW	LOW	—

NOTE(S):
(1) High (2.0 V ~ 3.0 V) Low (0.0 V ~ 0.2 V).
2. To change between High Power and Medium Power mode, switch $V_{CONT}1$ and $V_{CONT}2$ accordingly. Please reverse this procedure to power-down the module.

Table 4. Electrical Specifications for CDMA/AMPS Nominal Conditions[1]

Characteristic	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output Power						
Range 3	P_O3	PR3 selected	—	—	28.0	dBm
Range 2	P_O2	PR2 selected	—	—	13.0	dBm
Range 1	P_O1	PR1 selected	—	—	–5.0	dBm
Quiescent current	Iq1	PR1 selected	—	30.0	45.0	mA
Gain—Digital						
PR3 selected	G_P3	P_O = 28.0 dBm	28.7	31.0	33.5	dB
PR2 selected	G_P2	P_O = 13.0 dBm	24.0	28.0	30.0	dB
PR1 selected	G_P1	P_O = –5.0 dBm	17.0	20.0	22.5	dB
Gain—Analog	Gp	P_O = 31.0 dBm	29.0	31.0	33.5	dB
Total Supply Current						
PR3 selected	$I_{CC}3$	P_O = 28.0 dBm	—	560.0	620	mA
PR2 selected	$I_{CC}2$	P_O = 13.0 dBm	—	133.0	150	mA
PR1 selected	$I_{CC}1$	P_O = –5.0 dBm	—	46.0	55	mA
Total Supply Current in Power Down mode	I_{PD}	—	—	3.0	5.0	µA
Power-Added Efficiency Digital						
PR3 selected	PAE3	P_O3 = 28.0 dBm	31.0	33.0	—	%
PR2 selected	PAE2	P_O2 = 13.0 dBm	3.0	4.5	—	%
Power Added Efficiency Analog	PAEa	P_O = 31.0 dBm	40.0	45.0	—	%
Adjacent Channel Power[2]		Any PR selected, up to each range maximum output power				
885 kHz offset	ACP		—	–49.0	–47.0[3]	dBc
1980 kHz offset	ACP		—	–61.5	–58.5	dBc
Harmonic Suppression		Any PR selected, up to each range maximum output power				
Second	$2F_O$		—	—	–37.5	dBc
Third	$3F_O$		—	—	–39.0	dBc
Noise Power in RX Band	RxBN	Any PR selected, up to each range maximum output power, 45 MHz above Tx frequency	—	–133.0	–132.0	dBm/Hz
Noise Figure	NF	—	—	6.5	—	dB
Input Voltage Standing Wave Ratio						
PR3 selected	VSWR3	P_O = 28.0 dBm	—	1.5:1	1.8:1	—
PR2 selected	VSWR2	P_O = 13.0 dBm	—	1.6:1	1.9:1	—
PR1 selected	VSWR1	P_O = –5.0 dBm	—	1.6:1	1.9:1	—
Stability (spurious output)	—	5:1 VSWR all phases, and any PR selected	—	—	–60.0	dBc

Table 4. Electrical Specifications for CDMA/AMPS Nominal Conditions(1)

Characteristic	Symbol	Condition	Minimum	Typical	Maximum	Unit
Switching speed between states	τ-PR	From any PR to any other PR	—	—	5.0	µsec
Ruggedness–No damage	Ru	$P_O \leq 28$ dBm	10:1	—	—	VSWR

NOTE(S):

(1) V_{CC} = 3.4 V, V_{REF} = 3.0 V, Freq. = 836.5 MHz, T_C = 25 °C

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW

(3) ACPR maximum for low power mode (PR1 selected) = 45.6 dBc.

Table 5. Electrical Specifications for CDMA/AMPS Recommended Operating Conditions(1)

Characteristic	Symbol	Condition	Minimum	Maximum	Unit
Gain—Digital					
PR3 selected	G_P3	P_O = 28.0 dBm	26.0	34.8	dB
PR2 selected	G_P2	P_O = 13.0 dBm	23.5	31.8	dB
PR1 selected	G_P1	P_O = –5.0 dBm	16.8	24.8	dB
Gain—Analog	Gp	P_O = 31.0 dBm	26.0	35.8	dB
Power-Added Efficiency Digital					
PR3 selected					
PR2 selected	PAE3	P_O3 = 28.0 dBm	30.0	—	%
	PAE2	P_O2 = 13.0 dBm	2.4	—	%
Power Added Efficiency Analog	PAEa	P_O = 31.0 dBm	39.0	—	%
Adjacent Channel Power(2)		Any PR selected, up to each range maximum output power			
885 kHz offset					
1980 kHz offset	ACP		—	–44.0	dBc
	ACP		—	–57.0	dBc
Harmonic Suppression		Any PR selected, up to each range maximum output power			
Second	$2F_O$		—	–35.0	dBc
Third	$3F_O$		—	–35.0	dBc
Input Voltage Standing Wave Ratio					
PR3 selected					
PR2 selected	VSWR3	P_O = 28.0 dBm	—	2.0:1	—
PR1 selected	VSWR2	P_O = 13.0 dBm	—	2.0:1	—
	VSWR1	P_O = –5.0 dBm	—	2.0:1	—
Switching speed between states	τ-PR	From any PR to any other PR	—	5.0	µsec

NOTE(S):
(1) Maximum overall conditions listed in Table 2.
(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW

Characterization Data

The following graphs illustrate the characteristics of a typical CX77129 System Smart™ Power Amplifier under nominal operating conditions (V_{CC} = 3.4 V, V_{REF} = 3.0 V, room temperature) tested in an evaluation board described in the following section.

Figure 1. Total Battery Current vs. Output Power (Digital Mode)

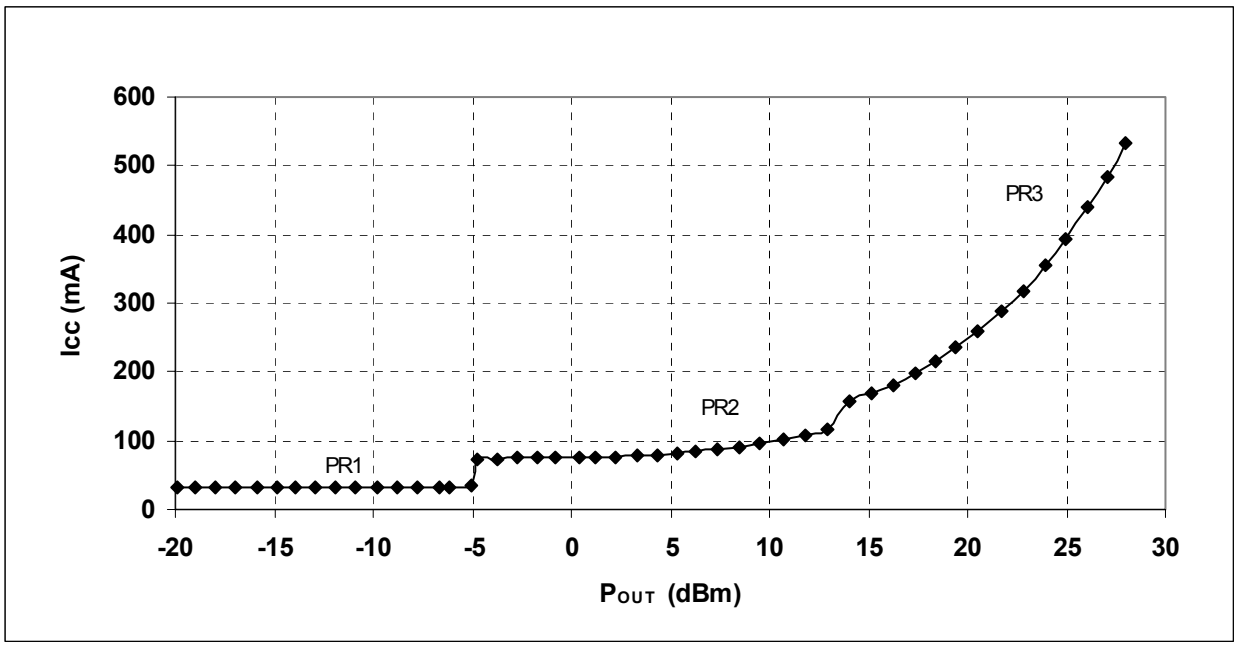


Figure 2. Total Battery Current in Low to Medium Power Range (Digital Mode)

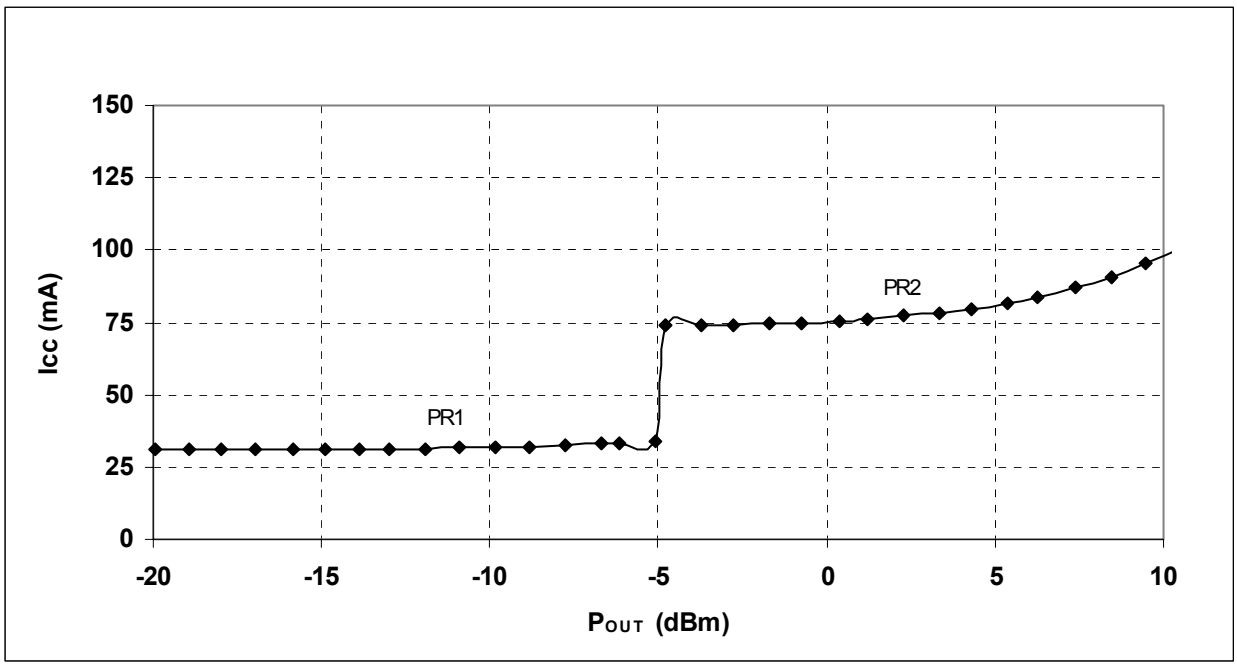


Figure 3. Gain vs. Output Power (Digital Mode)

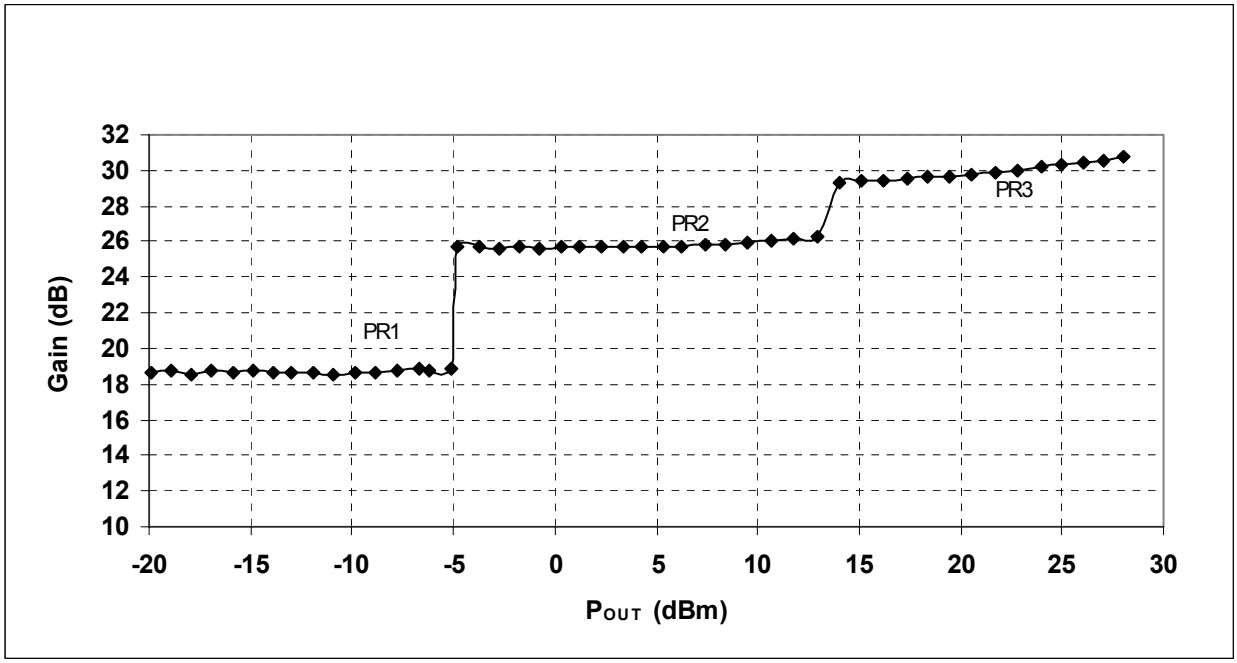


Figure 4. Power Added Efficiency vs. Output Power (Digital Mode)

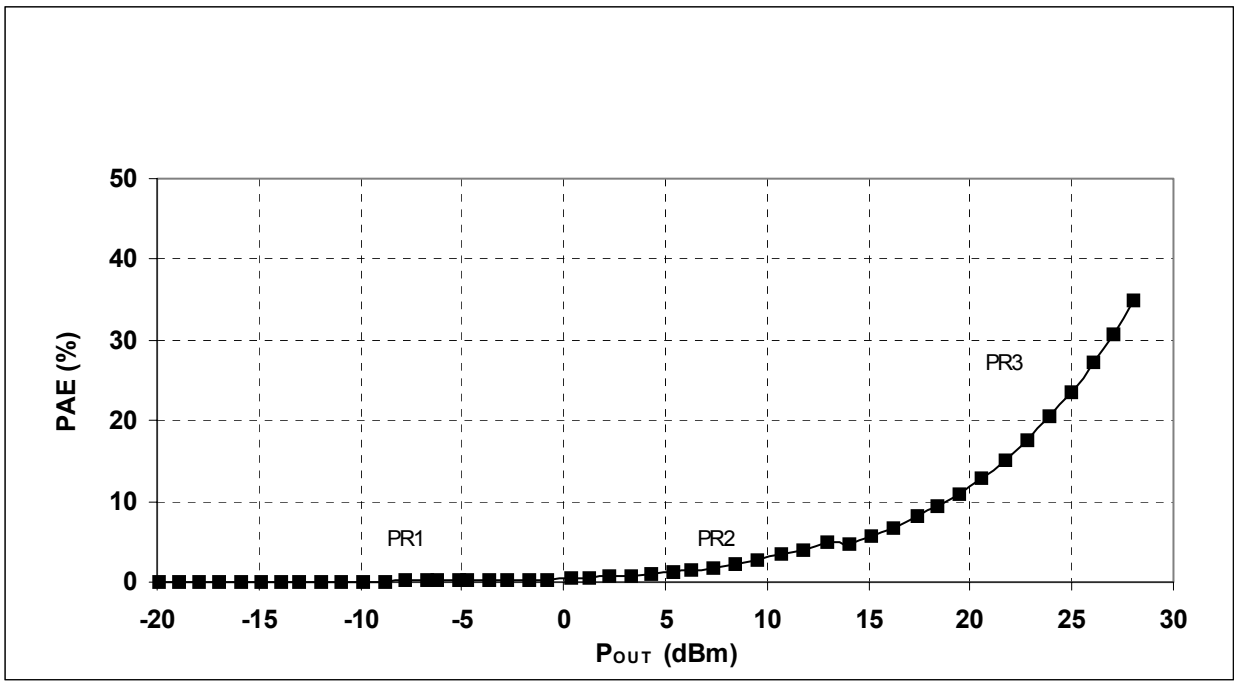


Figure 5. Adjacent Channel Power vs. Output Power (Digital Mode)

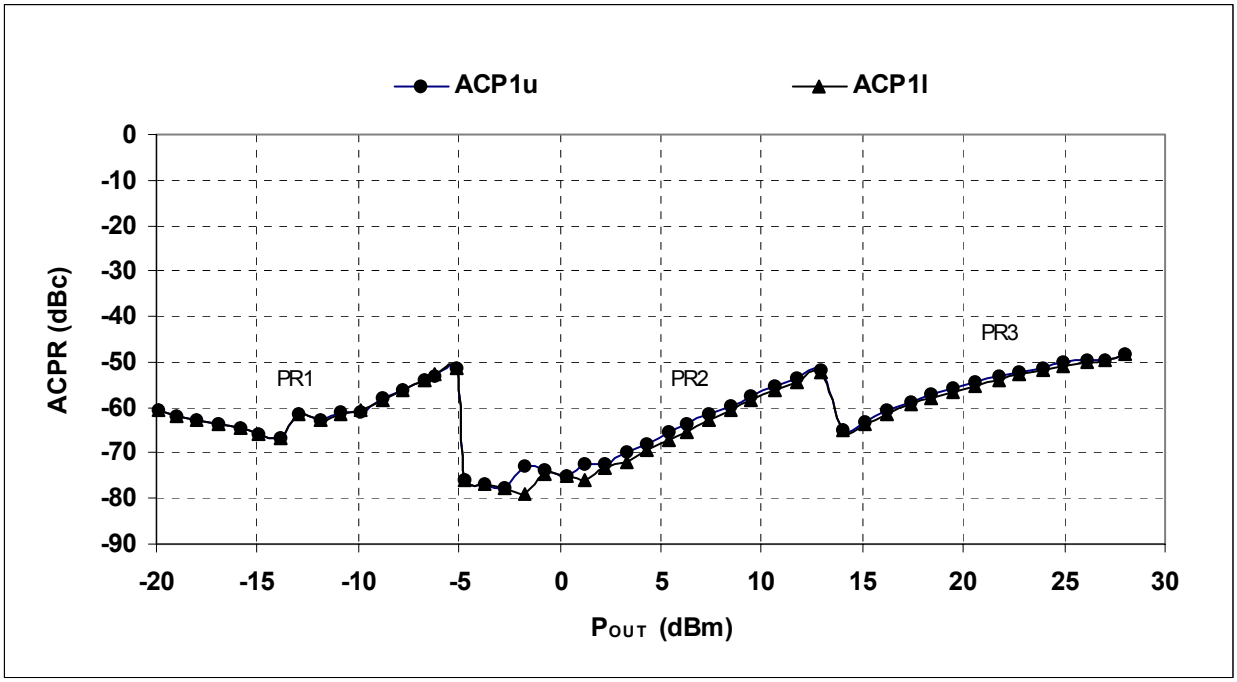


Figure 6. Harmonic Suppression vs. Output Power (Digital Mode)

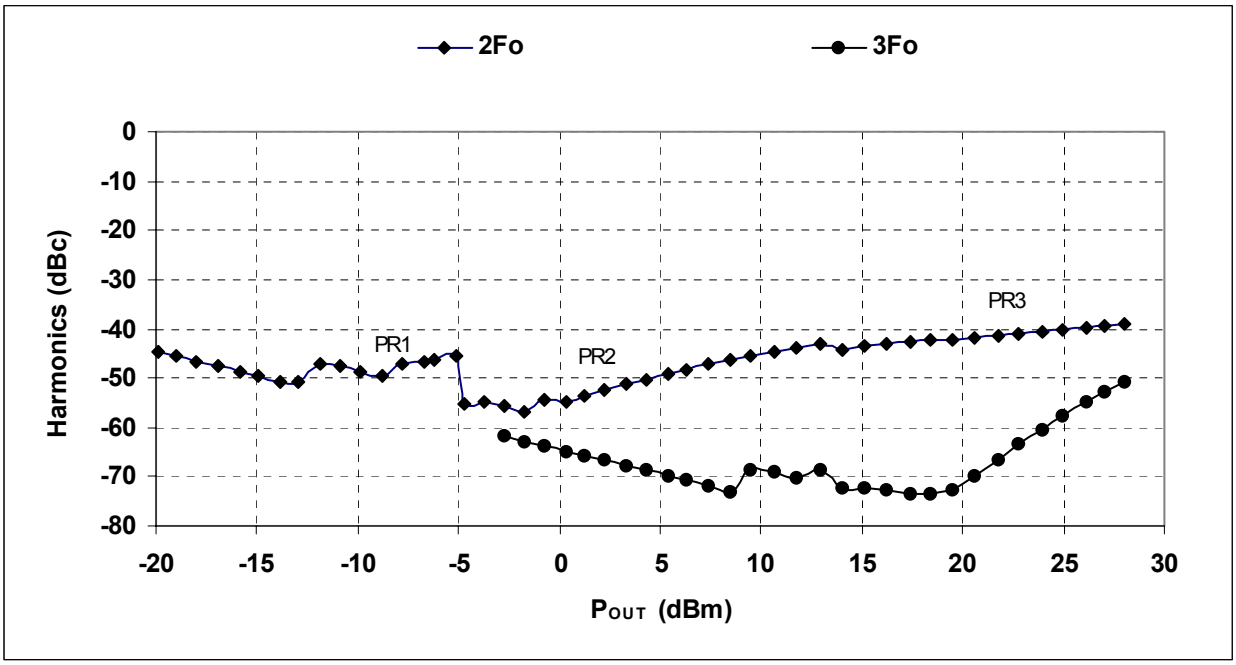


Figure 7. Gain vs. Output Power (Analog Mode)

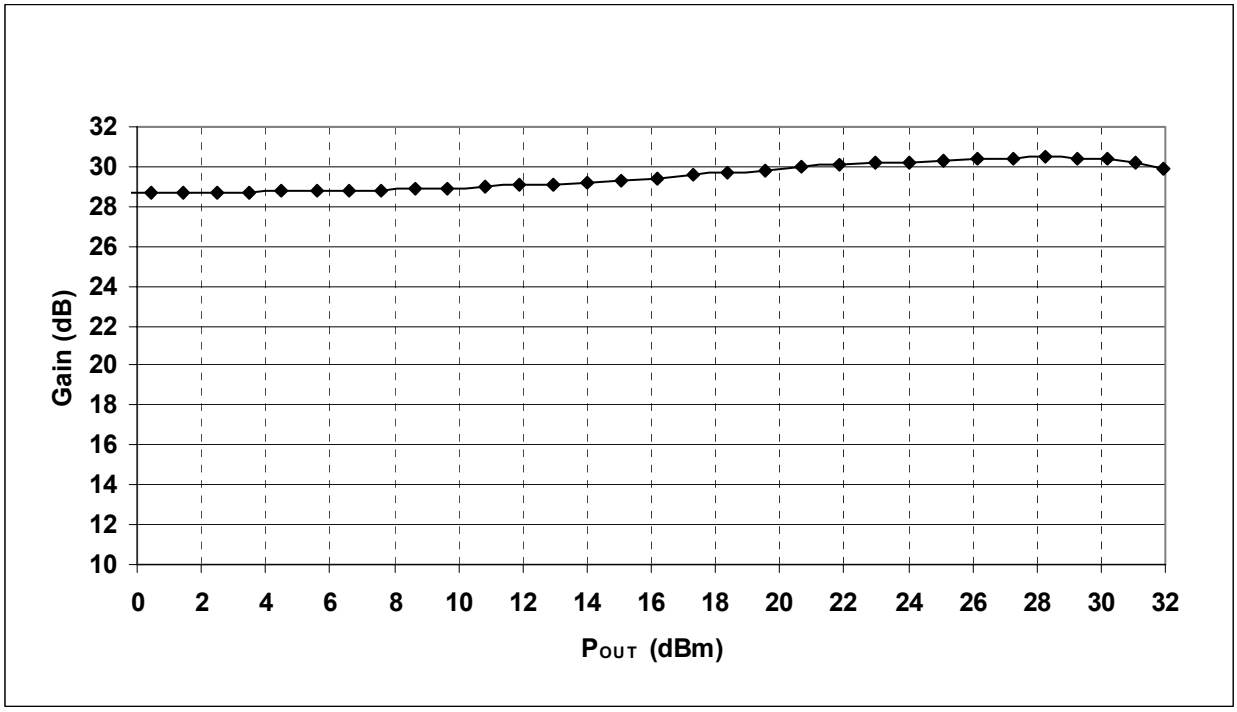


Figure 8. Power Added Efficiency vs. Output Power (Analog Mode)

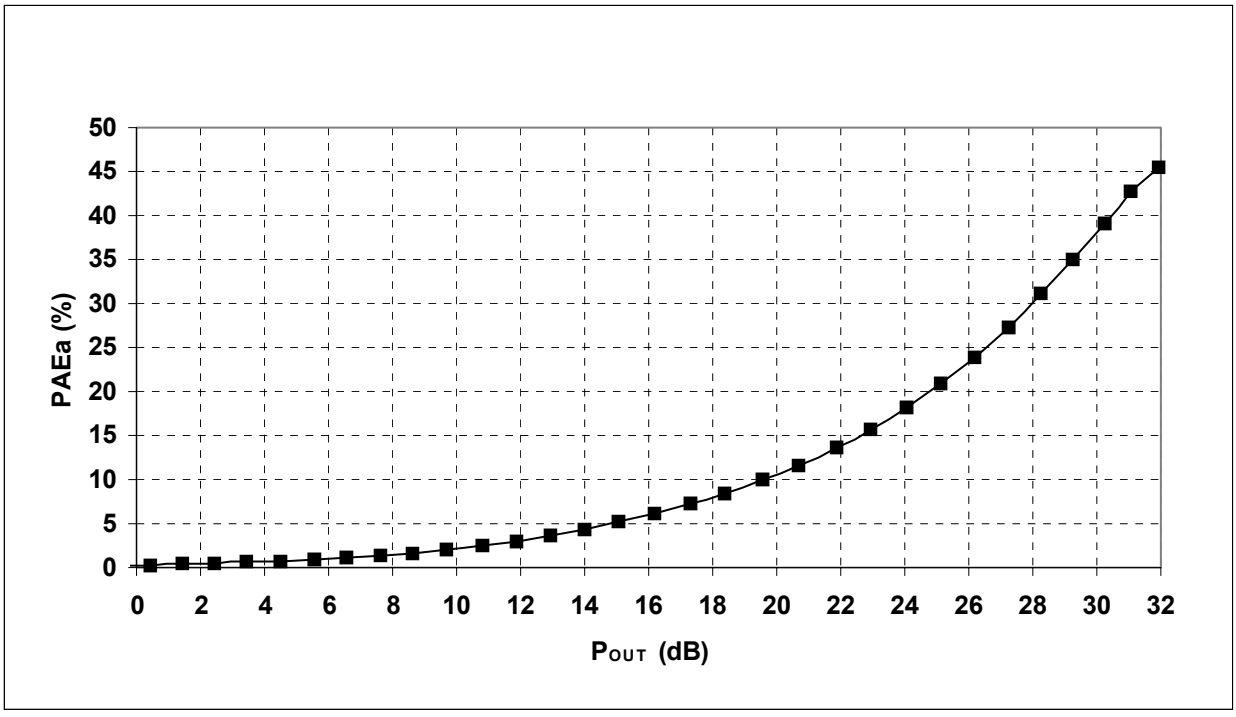
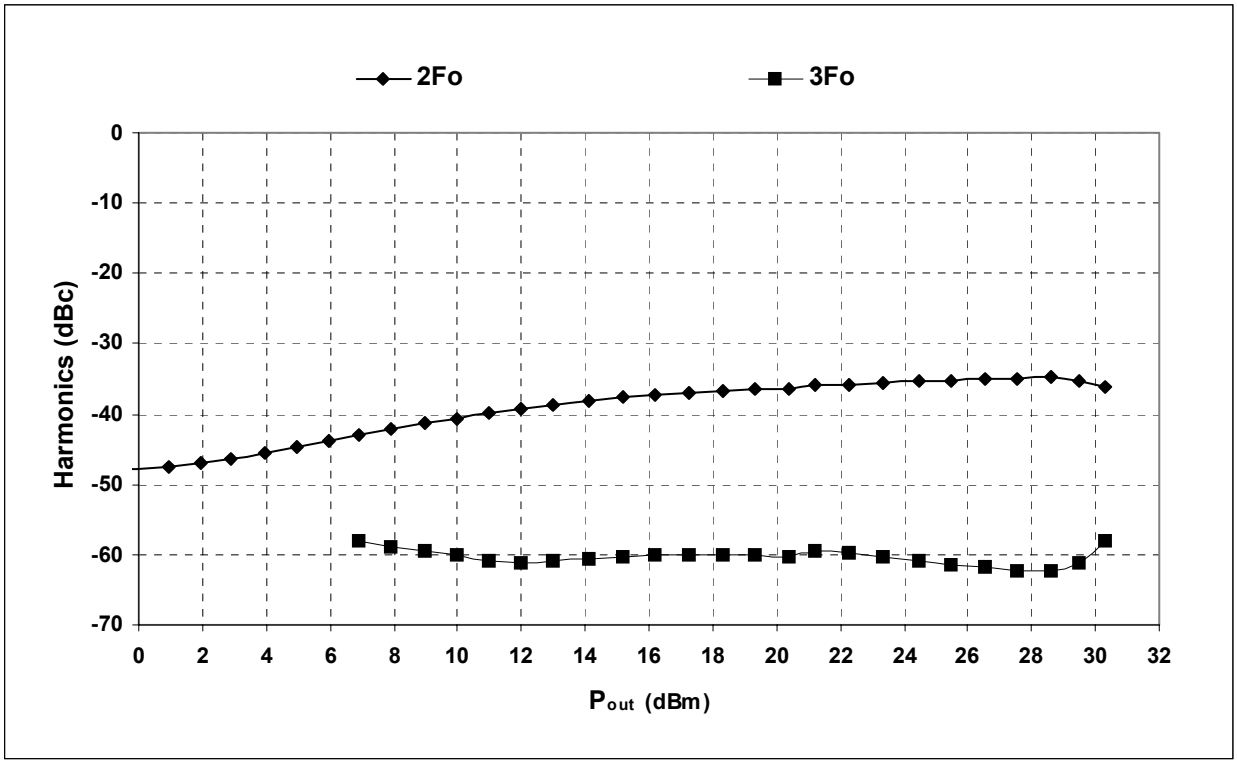


Figure 9. Harmonic Suppression vs. Output Power



Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77129, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 10 shows the basic schematic of the board for the 824 MHz to 849 MHz range. Figure 11 illustrates the board layout.

Figure 10. Evaluation Board Schematic

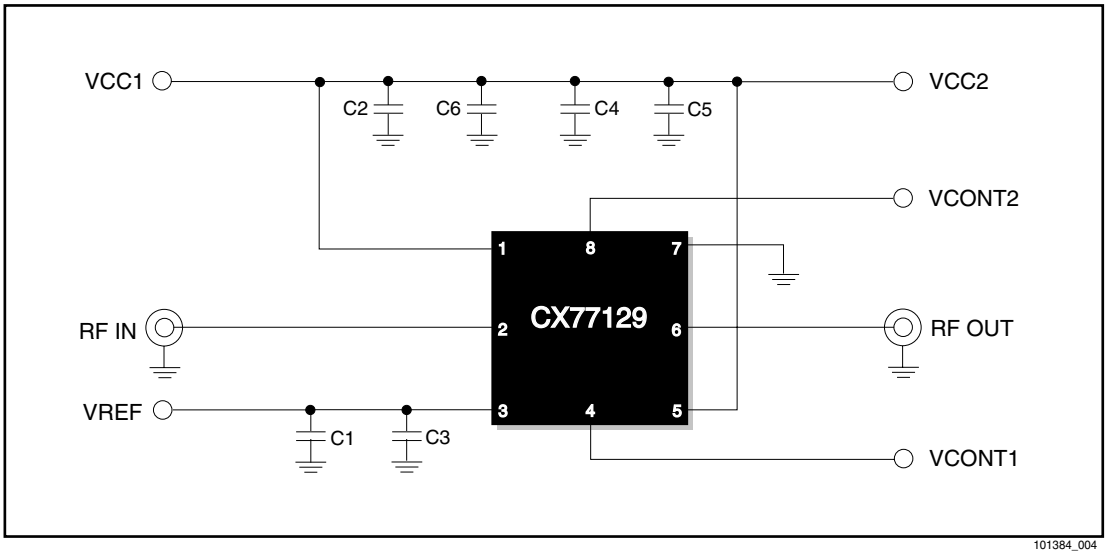
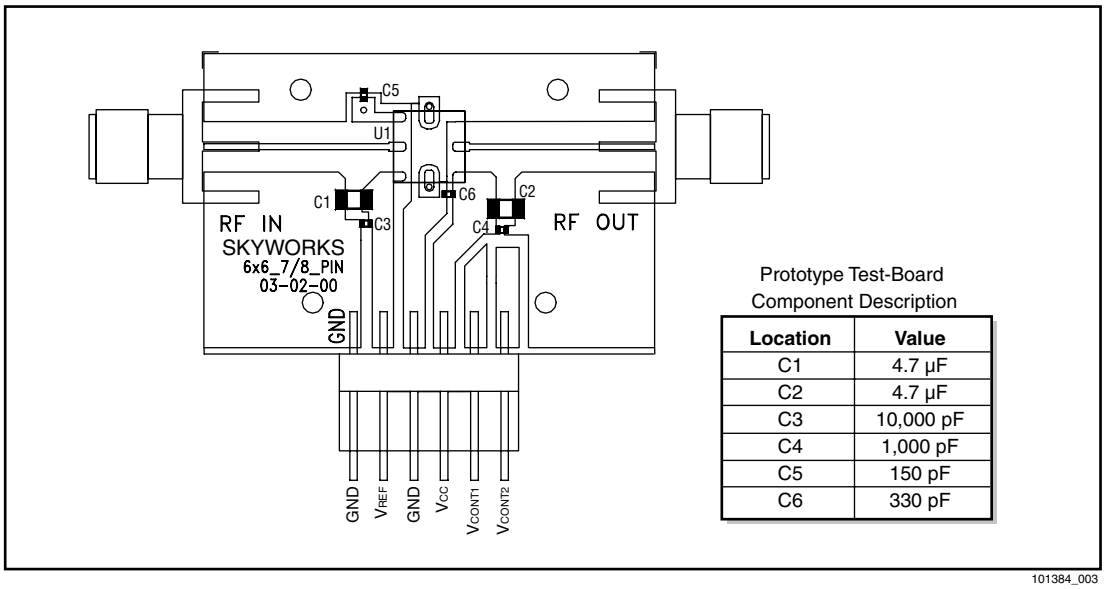


Figure 11. Evaluation Board Assembly Diagram



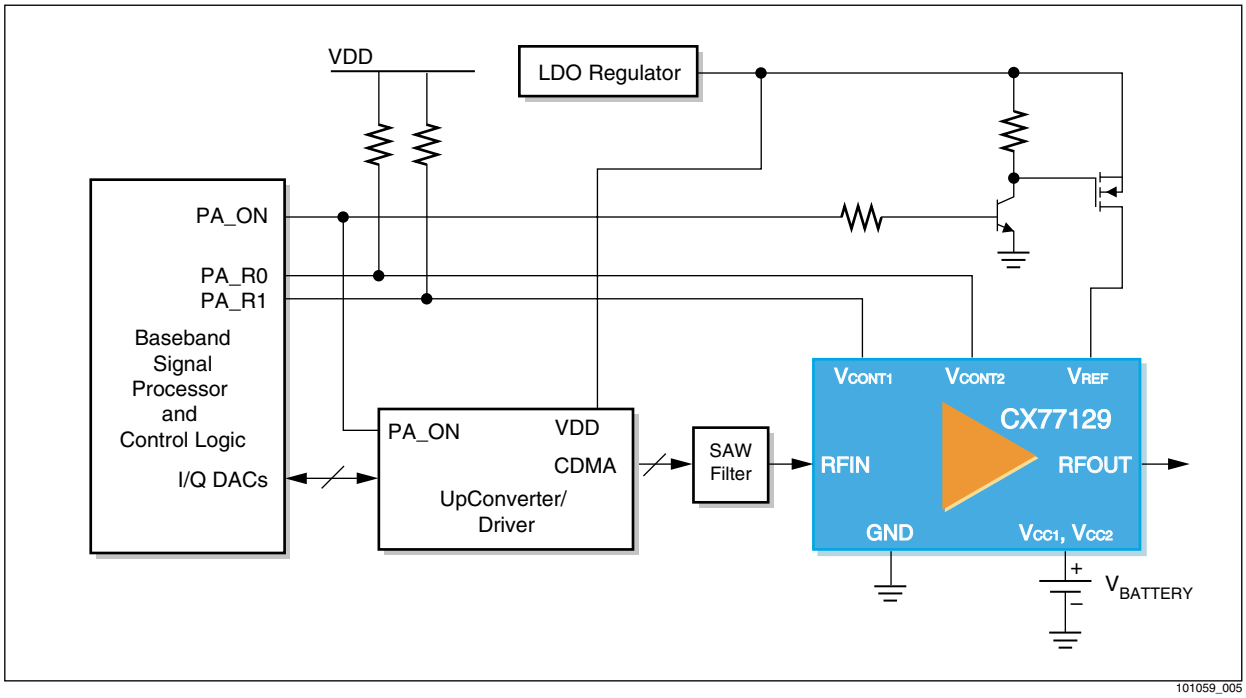
Prototype Test-Board
Component Description

Location	Value
C1	4.7 µF
C2	4.7 µF
C3	10,000 pF
C4	1,000 pF
C5	150 pF
C6	330 pF

Typical System Design Implementation

Figure 12 shows the CX77129 interface to baseband logic and transmit chain in a typical handset. Since CX77129 uses two CMOS logic level power control pins, two pull-up resistors are required. Another CMOS logic pin (PA_ON) can be used to enable / disable the CX77129. A NPN bipolar transistor and P-Channel P-FET are used to supply VREF to the CX77129. In order to provide a consistent voltage with adequate current from the Low Drop-Out voltage regulator, a low on-resistance P-FET is required.

Figure 12. Interconnect Schematic



The following steps are used to power up the CX77129 module.

1. Connect Vcc to a 3.4 V DC power supply, then turn on the supply.
2. Connect Vref to a 3.0 V DC power supply, then turn on the supply.
3. For High Power mode (up to 28dBm), apply HIGH to VCONT1 and VCONT2.
4. For Medium Power, Low Power, and Shutdown modes, refer to Table 3.
5. Apply RF signal.

Package Dimensions & Pin Descriptions

Figure 13 shows the bottom view of the CX77129 package outline with the solder pads clearly visible. Table 6 lists the CX77129 signal descriptions.

Figure 13. CX77129 Package Drawing

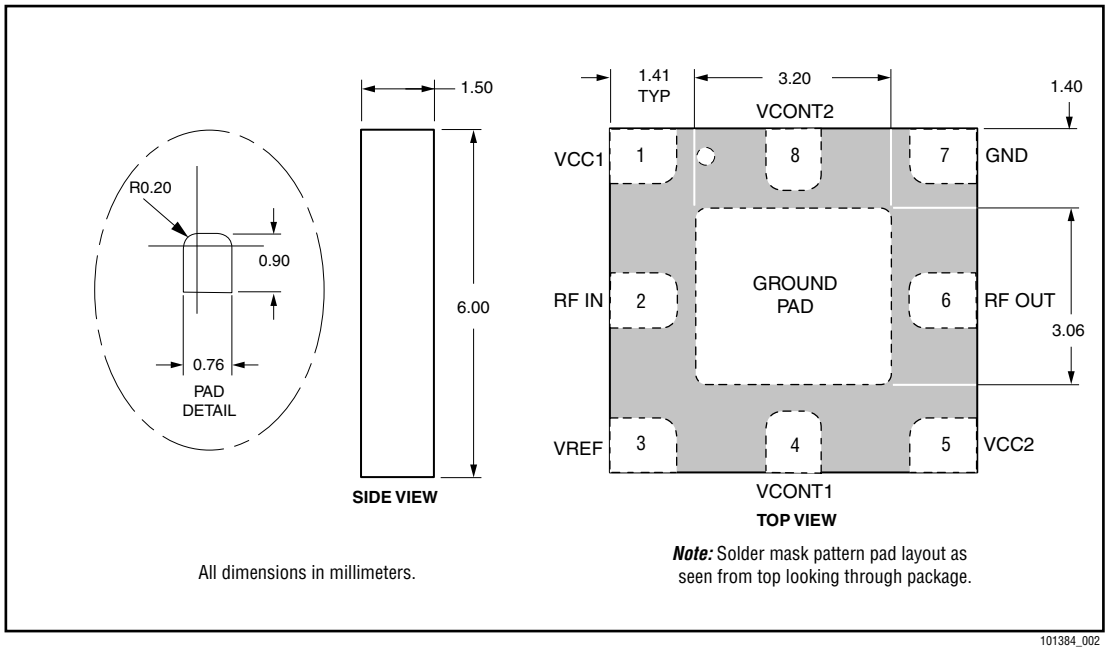


Table 6. Signal Description

Pin	Name	Description
1	VCC1	Supply for High-Power Amplifier. Must be decoupled close to package
2	RF IN	50 Ω RF Input—DC decoupled internally inside module
3	VREF	Power Range logic (Analog voltage, NOT CMOS COMPATIBLE). See Table 3 for logic states
4	VCONT1	Power Range logic (Digital Voltage, CMOS COMPATIBLE). See Table 3 for logic states
5	VCC2	Supply for High-Power Amplifier. Must be decoupled close to package
6	RF OUT	50 Ω RF Output—DC decoupled internally inside module
7	GND	GND for Logic Circuits
8	VCONT2	Power Range logic (Digital Voltage, CMOS COMPATIBLE). See Table 3 for logic states
9 (Pkg Base)	GND2	Backside of package must be solder-connected directly to a ground plane by multiple VIA's

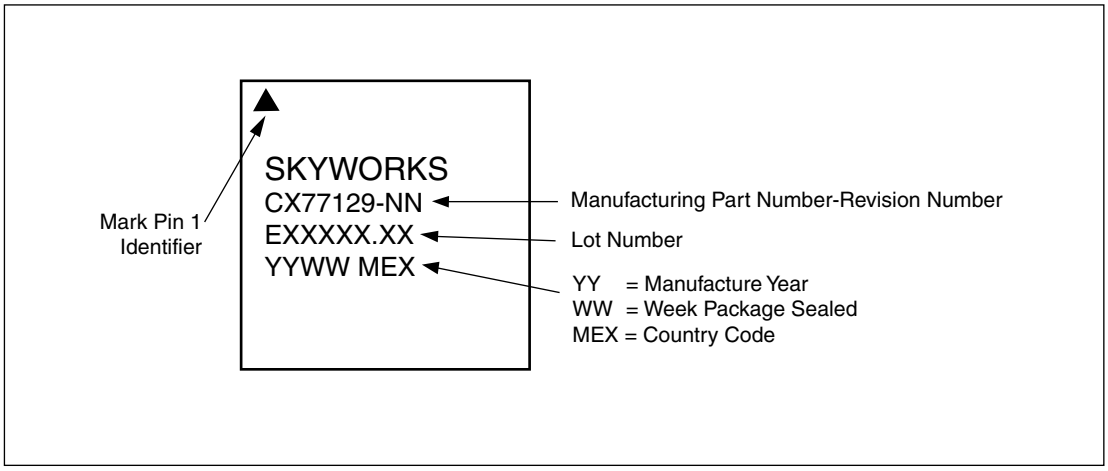
Packaging and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77129 is capable of withstanding an MSL 3/235 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 235 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 235 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020A*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

Figure 1. Typical Case Markings



Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77129	CX77129–12R	12	—	—

Revision History

Revision	Level	Date	Description
A	—	May 15, 2002	Initial Release
B	—	September 5, 2002	Revise: Functional Block Diagram, Table 6,Package and Handling Information, Manufacturing Part Number,

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.
Application Note: Tape and Reel, Document Number 101568
Standard SMT Reflow Profiles: JEDEC Standard J–STD–020A.

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