HD66224T

(Dot Matrix Liquid Crystal Graphic Display Column Driver with 80-Channel Outputs)

HITACHI

Description

The HD66224T is a column driver for dot matrix liquid crystal graphic display system. It has 80 liquid crystal drive circuits and can drive large LCDs. The column driver latches parallel data for display (4/8 bit parallel) from the controller, then generates a drive signal and selects the proper LCD drive voltage. A built-in standby function that allows all internal drivers except one to be placed in standby mode (IST) lowers device power consumption. The column driver package is a 7.5-mm wide ultra-small tape carrier package (TCP), allowing designs using half the frame area of conventional displays.

The column driver can be used in a wide range of battery-powered designs because its logic power supply can operate with an input voltage ranging from 2.5 to 5.5 V.

Features

- Display duty cycle: 1/64 to 1/240
- Number of liquid crystal drive circuits: 80
- Parallel data transfer: 4/8 bits
- High voltage: Drive voltage 10–28 V (absolute maximum rating 30 V)
- High-speed operation: Maximum clock speed 8 MHz (for 5 V) or 6.5 MHz (for 2.5 V)
- Logic power supply voltage: 2.5–5.5 V
- Built-in display off function
- Built-in automatic generation function for chip-enable signal
- Built-in standby function
- 107-pin 35 mm TCP

Ordering Information

Type No.	Data Input	Input Format	Outer Lead Pitch (µm)
HD66224TA1	4-bit input	Straight	210
HD66224TA2	4-bit input	Straight	200
HD66224TB0	8-bit input	Straight	200

Note: The details of TCP pattern are shown in “The Information of TCP.”

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Internal Block Diagram

Figure 1 is a block diagram of the HD66224T.

Liquid-Crystal Drive Circuit

The LCD drive circuit selects from four available voltage levels (V_1, V_3, V_4, and V_{EE}) based on the combination of the data of latch circuit 2 and input to pin M. The circuit outputs the selected voltage to the LCDs.

Level Shifter

The level shifter circuit raises the voltage of the logic power-supply voltage to the level used for driving the LCDs.

Latch Circuit 2

The 80-bit latch circuit 2 latches data from latch circuit 1 on the falling edge of clock CL1 and outputs the data to the level shifter circuit.

Latch Circuit 1

Latch circuit 1 consists of 4/8-bit parallel data latches that store input data D_0 to D_7 when signaled by the shift register.

Control Circuit

The control circuit generates signals that fetch the data for input to latch circuit 1.

Data Rearrange Circuit

The data rearrange circuit performs left to right (SHL) inversion on data D_0 to D_7.

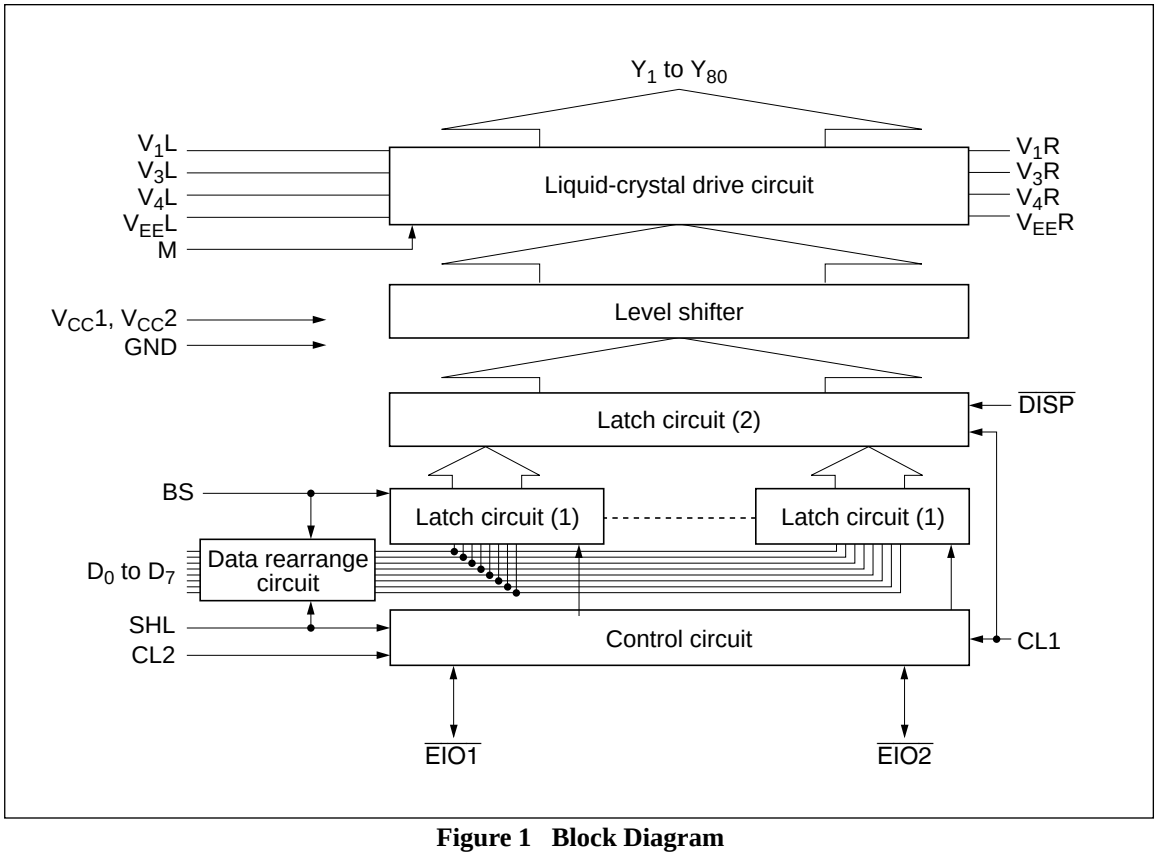
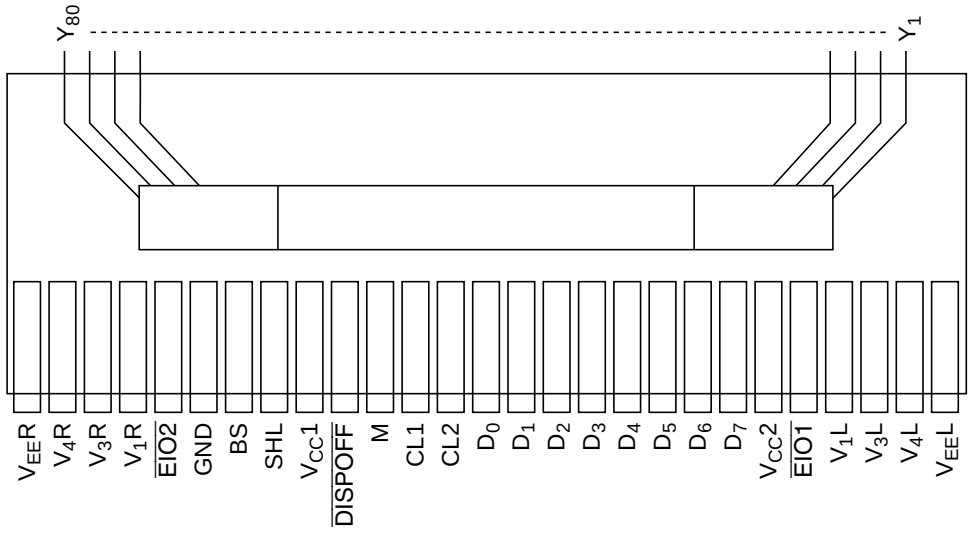


Figure 1 Block Diagram

Pin Arrangement



Note: This illustration does not correspond to the external shape of the TCP package.

Pin Description

Table 1 Pin Description

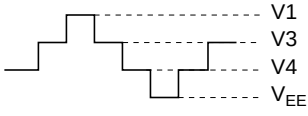
Type	Symbol	Pin Number	Pin Name	I/O	Function
Power supply	$V_{CC}1$	89	$V_{CC}1$	—	V_{CC} – GND: Connect to logic power supply.
	$V_{CC}2$	102	$V_{CC}2$		V_{CC} – V_{EE}: Connect to power supply for liquid-crystal drive circuit.
	GND	86	GND		
	$V_{EE}L$	107	$V_{EE}L$		
	$V_{EE}R$	81	$V_{EE}R$		
	V_1L	104	V_1L	I	Liquid crystal drive level power supply
	V_1R	84	V_1R		
	V_3L	105	V_3L		
	V_3R	83	V_3R		
	V_4L	106	V_4L		V_1, V_{EE}: selected level
	V_4R	82	V_4R		V_3, V_4: nonselected level
					The power supply should maintain the condition Vcc ≥ $V_1 > V_3 > V_4 > V_{EE}$. The L and R sides of V_1,V_3, and V_4 are separated within the device, so the potentials externally supplied to them must be identical.
Control signal	CL1	92	Clock 1	I	Synchronizes the drive signal that latches display data into latch circuit 2.
	CL2	93	Clock 2	I	Synchronizes the drive signal that latches display data into latch circuit 1.
	M	91	M	I	Converts the liquid crystal drive output to AC.
	D_0–D_7	94 to 101	Data 0–7	I	**Display Data** / **LCD Drive Output** / **LCD**: High / Selected level / On; Low / Nonselected level / Off

Table 1 Pin Description (cont)

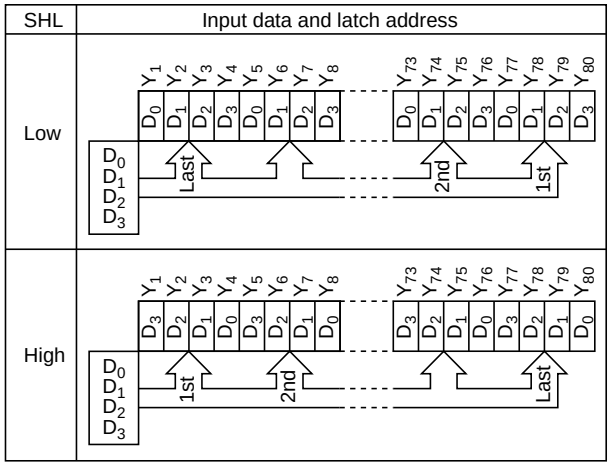
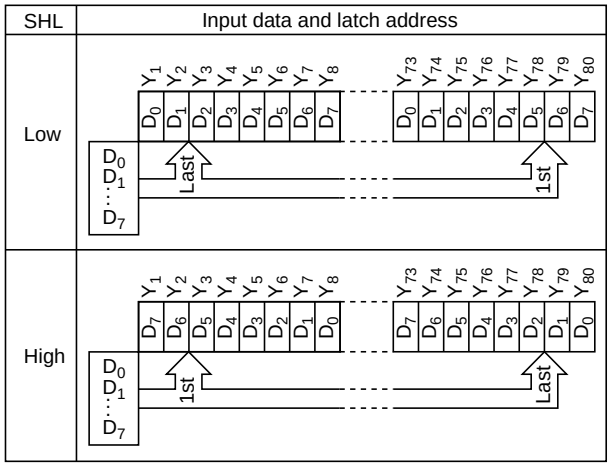
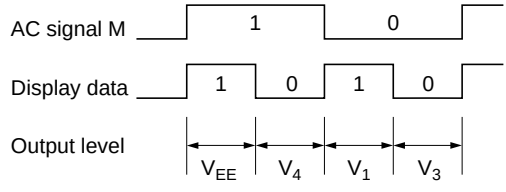
Type	Symbol	Pin Number	Pin Name	I/O	Function
Control signal (cont)	SHL	88	Shift left	I	Inverts the data output destination. 4-bit input mode:  8-bit input mode: 

Table 1 Pin Description (cont)

Type	Symbol	Pin Number	Pin Name	I/O	Function
Control signal (cont)	$\overline{\text{DISPOFF}}$	90	Display off	I	When the liquid crystal output nonselected level control input pin drives $\overline{\text{DISPOFF}}$ low, the liquid crystal drive output (Y_1 to Y_{80}) is set to the V1 level.
	$\overline{\text{EIO1}}$	103	Enable I/O 1	I/O	I/O pins for chip selection. Input/output is controlled by SHL input.
	$\overline{\text{EIO2}}$	85	Enable I/O 2		**SHL** / **Enable I/O 1** / **Enable I/O 2**: 0 — Output — Input; 1 — Input — Output. When the enable input signal goes low, data fetch begins. When all data has been fetched, the enable output changes from high to low and the next stage IC starts up.
	BS	87	Bus select	I	Switches the number of input bits for the display data. When high, places the device in 8-bit input mode; when low, changes the device to the 4-bit input mode.
Liquid crystal drive output	Y_1 to Y_{80}	1 to 80	Y_1 to Y_{80}	O	Outputs one of the four voltage levels V_1, V_3, V_4, or V_{EE}, based on the combination of the M signal and the display data.



Note: 0 and low levels indicate ground level. 1 and high levels indicate V_{CC} level.

Sample Application

Figure 2 shows an example of an LCD panel comprised of 640 × 200 dots, using the HD66224T. The recommended common driver is HD66215. For 640 × 400 dots, extend the configuration shown to configure two screens.

R1 and R2 differ depending on the LCD panel used. For a 1/15 bias, for example, R1 = 3 kΩ and R2 = 33 kΩ are used so that R1 (4R1 + R2) = 1/15.

When designing a board locate bypass capacitors as close to each device as possible, to stabilize the power supply. We recommend that two capacitors (of about 0.1 pF) be used with each HD66224T. One capacitor should be connected between V_{CC} and GND, and one between V_{CC} and V_{EE}.

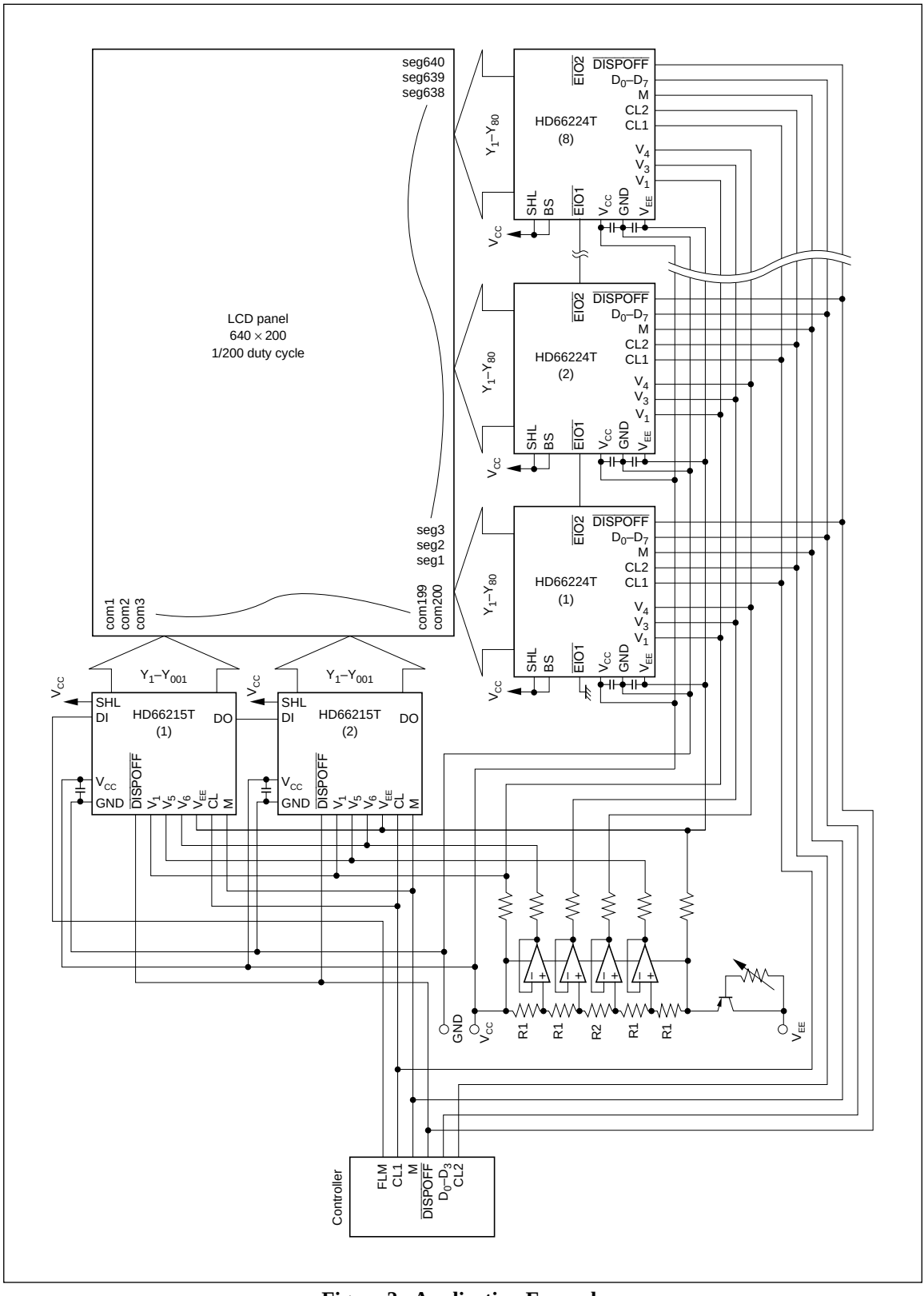


Figure 2 Application Example

Absolute Maximum Ratings

Parameters		Symbol	Rating	Unit	Notes
Power supply voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	Liquid crystal drive circuit	V_{EE}	V_{CC} – 30.0 to V_{CC} + 0.3		
Input voltage (1)		V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)		V_{T2}	V_{EE} – 0.3 to V_{CC} + 0.3	V	1, 3
Operating temperature		T_{opr}	–20 to + 75	°C	
Storage temperature		T_{stg}	–40 to +125	°C	

Notes: 1. Indicates the potential from GND.

2. Applies to the CL1, CL2, M, SHL, $\overline{EIO1}$, $\overline{EIO2}$, D_0 to D_7, and $\overline{DISPOFF}$ pins.
3. Applies to the V_1, V_3, and V_4 pins.
4. When a device is used outside of the absolute maximum ratings, it may suffer permanent damage. Exceeding the limits may cause malfunctions and have negative effects on device reliability. We recommend that device operating parameters be kept within these limits.

Electrical Characteristics

Table 2 **DC Characteristics (1)** (V_{CC} = 5 V ± l0%, GND = 0 V, $V_{CC} - V_{EE}$ = 10 to 28 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions	Notes
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	$0.2 \times V_{CC}$	V		
Output high level voltage	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	I_{OH} = –0.4 mA	
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA	
Resistance between Vi and Yj	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA	1, 2
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D0 to D7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	$V_{IN} = V_{CC}$ to GND	
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25	—	25	µA	$V_{IN} = V_{CC}$ to V_{EE}	
Current consumption 1	I_{GND}	—	—	—	3.0	mA	f_{CL2} = 8.0 MHz, f_{CL1} = 20 kHz, $V_{CC} - V_{EE}$ = 28 V	3
Current consumption 2	I_{EE}	—	—	150	500	µA		
Current consumption 3	I_{ST}	—	—	—	200	µA		3, 4

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:

$V_{CC} - V_{EE}$ = 28 V
V_1, $V_3 = V_{CC} - 2/10(V_{CC} - V_{EE})$
$V_4 = V_{EE} + 2/10(V_{CC} - V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} - V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that $V_{IH} = V_{CC}$ and V_{IL} = GND.
4. Current during standby.

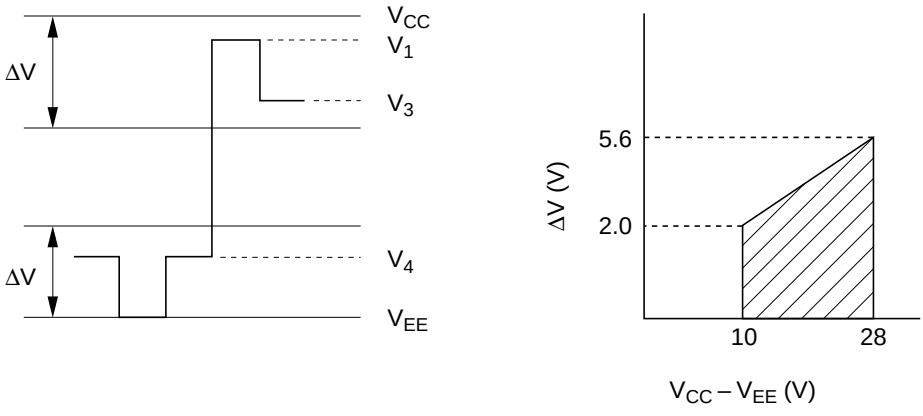


Figure 3 Relationship between Driver Output Waveform and Level Voltages

Table 3 **DC Characteristics (2)** (V_{CC} = 2.5 to 4.5 V, GND = 0 V, V_{CC}–V_{EE} = 10–28 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Typ	Max	Unit	Measurement Conditions
Input high level voltage	V_{IH}	CL1, CL2, M, SHL, D_0 to D_7	$0.8 \times V_{CC}$	—	V_{CC}	V	—
Input low level voltage	V_{IL}	$\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	0	—	$0.2 \times V_{CC}$	V	—
Output high level e voltag	V_{OH}	$\overline{EIO1}$, $\overline{EIO2}$	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA
Output low level voltage	V_{OL}	$\overline{EIO1}$, $\overline{EIO2}$	—	—	0.4	V	I_{OL} = 0.4 mA
Resistance between V_i and Y_j*1, *2	R_{ON}	Y_1 to Y_{80}, V_1, V_3, V_4	—	0.6	1.5	kΩ	I_{ON} = 100 µA
Input leakage current 1	I_{IL1}	CL1, CL2, M, SHL, D_0 to D_7, $\overline{EIO1}$, $\overline{EIO2}$, $\overline{DISPOFF}$, BS	–1.0	—	1.0	µA	V_{IN} = V_{CC} to GND
Input leakage current 2	I_{IL2}	V_1, V_3, V_4	–25	—	25	µA	V_{IN} = V_{CC} to V_{EE}
Current consumption 1*3	I_{GND}	—	—	—	1.5	mA	f_{CL2} = 6.5 MHz f_{CL1} = 16.8 kHz f_M = 35 Hz V_{CC} = 3.0 V V_{CC} – V_{EE} = 28 V
Current consumption 2*3	I_{EE}	—	—	—	500	µA	
Current consumption 3*3, *4	I_{ST}	—	—	—	50	µA	

Notes: 1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:

$V_{CC} – V_{EE}$ = 28 V
V_1, V_3 = $V_{CC} – 2/10(V_{CC} – V_{EE})$
V_4 = $V_{EE} + 2/10(V_{CC} – V_{EE})$

2. Describes the voltage range for the liquid-crystal drive level power supply. A voltage near V_{CC} is supplied to V_1 and V_3. A voltage near V_{EE} is supplied to V_4. Use within the range of ΔV for each. These ranges should be set so that the impedance ROM of the driver output obtained is stable. Note also that ΔV depends on the power supply voltage ($V_{CC} – V_{EE}$). See figure 3.
3. Excluding the current flowing to the input area and output area. When the driver uses an intermediate level for input, a through current flows to the input circuit and the power supply current increases, so be sure that V_{IH} = V_{CC} and V_{IL} = GND.
4. Current during standby.

Table 4 **AC Characteristics (1)** (V_{CC} = 5.0 V ±10%, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	125	—	ns
Clock high level width 2	t_{CWH2}		45		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	30		
Data hold time	t_{DH}				
Clock high level width 1	t_{CWH1}	CL1	45		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	30		
CL2 fall to CL1 fall	t_{SCL}		45		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r		—	50	
Input signal fall time*1	t_f				

Table 5 **AC Characteristics (2)** (V_{CC} = 2.5 V to 4.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Parameter	Symbol	Pin	Min	Max	Unit
Clock cycle time*2	t_{CYC}	CL2	152	—	ns
Clock high level width 2	t_{CWH2}		65		
Clock low level width 2	t_{CWL2}				
Data setup time	t_{DS}	D_0 to D_7, CL2	50		
Data hold time	t_{DH}		40		
Clock high level width 1	t_{CWH1}	CL1	65		
CL2 rise to CL1 rise	t_{LD}	CL1, CL2	20		
CL2 fall to CL1 fall	t_{SCL}		65		
CL1 rise to CL2 rise	t_{LS}				
CL1 fall to CL2 fall	t_{HCL}				
Input signal rise time*1	t_r		—	50	
Input signal fall time*1	t_f		—	50	

Notes (tables 4 and 5):

1. This is the resistance value between the Y pin and V pin (V_1, V_3, V_4, or V_{EE}) when a load current flows to one of the pins Y_1 to Y_{80}. Set with the following conditions:
   $V_{CC} – V_{EE}$ = 28 V
   V_1, $V_3 = V_{CC} – 2/10(V_{CC} – V_{EE})$
   $V_4 = V_{EE} + 2/10(V_{CC} – V_{EE})$
2. t_r, $t_f \leq$ 11 ns

AC Characteristic Test Waveforms

Figure 4 shows test point loading and test waveforms. Connect test points through a 15-pF capacitor to ground, as shown at the top of figure 4.

BS = GND (4-Bit Fetch Mode)

When the data fetch operation enable signal goes low (with SHL = GND and $\overline{EIO2}$ = GND), data standby is cleared. On the next rising edge of clock CL2, the standby is cleared. Figure 5 shows timing for 4-bit fetch mode operation. When CL2 falls, the first 4-bit data fetch is performed. The 4-bit fetches continue on each subsequent falling edge of CL2 until 76 bits have been fetched. The enable signal (when SHL = GND, $\overline{EIO1}$) then goes to GND level. When 80 bits have been fetched, fetch is automatically halted (standby). If the $\overline{EIO1}$ pin is connected to the $\overline{EIO2}$ pin of the next stage, the next device will begin 4-bit fetch operation.

The data output changes when CL1 falls. The output destination for the fetched data when SHL = GND is output pin Y_{80} for d_1, and Y_1 for d_{80}.

When SHL = V_{CC}, the destinations are reversed; d_{80} is output to Y_{80} and d_1 is output to Y_1. The output level (V_1 through $V_{4)}$ is actually selected by the combination of the display data and AC signal M.

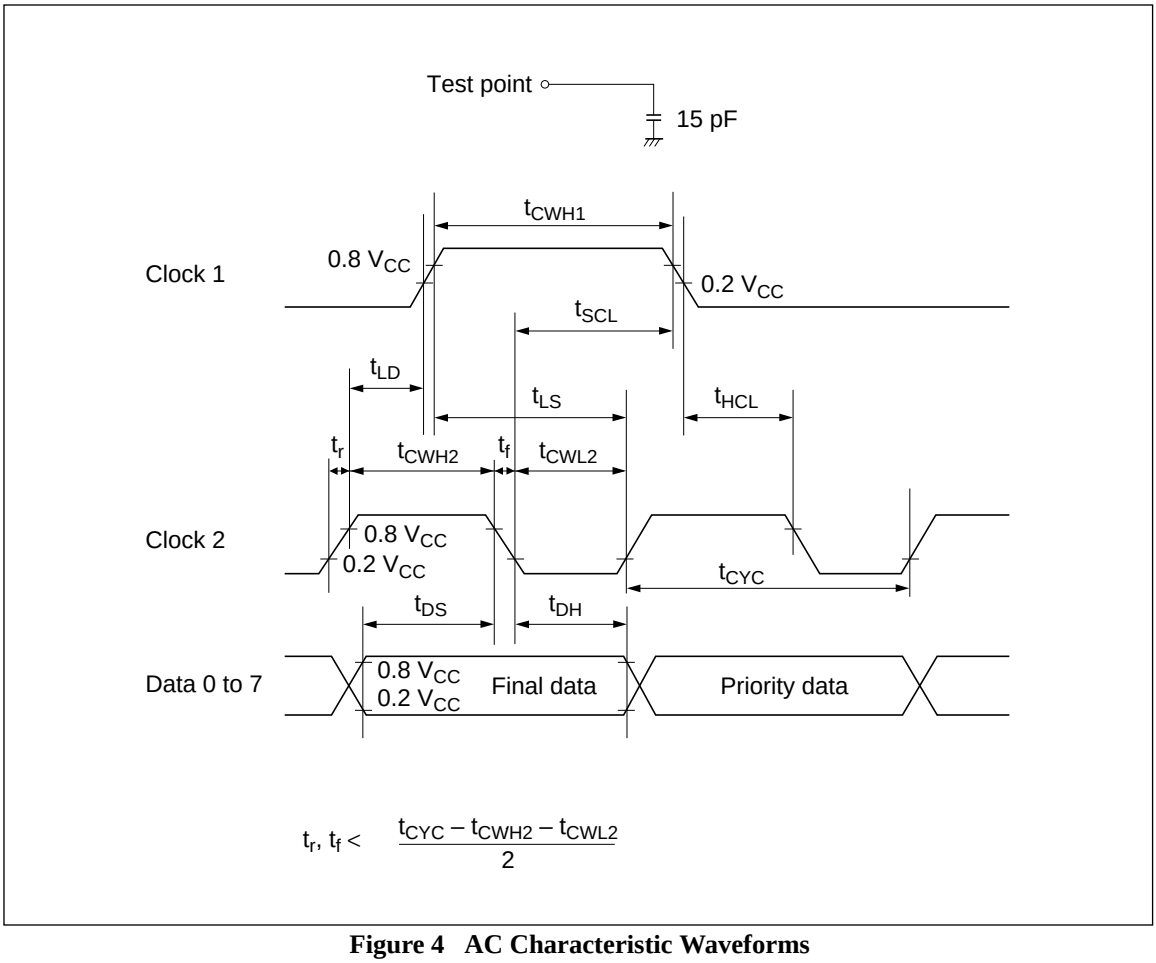


Figure 4 AC Characteristic Waveforms

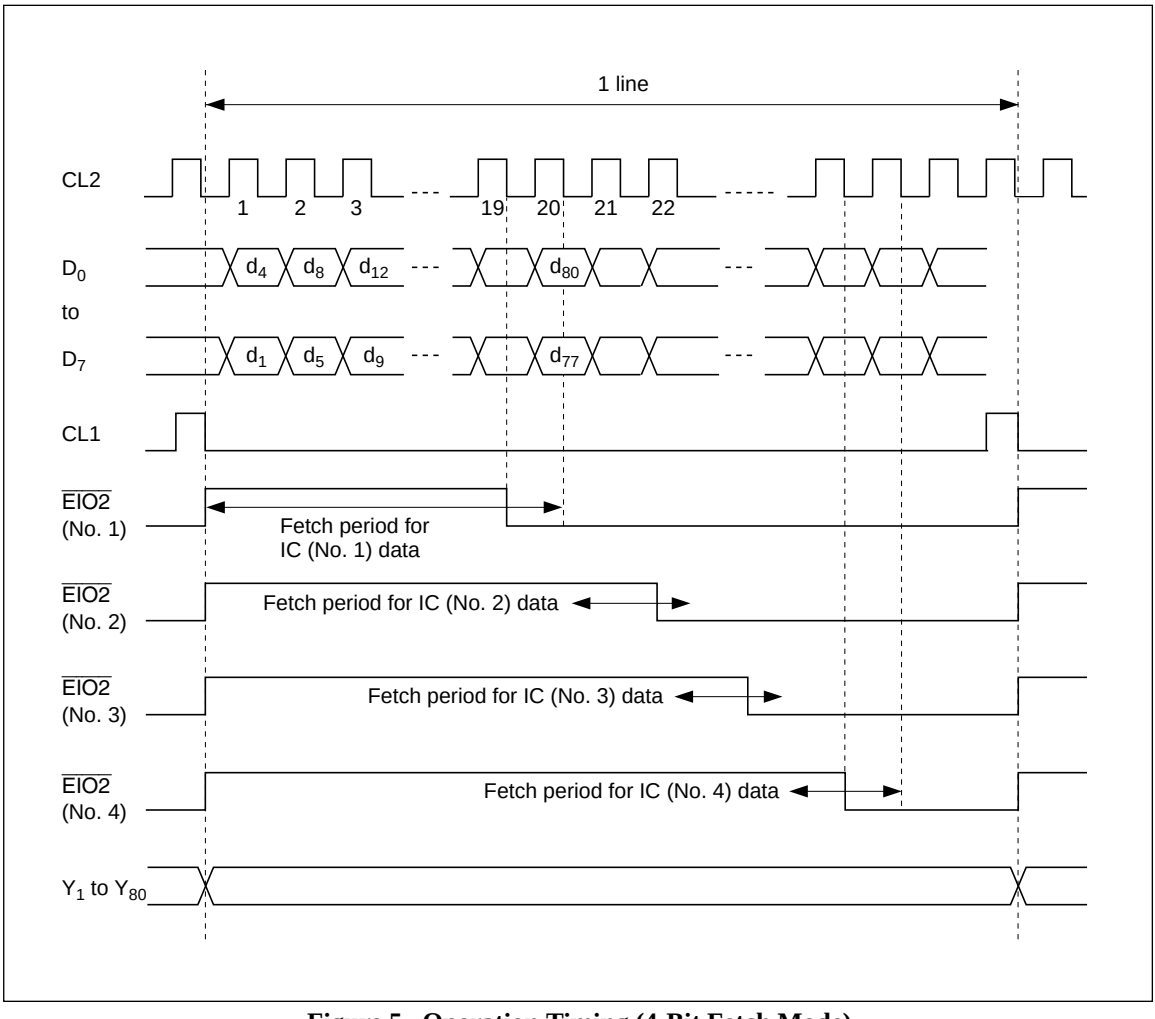


Figure 5 Operation Timing (4-Bit Fetch Mode)

BS = V_{CC} (8-Bit Fetch Mode)

The 8-bit data fetch basic functions are the same as in the 4-bit fetch mode. Figure 6 shows timing for 8-bit fetch mode operation.

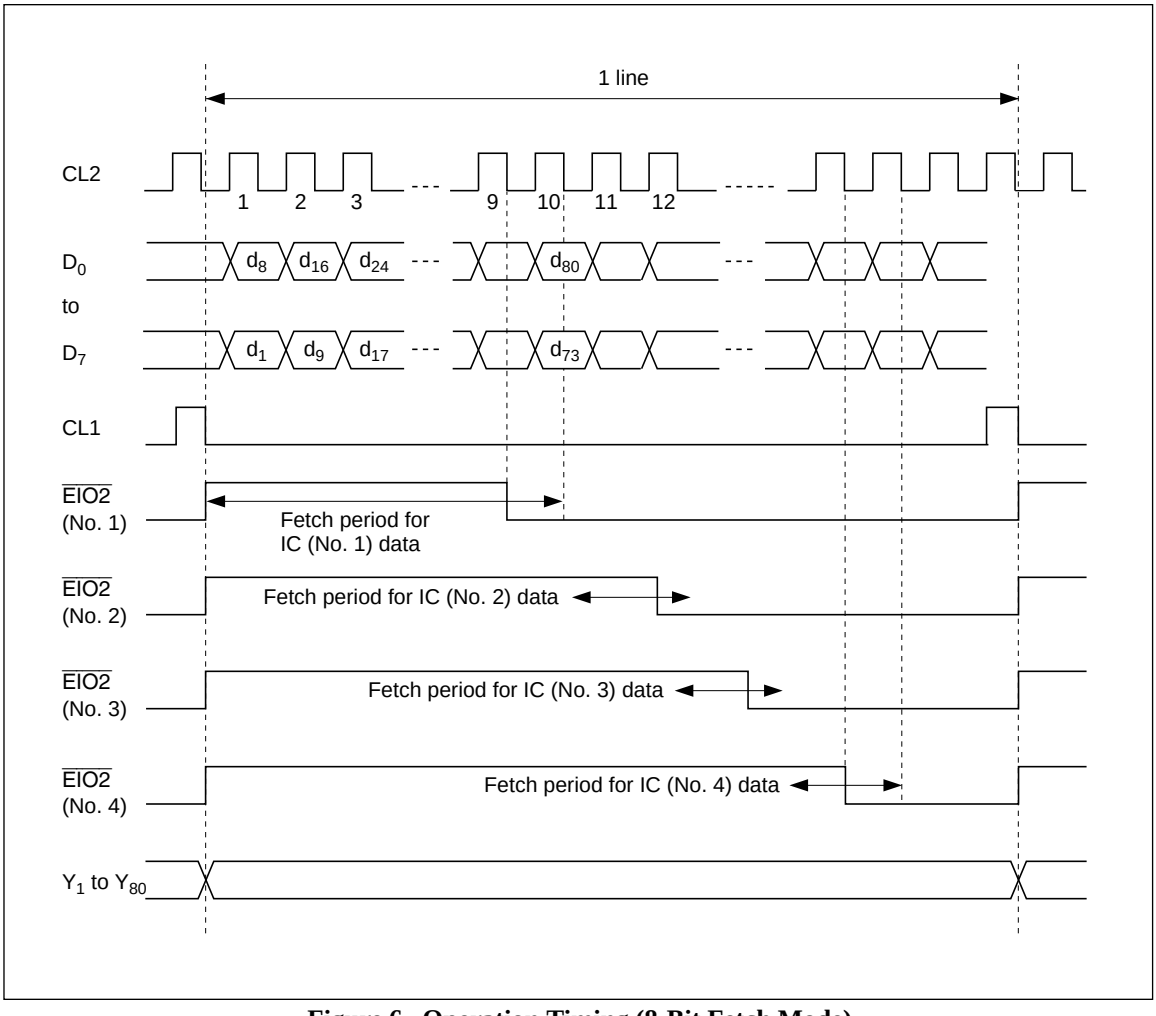


Figure 6 Operation Timing (8-Bit Fetch Mode)