CompactPCI® Backplane Interface / Termination IC

Features

- Twelve channel termination
- Hot-swap capability
- Suitable for non-system slot cards
- Industrial temperature range: -40°C to +85°C
- Typical TCR of resistors: -100 ppm/°C
- Very low capacitance
- 28-pin QSOP or low-profile 28-pin TSSOP package
- Allows backplane termination with minimal PCB footprint

Applications

- Hot-swap CompactPCI cards
- Computer Telephony
- Industrial PCs
- Telecom/Datacom equipment
- Instrumentation
- Industrial Automation

Product Description

The CMCPCI101 is a 12-channel backplane interface/ termination IC specifically designed for the latest version of the CompactPCI specification. The CMCPCI101 allows CompactPCI non-system slot cards to interface to the backplane. To minimize signal reflection and ringing, it provides a 10Ω resistor for each channel to terminate the transmission line stub on the board, per CompactPCI specification.

The CompactPCI standard requires peripheral boards to be hot-swappable. To accommodate this requirement, the CMCPCI101 features a switched 10kΩ resistor connected to the 1V Precharge Supply Voltage which allows for live insertion of boards. If the precharge enable pin (P_EN) is asserted, then the 10kΩ pull-up resistors are connected to precharge the circuits.

The CMCPCI101 integrates these functions into a 28-pin QSOP or a low-profile 28-pin TSSOP package.

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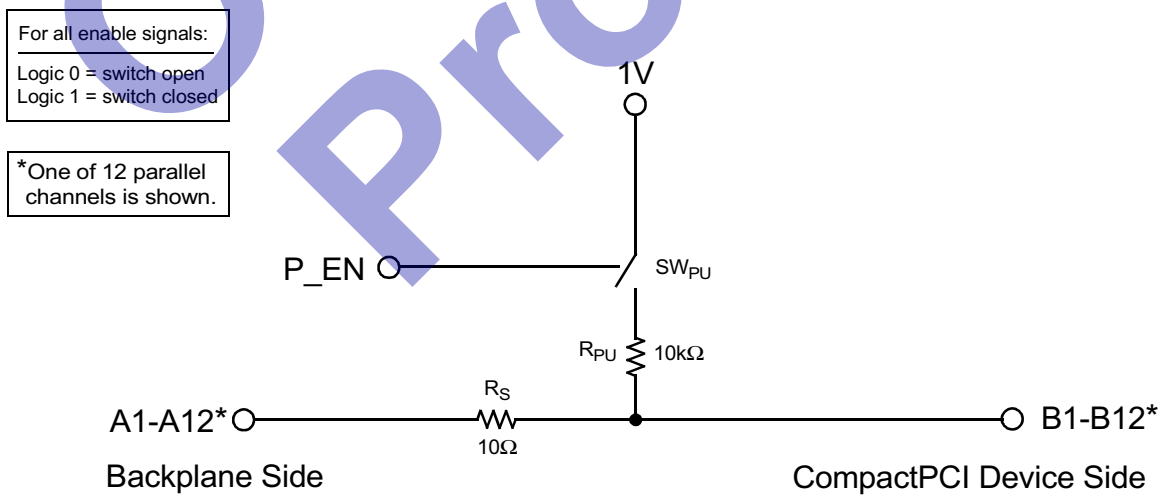
Simplified Electrical Schematic



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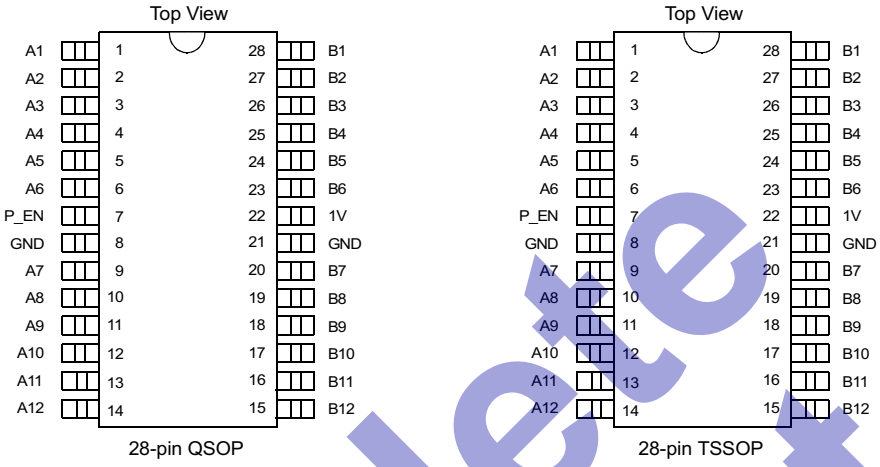
PACKAGE / PINOUT DIAGRAMS



Note: These drawings are not to scale.

PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1-6	A1 - A6	The backplane-side input signals for channels 1 through 6, respectively. These pins are configured with a 10kΩ internal precharge (pull-up) resistor which is switch-controlled by P_EN (pin 8).
9-14	A7 - A12	The backplane-side input signals for channels 7 through 12, respectively. These pins are configured with a 10kΩ internal precharge (pull-up) resistor which is switch-controlled by P_EN (pin 8).
23-28	B1 - B6	The device-side connection for channels 1 through 6, respectively.
15-20	B7 - B12	The device-side connection for channels 7 through 12, respectively.
22	1V	A 1-volt precharge supply voltage input for all channels.
7	P_EN	The precharge enable input which controls the precharge pull-up resistors for all channels. When this active high control signal is set to '1', precharge of channels A1 through A12 is enabled.
8, 21	GND	The ground voltage reference for the CMCPCI101.

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Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Ordering Part Number[1]	Part Marking
28	QSOP	CMCPCI101Q	CMCPCI101Q
28	TSSOP	CMCPCI101T	CMCPCI101TS

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

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Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Pin Voltages		
1V, P_EN	-0.5 to +6.0	V
A1-A12	-0.5 to +6.0	V
B1-B12	-0.5 to +6.0	V
ESD Withstand Voltage (Note 1)		
Human Body Model, MIL-STD-883D, Method 3015 (Note 2)		
1V, P_EN	±2	kV
All other pins	±1.25	kV
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (Ambient)	-40 to +85	°C
DC Power per Resistor	62	mW
Package Power Rating	1	W

Note 1: This parameter guaranteed by design.
Note 2: ESD is applied to input / output pins with respect to GND, one at a time; unused pins are left open.

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Pin Voltages		
1V, P_EN	0 to +5.5	V
A1-A12	0 to +5.5	V
B1-B12	0 to +5.5	V
Ambient Operating Temperature Range	-40 to +85	°C

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Specifications (Cont'd)

ELECTRICAL OPERATING CHARACTERISTICS						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
R_S	Series Resistance through R_S	A to B; T_A=25°C		10		Ω
R_{PU}	Resistance of R_{PU} pull-up	T_A=25°C	9.5	10	15	kΩ
TOL_{RS}	Resistance Tolerance (R_S)	T_A=25°C			±5	%
TCR_{PU}	Temperature Coefficient of Resistance (R_{PU})			-100		ppm/°C
TCR_S	Temperature Coefficient of Resistance (R_S)			+200		ppm/°C
C_1	Capacitance on backplane side (A side) of series resistor R_S	Measured at 66MHz; 30mV osc level; Note 1		1.4		pF
C_2	Capacitance on device side (B side) of series resistor R_S	Measured at 66MHz; 30mV osc level; Note 2		1.9		pF
V_{IL}	Logic Low Input Voltage to P_EN		-0.5		0.5	V
V_{IH}	Logic High Input Voltage to P_EN		2.0		5.5	V
I_{LEAK}	Leakage Current into P_EN	-0.5V < V < 5.5V		±1	±10	µA
t_{PLH}, t_{PHL}	Switch closure delay from the low-to-high or high-to-low transition of enable signal	Note 2			10	ns

Note 1: All parameters specified at T_A=-40 to +85°C unless otherwise noted.
Note 2: This parameter is guaranteed by design; it is not tested 100%.

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Application Information

Board Layout Recommendations

The CMCPCI101 devices should be located on the board as close as possible to the CompactPCI connector. Most of the signals do need to be terminated (with series stub and pull-up resistors), but some signals can be left out depending on the application and the type of board.

For 32-bit peripheral slot boards, the following signals needs to be terminated:

AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, RST#, REQ64#, and ACK64#

If used on the board, the following signals should be terminated:

INTA#, INTB#, INTC# and INTD#

For 64-bit peripheral slot boards, the following signals should also be terminated:

AD32-AD63, C/BE4#-C/BE7#, and PAR64.

Figure 1 shows a 64-bit peripheral board connection between the CMCPCI101 termination and the CompactPCI 5-row connector (2 mm pitch) labeled A to E (row F is Ground). The peripheral slot should have signal lengths not exceeding 63.5 mm (2.5 inches). To minimize trace length, it is recommended that the CMCPCI101s be placed on alternate sides of the PC board. The configuration shown illustrates a fully-terminated 64-bit board utilizing 9 CMCPCI101 devices. Some applications (e.g. 32-bit boards) do not require all lines to be terminated, per the above table.

The CMCPCI101 resistors have a very low TCR (typically -100ppm/°C) so that resistance will not fluctuate over temperature.

A typical peripheral slot card may use 9 CMCPCI101 devices to replace 6 16-bit FET bus switches and 48 4-resistor packs (0805 form factor), thus providing significant reduction in both component count and assembly costs. At the same time this highly integrated solution improves reliability and manufacturing efficiency, saves board area for space-critical designs, and satisfies CompactPCI height requirements.

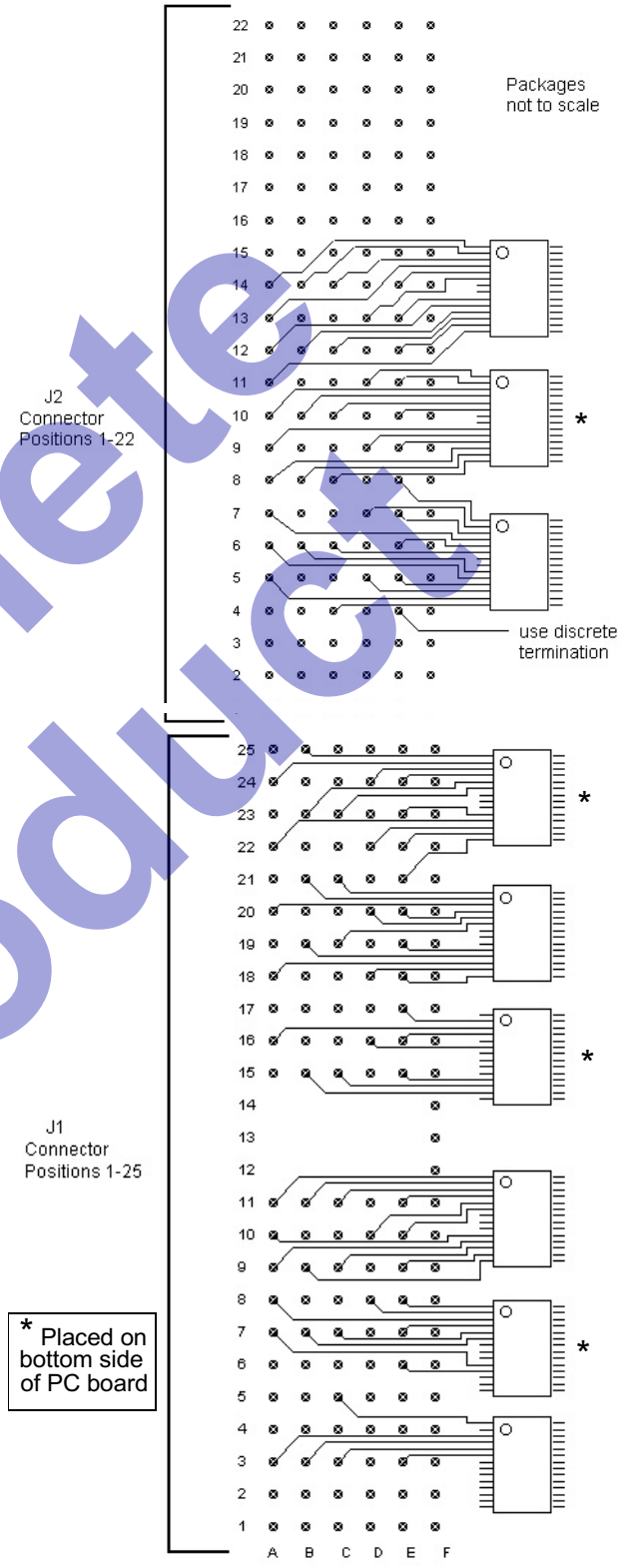

Figure 1. Schematic for 64-bit peripheral board

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Mechanical Details

CMCPCI101 devices are packaged in either 28-pin QSOP packages or low-profile 28-pin TSSOP packages.

QSOP Mechanical Specifications:

Dimensions for CMCPCI101 devices packaged in 28-pin QSOP packages are presented below.

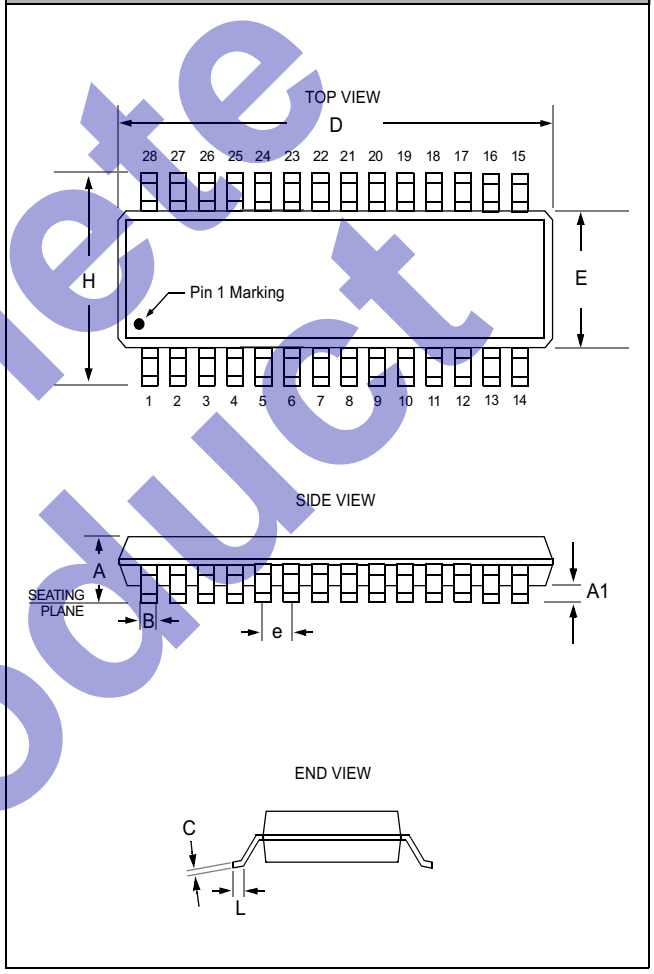
For complete information on the QSOP-28 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS

Package	QSOP (JEDEC name is SSOP)			
Pins	28			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	9.80	9.98	0.386	0.393
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling Dimensions: inches				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for QSOP-28

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TSSOP Mechanical Specifications

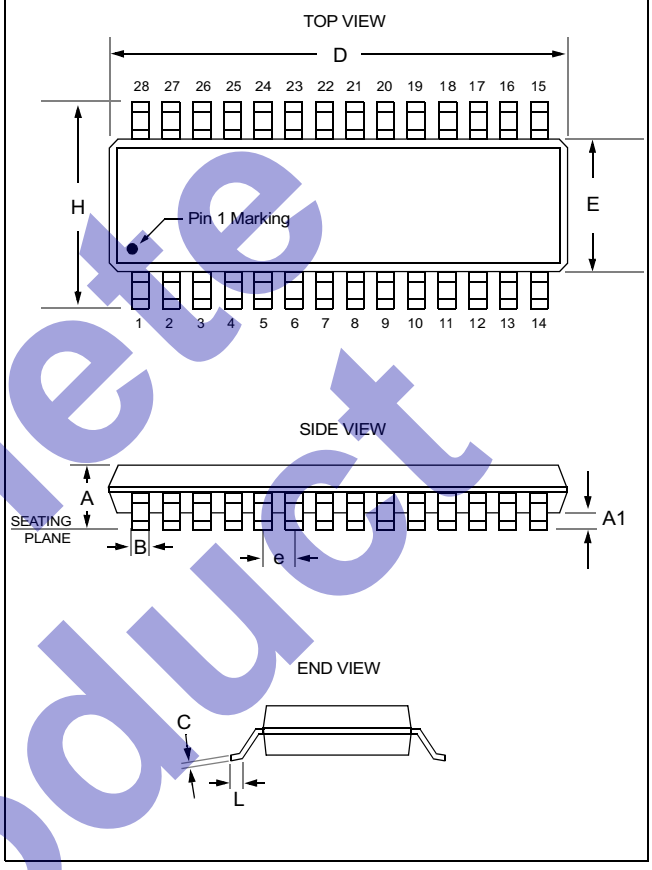
Dimensions for CMCPCI101 devices packaged in 28-pin TSSOP packages are presented below.

For complete information on the TSSOP-28 package, see the California Micro Devices TSSOP Package Information document.

PACKAGE DIMENSIONS				
Package	TSSOP			
Pins	28			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	—	1.10	—	0.0433
A1	0.05	0.15	0.002	0.006
B	0.19	0.30	0.0075	0.0118
C	0.09	0.20	0.0035	0.0079
D	9.60	9.80	0.378	0.386
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for TSSOP-28

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