Signetics

68155
Interrupt Handler

Product Specification

Military Microprocessor Products

DESCRIPTION

The Signetics 68155 is an asynchronous interrupt handler for VMEbus and VERSAbus® systems. Up to 14 interrupts are prioritized by the 68155 to one of seven levels and are output on the interrupt priority level lines (IPLON-IPL2N). The 68155 prioritizes the interrupts in the following manner: local bus requests over system bus requests with the non-maskable interrupt (NMIN) considered the highest priority local interrupt (NMIN over IRQ7N, then LRQ6N-LRQ1N over IRQ6N-IRQ1N).

The local interrupt requests can be programmed to be either active high or low, and either edge of level sensitive. The system bus interrupt requests are always active low and level sensitive. The non-maskable interrupt is always negative edge-triggered.

During a local interrupt acknowledge sequence, two modes of response are available: vectored mode or device-supplies-the vector mode.

For system bus responses, the 68155 works with a bus requester (for example, the 68172 VMEbus Controller), to acquire a status/ID byte (interrupt vector) for the system.

The 68155 was designed primarily for interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

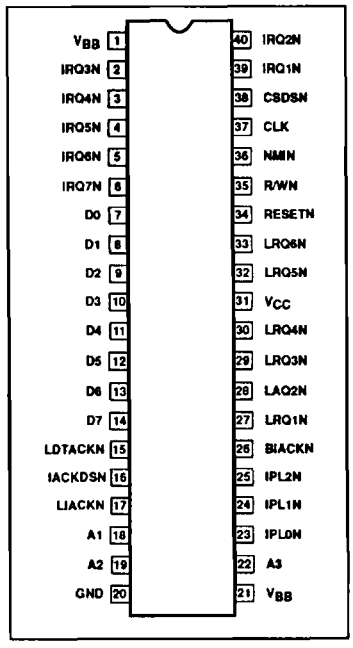
FEATURES

- **Asynchronous interrupt handler for VMEbus and VERSAbus® systems**
- **Receives and prioritizes non-maskable, six local and seven system bus interrupts**
- **Interrupts may be polled in lieu of real-time operation**
- **Programmable local interrupt response**
- **Complete device status, including last interrupt acknowledged**
- **High-speed bipolar technology**

ORDERING INFORMATION

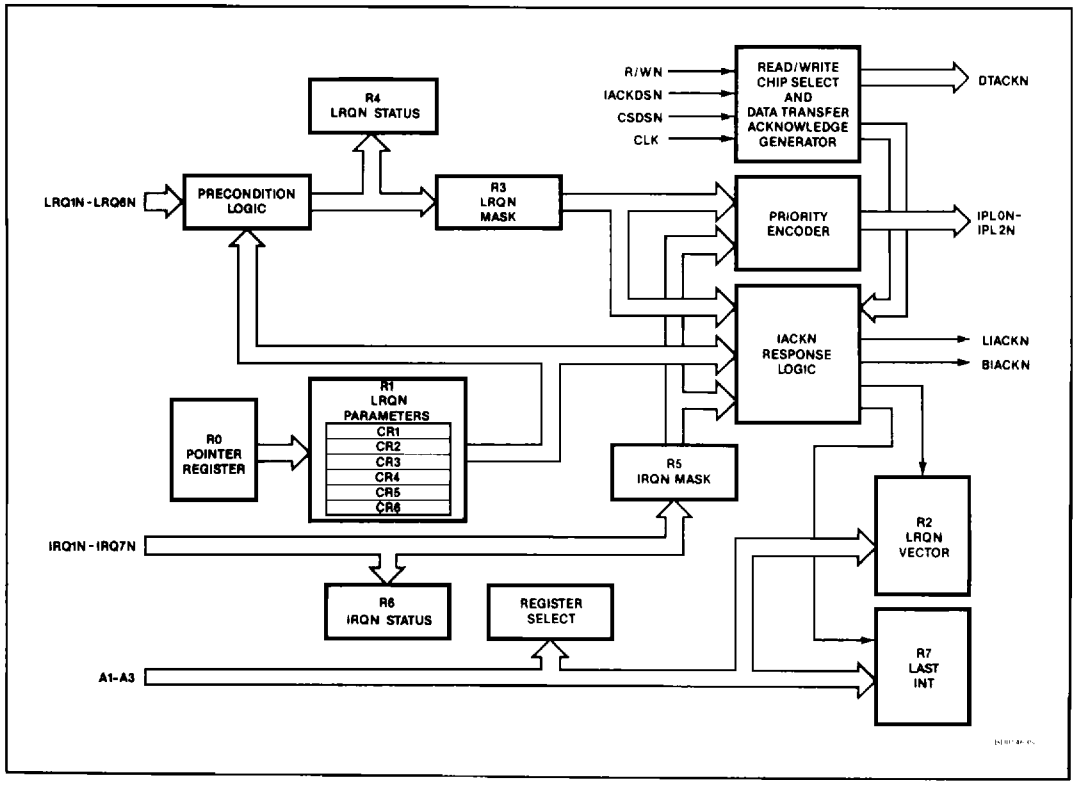
PACKAGE	ORDERING CODE
40–Pin Ceramic DIP	68155/BQA

PIN CONFIGURATION



VERSAbus is a registered trademark of Motorola, Inc.

BLOCK DIAGRAM



Interrupt Handler | 68155

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{BB}	1, 21	I	**Supply Voltage:** Supply voltage for internal gates.
IRQ1N – IRQ7N	39, 40, 2 – 6	I	**Bus Interrupt Request:** Active–Low inputs for bus–generated interrupts.
D0 – D7	7 –14	I/O	**Bus Data:** 3–State local data bus.
LDTACKN	15	O	**Local Data Transfer Acknowledge:** Acitive–Low, open–collector output. Indicates that valid data is available on the local data bus during interrupt acknowledge cycle or data transfer cycle.
IACKDSN	16	I	**Interrupt Acknowledge:** Active–Low interrupt acknowledge input from the local master. This signal must be qualified by the local master's data strobe prior to input.
LIACKN	17	O	**Local Interrupt Acknowledge:** Active–Low interrupt acknowledge totem–pole output to the local interrupting devices.
A1 – A3	18, 19, 22	I	**Address Lines:** Address inputs from local master.
GND	20	I	**Ground**
IPL0N – IPL2N	23 – 25	O	**Interrupt Priority Level:** Active–Low totem–pole outputs to the local master. The priority level of the interrupt request is encoded on these outputs.
BIACKN	26	O	**Bus Interrupt Acknowledge:** Acitve–Low interrupt acknowledge totem–pole output to the system bus.
LRQ1N – LRQ6N	27 – 30, 32, 33	I	**Local Interrupt Request:** User can define the active state of these inputs.
V_{CC}	31	I	**Supply Voltage:** +5V power supply.
RESETN	34	I	**Reset:** Active–Low input reset.
R/WN	35	I	**Read/Write:** This signal specifies the data transfer cycle to be either read or write.
NMIN	36	I	**Non–Maskable Interrupt:** Active–Low highest priority interrupt.
CLK	37	I	**Clock:** Clock input (typically CPU clock).
CSDSN	38	I	**Chip Select:** Active–Low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Supply voltage range[3]	–0.5 to +7.0	V
V_I	Input voltage range[3]	–0.5 to +5.5	V
V_O	Voltage applied to output in OFF–State[3]	–0.5 to +5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATINGS			UNIT
		Min	Nom	Max	
V_{BB}	Supply voltage range	1.35	1.5	1.65	V
V_{CC}	Supply voltage range	4.5	5.0	5.5	V
V_{IH}	High level input voltage range	2.0			V
V_{IL}	Low level input voltage range			0.8	V
I_{OL}	Low level output current range			8.0	mA
I_{OH}	High level output current range			–3.0	µA
T_A	Operating free–air temperature range[2]	–55 to +125			°C

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C^2$, $4.5V \leq V_{CC} \leq 5.5V^5$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[4]		UNIT
			Min	Max	
V_{CC}	Supply voltage range		4.5	5.5	V
V_{BB}	Supply voltage range		1.35	1.65	V
I_{CC}	V_{CC} supply current range	V_{CC} = 5.5V		100	mA
I_{BB}	V_{BB} supply current range	V_{BB} = 1.65V		200	mA
I_{IL}	Input Low current range	V_{CC} = 5.5V, V_{BB} = 1.65V, V_{IL} = 0.4V		–20	µA
I_{IH}	Input High current range	V_{CC} = 5.5V, V_{BB} = 1.65V, V_{IH} = 2.7V		20	µA
I_{OS}	Short circuit output current except LDTACKN	V_{CC} = 5.5V, V_{OUT} = 0V[6]	–15	–100	mA
V_{OL}	Output Low voltage range	V_{CC} = 4.5V, V_{BB} = 1.35V, I_{OL} = 8mA		0.6	V
V_{OH}	Output High voltage except LDTACKN (open collector)	V_{CC} = 4.5V, V_{BB} = 1.35V, I_{OH} = –3mA	2.5		V
I_I	Input leakage current	V_{CC} = 5.5V, V_I = 5.5V		100	µA
I_{CEX}	Open–Collector leakage current LDTACKN	V_{CC} = 4.5V, V_O = 4.5V		100	µA
V_{IC}	Input clamp voltage	V_{CC} = 4.5V, I_{IK} = –10mA	–1.5		V
V_{IL}	Input Low voltage			0.8	V
V_{IH}	Input High voltage		2.0		V

AC ELECTRICAL CHARICTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			Min	Max	
t_{RWS}	3 & 4	R/WN TO CSDSN Low set up time	5		ns
t_{IAKS}	3 & 4	IACKDSN High to CSDSN Low set up time	42		ns
t_{ADRS}	3 & 4	A1 – A3 valid to CSDSN Low set up time	29		ns
t_{DTV}	3	CSDSN Low to D0 – D7 set up time		164	ns
t_{ACCR}	3	CSDSN Low to LDTACKN Low read access time	CLK + 33	2CLK + 175	ns
t_{RWH}	3 & 4	CSDSN High to R/WN High hold time	16		ns
t_{ADRH}	3 & 4	CSDSN High to A1 – A3 valid hold time	6		ns
t_{DTH}	3 & 4	CSDSN High to D0 – D7 valid hold time	34	104	ns
t_{TST}	3	CSDSN High to D0 – D7 3–State	34	104	ns
t_{ACK}	3 & 4	CSDSN High to LDTACKN High time	15	56	ns
t_{CSH}	3 & 4	CSDSN High time	42		ns
t_{DTCS}	3 & 4	LDTACKN Low to CSDSN High	18		ns
t_{DS}	4	D0 – D7 valid to CSDSN Low set up time	0		ns
t_{ACCW}	4	CSDSN Low to LDTACKN Low write access time	CLK + 33	2CLK + 175	ns
t_{CSS}	5, 6 & 7	CSDSN High to IACKDSN Low set up time	42		ns
t_{PDL}	5 & 6	IACKDSN Low to LIACKN Low propagation time	CLK + 33	2CLK + 175	ns
t_{DAV}	5	IACKDSN Low to D0 – D7 vector valid		189	ns
t_{ACCV}	5	IACKDSN Low to LDTACKN Low (vector access time)	CLK + 33	2CLK + 175	ns
t_{IKH}	5, 6 & 7	IACKDSN High time	42		ns
t_{DAH}	5	IACKDSN High to D0 – D7 valid hold time	34	104	ns
t_{TRST}	5	IACKDSN High to D0 – D7 3–State	34	104	ns
t_{IKDT}	5	IACKDSN High to LDTACKN High	15	56	ns
t_{PDH}	5 & 6	IACKDSN High to LIACKN High propagation delay	15	56	ns
t_{DTIK}	5	LDTACKN Low to IACKDSN High time	18		ns
t_{ADRS}	5, 6 & 7	A1 – A3 valid to IACKDSN Low set up time	29		ns
t_{ADH}	5, 6 & 7	IACKDSN High to A1 – A3 valid hold time	6		ns
t_{PDL2}	7	IACKDSN Low to BIACK Low propagation delay	CLK + 33	2CLK + 175	ns
t_{PDH2}	7	IACKDSN High to BIACK High propagation delay	15	56	ns
t_{RST}	8	RESET Low time	31		ns
t_{CKPD}	9	Clock period	100		ns
t_{CKH}	9	Clock High	45		ns
t_{CKL}	9	Clock Low	35		ns
t_S	9	CSDSN Low to clock High set up time	45		ns

NOTES:

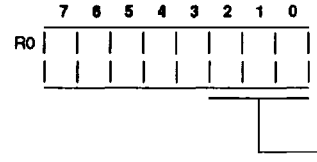
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of ≤3ns maximum and output voltages are checked at 1.5V.
6. At any time, no more than one output should be connected to ground.
7. t_{TST} is always greater than or equal to t_{DTH}.
8. Signal number t_{TRST} is always greater than or equal to signal number t_{DAH}.

REGISTERS

The 68155 contains eight internal registers (R0 – R7) accessible to the local master. There are also six sub–registers contained in register R1. Register R0 specifies which sub–register is to be accessed in R1. Register R2 stores the interrupt vector for vectored mode responses. Register R3 and R5 are the interrupt mask registers for the local and system bus interrupts, respectively. Registers R4 and R6 are the status registers for local and bus interrupts, respectively, allowing all interrupts to be polled. Register R7 can be read by the local master to determine the last interrupt acknowledged.

All data transfers between the 68155 and the local master are done using the local data bus (D0 – D7), address bus (A1 – A3), a chip select (CSDSN) and a read/write (R/WN) input.

Register R0 — A3A2A1 = 000

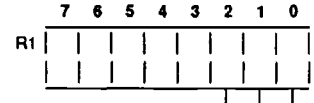


Pointer register (write only).
Bit 0 – 2 of R0 specify which control sub–register CR1 – CR6 during an access of R1.
During register I/O, bits 7 – 3 will read as 0.

B2 – B1 – B0

000 – none	100 – CR4
001 – CR1	101 – CR5
010 – CR2	110 – CR6
011 – CR3	111 none

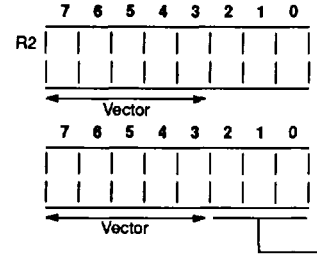
Register R1 — A3A2A1 = 001



Control registers CR1 – CR6 (read or write).
These six registers program the function of the local interrupt requests (LRQ1N – LRQ6N).
(CR1 programs LRQ1N, CR2 programs LRQ2N, etc.).
During register I/O, bits 7 – 3 will be read as 0.

LRQnN active state (High/Low)	(1 = active High)
LRQnN edge/level sensitive	(1 = edge sensitive)
LRQnN vector enable	(1 = enabled)

Register R2 — A3A2A1 = 010

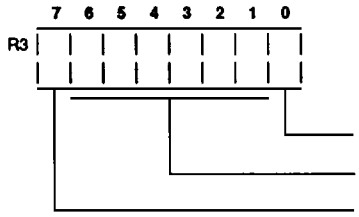


LRQ vector (read or write).
Bits 7 – 3 of this register are the top five bits of the local interrupt vector.
During register I/O, bits 2 – 0 will be read as zeros.

LRQ vector output during local interrupt acknowledge (if vector enable = 1).

001 – LRQ1N	100 – LRQ4N
010 – LRQ2N	101 – LRQ5N
011 – LRQ3N	110 – LRQ6N
	111 – NMIN

Register R3 — A3A2A1 = 011

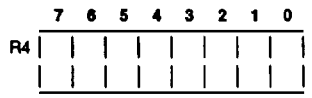


LRQ mask (read or write).
This register allows the user to mask local interrupts. It also enables vectored response for NMIN.

NMIN Vector enable (1 = enabled)
LRQN 1 – 6 mask (1 = interrupt enabled)
NMIN mask (1 = NMIN enabled)

Bit 1 = LRQ1N
Bit 2 = LRQ2N
Bit 3 = LRQ3N
Bit 4 = LRQ4N
Bit 5 = LRQ5N
Bit 6 = LRQ6N
Bit 7 = NMIN

Register R4 — A3A2A1 = 100

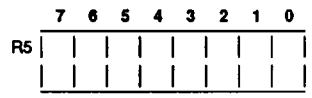


LRQ status (read only).
Local interrupts can be polled through this register.
During register I/O, bit 0 will be read as a 0.

Bit 1 = LRQ1N
Bit 2 = LRQ2N
Bit 3 = LRQ3N
Bit 4 = LRQ4N
Bit 5 = LRQ5N
Bit 6 = LRQ6N
Bit 7 = NMIN

LRQN status (1 = interrupt pending)
NMIN stauts (1 = interrupt pending)

Register R5 — A3A2A1 = 101

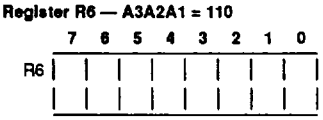


IRQ mask (read or write).
This register allows the user to mask system bus interrupts.
During register I/O, bit 0 will be read as a 0.

Bit 1 = IRQ1N
Bit 2 = IRQ2N
Bit 3 = IRQ3N
Bit 4 = IRQ4N
Bit 5 = IRQ5N
Bit 6 = IRQ6N
Bit 7 = IRQ7N

(1 = interrupt enabled)

Register R6 — A3A2A1 = 110

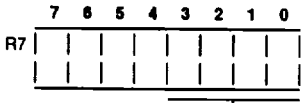


IRQ status (read only).
System bus interrupts can be polled through this register.
During register I/O, bit 0 will be read as 0.

Bit 1 = IRQ1N
Bit 2 = IRQ2N
Bit 3 = IRQ3N
Bit 4 = IRQ4N
Bit 5 = IRQ5N
Bit 6 = IRQ6N
Bit 7 = IRQ7N

IRQN status (1 = interrupt pending)

Register R7 — A3A2A1 = 111



Last interrupt acknowledged (read only).
This register can be read by the local CPU to determine the last interrupt acknowledged. During register I/O, bits 7 – 4 will be read as 0.

0000 – none	1000 – none
0001 – IRQ1N	1001 – LRQ1N
0010 – IRQ2N	1010 – LRQ2N
0011 – IRQ3N	1011 – LRQ3N
0100 – IRQ4N	1100 – LRQ4N
0101 – IRQ5N	1101 – LRQ5N
0110 – IRQ6N	1110 – LRQ6N
0111 – IRQ7N	1111 – NMIN

FUNCTIONAL OPERATION

Typical Configuration

The 68155 can handle interrupts from 14 sources: seven bus interrupt requests generated on the IRQ1N – IRQ7N inputs, six local interrupt sources generated on the LRQ1N – LRQ6N inputs, and one non–maskable interrupt which may originate locally or from the system (such as the system's AC fail signal). All interrupts are encoded to one of seven levels and output on the IPL0N – IPL2N lines. Table 1 shows how the 68155 encodes the interrupts.

BIACKN is the bus interrupt acknowledge signal which is asserted during a bus interrupt acknowledge sequence. BIACKN can be used to get the associated bus requester (for example, the Signetics 68172), to acquire an interrupt vector from the system bus. Figure 1 shows a typical 68155 – 68172 system configuration.

LIACKN is the local interrupt acknowledge signal which is asserted during a local interrupt acknowledge sequence. Figure 2 shows a typical configuration for the 68155.

Non–Maskable Interrupt (NMI)

The highest priority interrupt request is the non–maskable interrupt (NMIN). It is an Active–Low, negative edge–triggered interrupt. NMIN is considered by the 68155 to be the highest priority local interrupt, however, the user is not restricted to having it represent a local device. When the local master responds to an NMIN, bit 7 in the LRQ status register R4 is cleared to 0.

Both vectored and device–supplies–the–vector modes are available with NMIN. However, it is recommended that the 68155 response to an NMIN be a vectored mode interrupt acknowledge.

Local Interrupts

The 68155 can handle interrupts generated by local devices through its six local interrupt request lines (LRQ1N – LRQ6N). The local interrupt requests are prioritized with LRQ6N being the highest priority, and LRQ1N the lowest priority.

The response of the 68155 to an acknowledge of a local interrupt can be selected by means of the 68155 R1 register. Pointer register R0 points to one of the six control sub–registers when accessing register R1. The six control registers (CR1 – CR6) in register R1 define the functions of the six local interrupt requests (LRQ1N – LRQ6N).

Control Register 'n' Bit 0
Selects local interrupt requests 'n' (LRQnN), to be either Low or High. Bit 0 = 1 defines active state to be High.

Control Register 'n' Bit 1
Selects local interrupt request 'n', to be either edge or level sensitive. Bit 1 = 1 defines LRQnN to be edge sensitive.

Control Register 'n' Bit 2
Selects either vectored mode or device–supplies–the–vector mode response. Bit 2 = 1 enables vectored mode operation for LRQnN.

Two modes of operation for a local interrupt response are possible; vectored mode and device–supplies–the–vector mode. In vectored mode, the 68155 supplies the interrupt vector to the local CPU and asserts LDTACKN to complete the transfer. In the device–supplies–the–vector mode, the local interrupting device supplies its own interrupt vector and asserts LDTACKN to complete the transfer.

The vector register R2 allows the user to program the five most significant bits (bits 7 – 3) of the interrupt vector supplied in vectored mode. During a vectored local interrupt acknowledge cycle, the upper five bits of the vector register are concatenated with a 3–bit interrupt level (address lines A3 = B2 of the vector, A2 = B1 and A1 = B0). This forms the unique vector for the local interrupt request level being acknowledged.

The local interrupt request mask register R3 allows the user to selectively enable local interrupt requests by setting appropriate bits in the register.

The current state of the local interrupt requests can be determined by the local master by reading the local interrupt status register R4.

Local Interrupt Acknowledge

An interrupt acknowledge, by the local CPU, is signified by the assertion of the interrupt acknowledge input (IACKDSN). The 68155 responds by reading the three address lines (A1 – A3) to determine what level is being acknowledged. If a local interrupt is the highest priority interrupt pending on the level acknowledged, the 68155 will respond as though it is programmed for that level.

If vectored mode is programmed, the 68155 will assert the local interrupt acknowledge (LIACKN) and place the interrupt vector on the local data bus. To complete the transfer of the vector to the local CPU, the 68155 asserts the local data transfer acknowledge signal (LDTACKN).

If device–supplies–the–vector mode is programmed, the 68155 asserts the local interrupt acknowledge signal (LIACKN). The interrupting device is then allowed to place its own vector on the local data bus and assert LDTACKN.

When a local interrupt is acknowledged by the local master, the appropriate bit in the LRQ status register R4 is cleared to 0.

Bus Interrupts

The VMEbus specification defines a maximum of seven interrupt levels. The 68155 can handle seven system bus interrupts through its IRQ1N – IRQ7N lines. Bus interrupt requests are Active–Low level sensitive, and prioritized with IRQ7N being the highest priority and IRQ1N the lowest priority. The bus mask control register R5 allows the user to selectively enable bus interrupt requests by setting appropriate bits in

the register. The local CPU can read the bus interrupt status register R6 to determine the current state of the bus interrupt requests.

Bus Interrupt Acknowledge

The local CPU asserts the interrupt acknowledge signal (IACKDSN) to signify an interrupt acknowledge. The 68155 responds by reading the interrupt level on A1 – A3 to determine what level is being acknowledged. If a local interrupt is not pending on the level acknowledged, and that bus level is not masked, the 68155 will assert bus interrupt acknowledge (BIACKN). If that bus level is masked, the 68155 will not respond to the interrupt acknowledge by the local master.

Part of the interrupt acknowledge sequence for a bus interrupt consists of acquiring a vector (status/ID byte) from the system bus.

The bus signals required to acquire this vector are available with a bus controller. The Signetics 68172 bus controller can be used by the 68155 to acquire the vector (status/ID byte), thereby eliminating the need for the 68155 to duplicate this bus control functions. Because most interrupts are serviced by boards that already have the 68172, a one–chip addition of the 68155 gives that board complete interrupt handling capability.

Since the 68155 is an asynchronous device, it is possible for a local interrupt request to be asserted during acknowledgement of a bus interrupt on the same level. The 68155 passes all local interrupt requests through transparent latches which close during each interrupt acknowledge cycle. All possibility of contention is therefore eliminated.

Reset

When RESETN is asserted, the 68155 drives LDTACKN, LIACKN, BIACKN and IPL0N – IPL2N all High. The D0 – D7 I/O pins go to 3–State and all internal registers are cleared.

Table 1. 68155 Interrupt Level Encoding

INTERRUPT REQUEST LEVEL	INTERRUPT PRIORITY LEVEL OUTPUTS		
	IPL2N	IPL1N	IPL0N
NMIN, IRQ7N	0	0	0
LRQ6N, IRQ6N	0	0	1
LRQ5N, IRQ5N	0	1	0
LRQ4N, IRQ4N	0	1	1
LRQ3N, IRQ3N	1	0	0
LRQ2N, IRQ2N	1	0	1
LRQ1N, IRQ1N	1	1	0
None	1	1	1

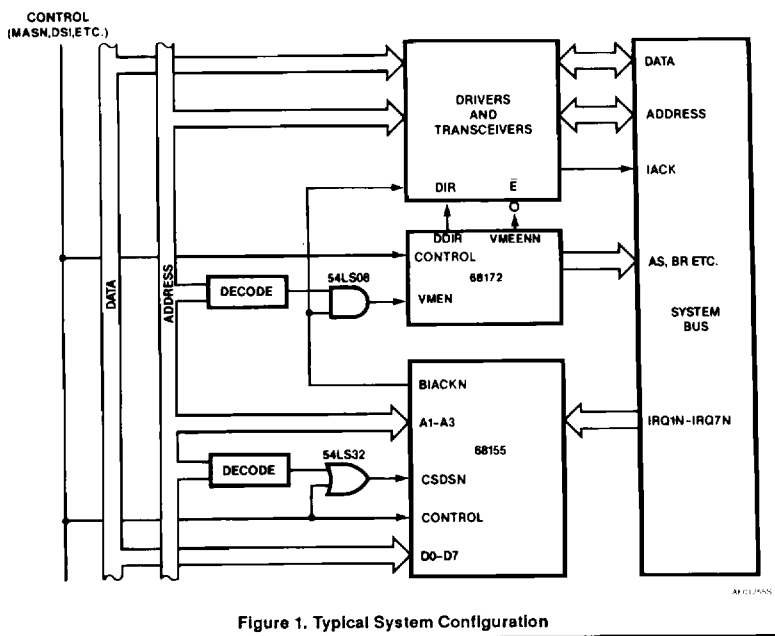


Figure 1. Typical System Configuration

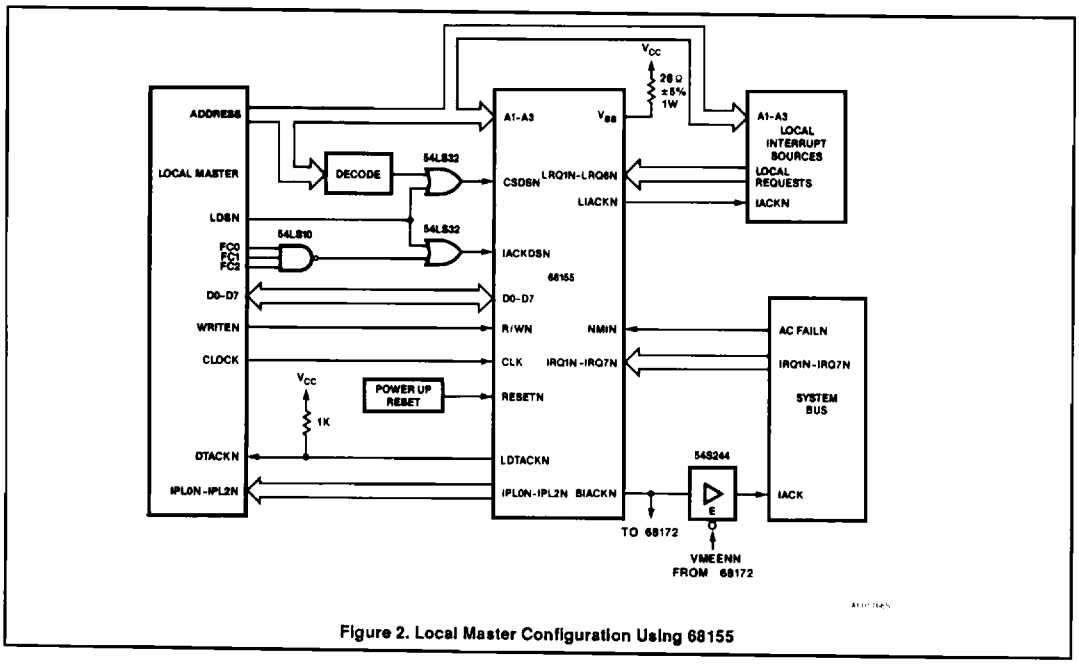
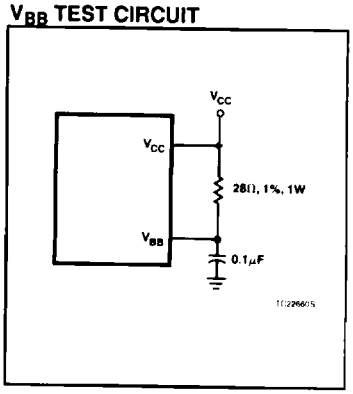
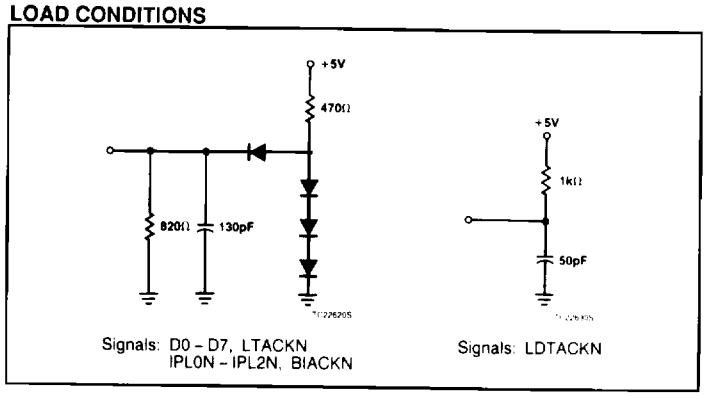


Figure 2. Local Master Configuration Using 68155

V_{BB} TEST CIRCUIT



LOAD CONDITIONS



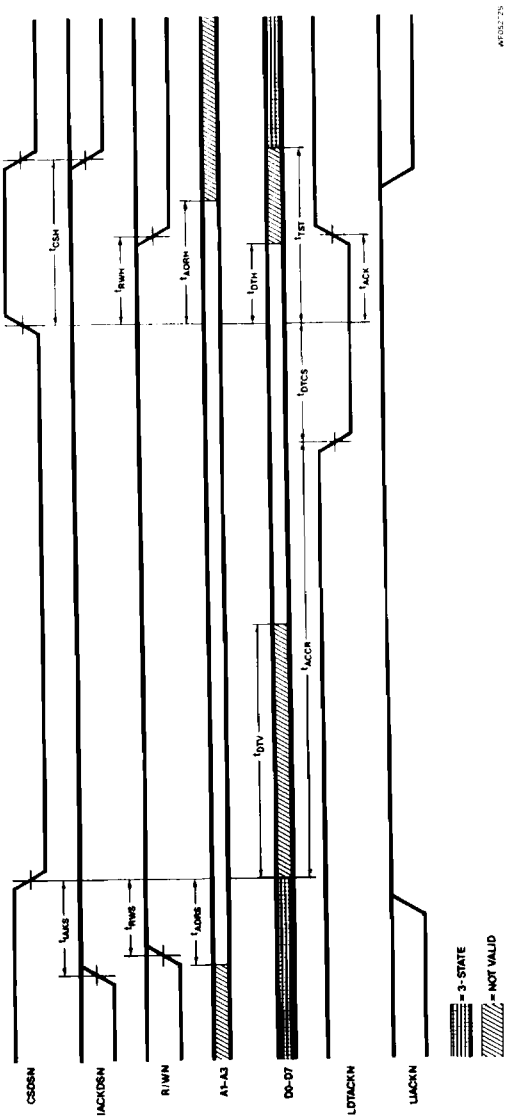


Figure 3. Register Read[5]

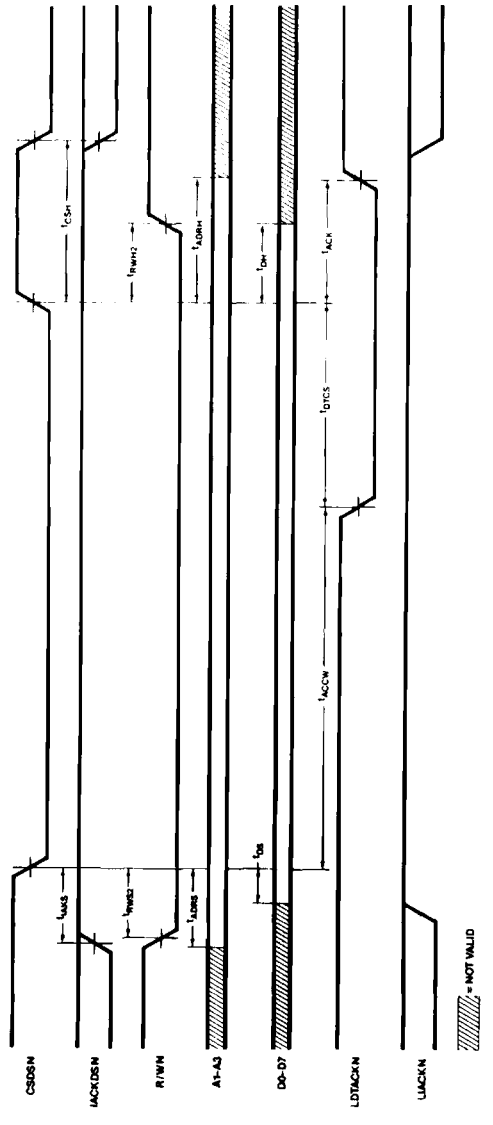


Figure 4. Register Write[5]

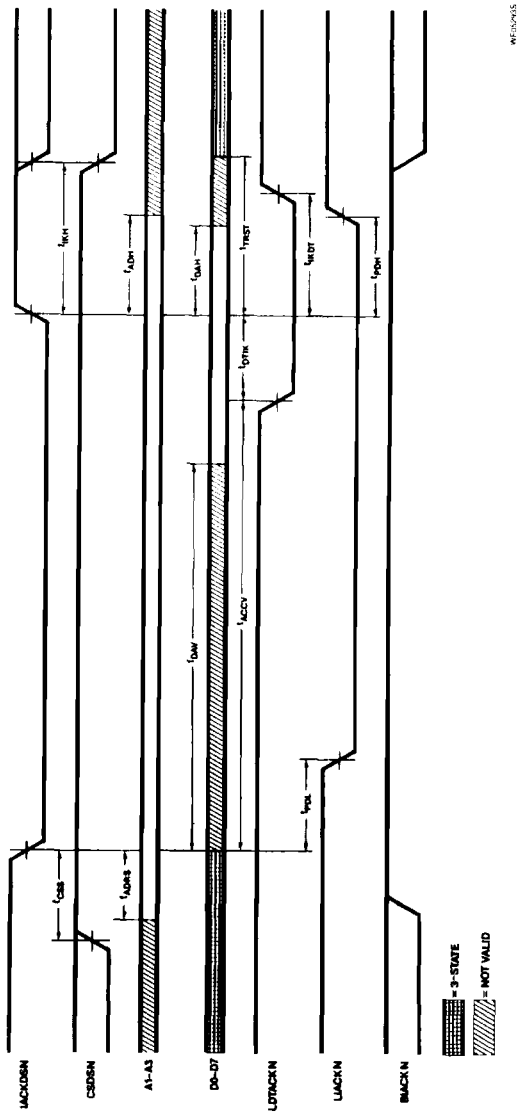


Figure 5. Local Interrupt Acknowledge (Vector Mode)[5]

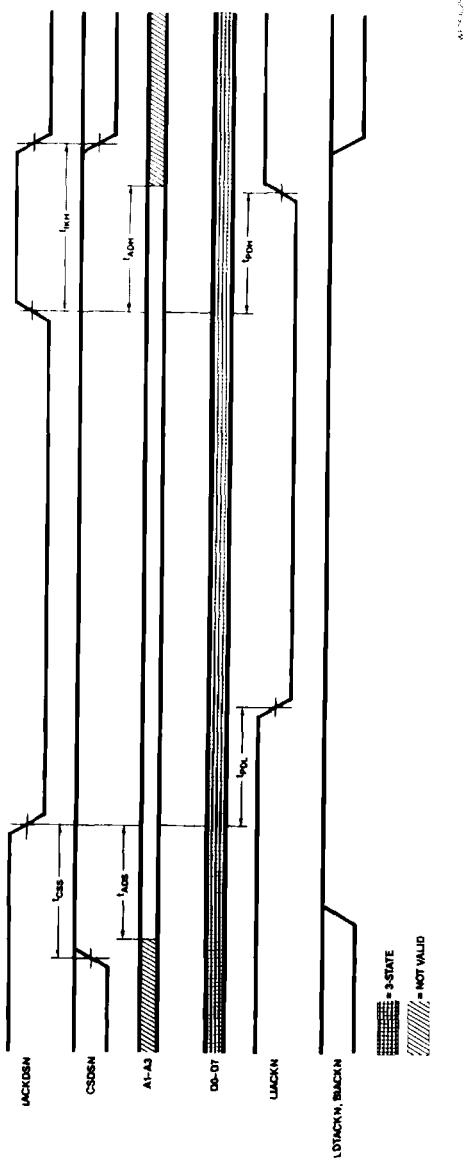


Figure 6. Local Interrupt Acknowledge (Non-Vectored Mode)[5]

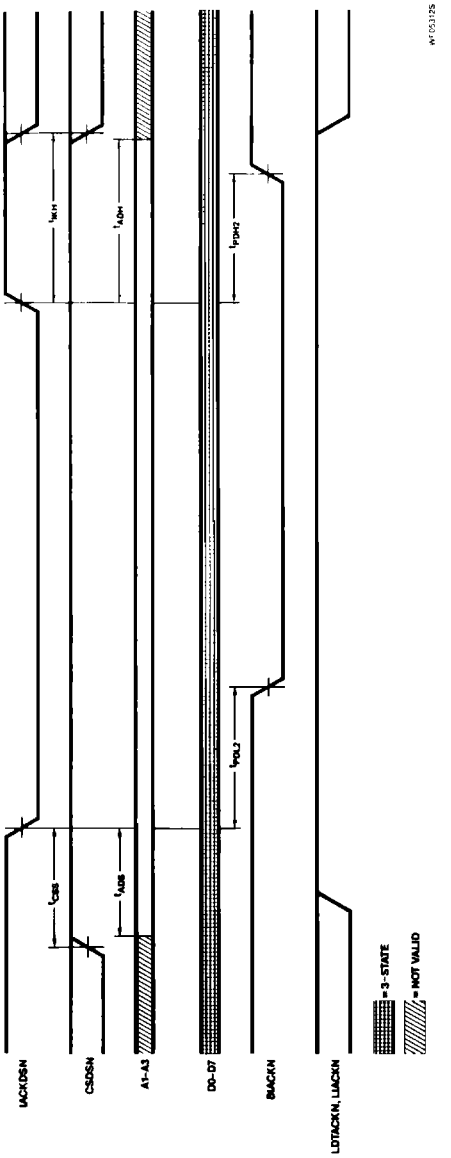


Figure 7. Bus Interrupt Acknowledge[5]

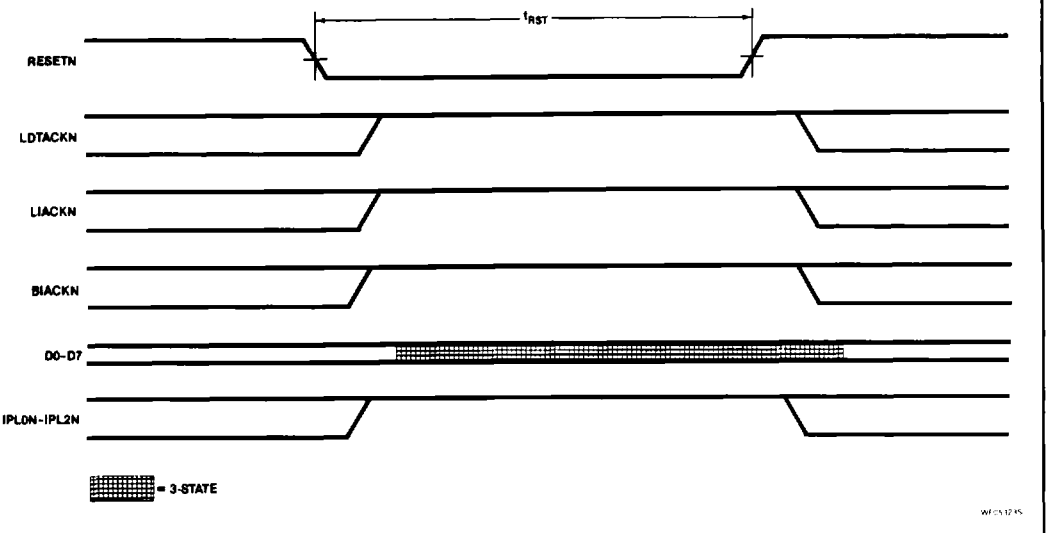


Figure 8. Reset[5]

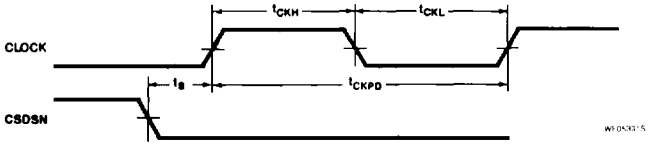


Figure 9. Clock[5]