



SANYO Semiconductors

DATA SHEET**LA6567H**

Monolithic Linear IC

For MD and CD Player

Five-Channel Motor Driver**(four BTL channels plus one H bridge channel)****Overview**

The LA6567H is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6567H features a separate power supply for the H bridge block, an output adjustment pin, and a 5V regulator to support a wide range of applications.

Functions

- Power amplifier 4-channel (BTL) and 1-channel (H bridge) built-in.
- I_O max 700mA (Each channel)
- Level shift circuit built-in (BTL AMP).
- Overheat protection circuit (thermal shutdown) built-in.
- With loading output voltage setting function
- 5V regulator built-in.

Specifications**Maximum Ratings** at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Allowable power dissipation	P_d max	Mounted on a specified board*	2.0	W
Maximum output current	I_O max	Each output for channel 1 to 5.	0.7	A
Maximum input voltage	V_{INB}		13	V
MUTE pin voltage	VMUTE		13	V
Operating temperature	T_{opr}		-30 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

* Mounted on a specified board : 76.1×114.3×1.6mm³, glass epoxy board.**Recommended Operating Conditions** at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

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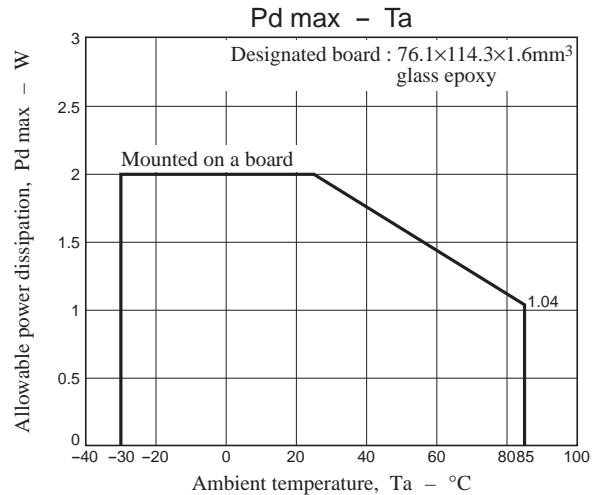
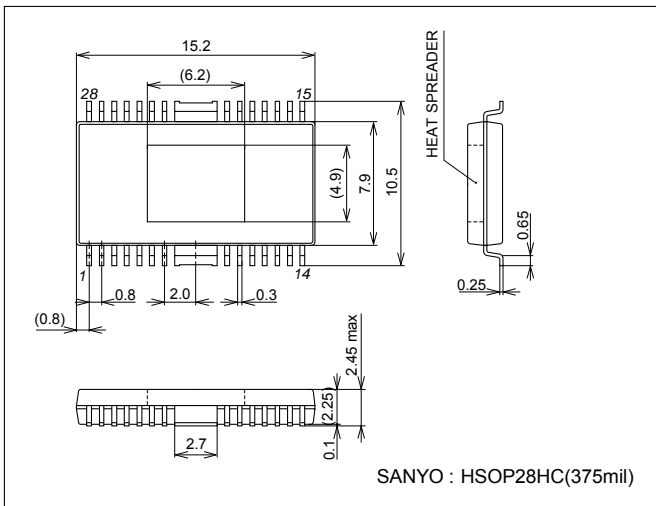
Electrical Characteristics at Ta = 25°C, VCC1 = VCC2 = 8V, VREF = 1.65V, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall Characteristics]						
No-load current drain ON	I _{CC}	All outputs ON, FWD = REV = 0V *1		30	50	mA
VREF input voltage range	VREF-IN		1		V _{CC} -1	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	Voltage difference between outputs for BTL AMP, each channel.	-50		50	mV
Input voltage range	V _{IN}	Input voltage range	0		V _{CC}	V
Output voltage	V _O	Each voltage between V _{O+} and V _{O-} when R _L = 8Ω. *2	4	5		V
Closed-circuit voltage gain	VG	Input and output gain.	3.7	4	4.3	deg
Slew rate	SR	AMP Independent Multiply 2 between outputs. *3		0.5		V/μs
[H Bridge Block]						
Output voltage	V _O -LOAD	VCONT = 8V *2	5.45	6		V
Input low level	V _{IN} -L				1	V
Input high level	V _{IN} -H		2			V
Output setting voltage	VCONT	VCONT = 8V *2	3.0	3.5	4.0	V
[Regulator Block] (PNP transistor : 2SB632K-use)						
Output voltage	Vreg	I _L = 100mA	4.75	5	5.25	V
Output load fluctuation	ΔVRL	I _L = 0 to 200mA	-50	0	10	mV
Supply voltage fluctuation	ΔVV _{CC}	V _{CC} = 6 to 12V, I _L = 100mA	-15	21	60	mV

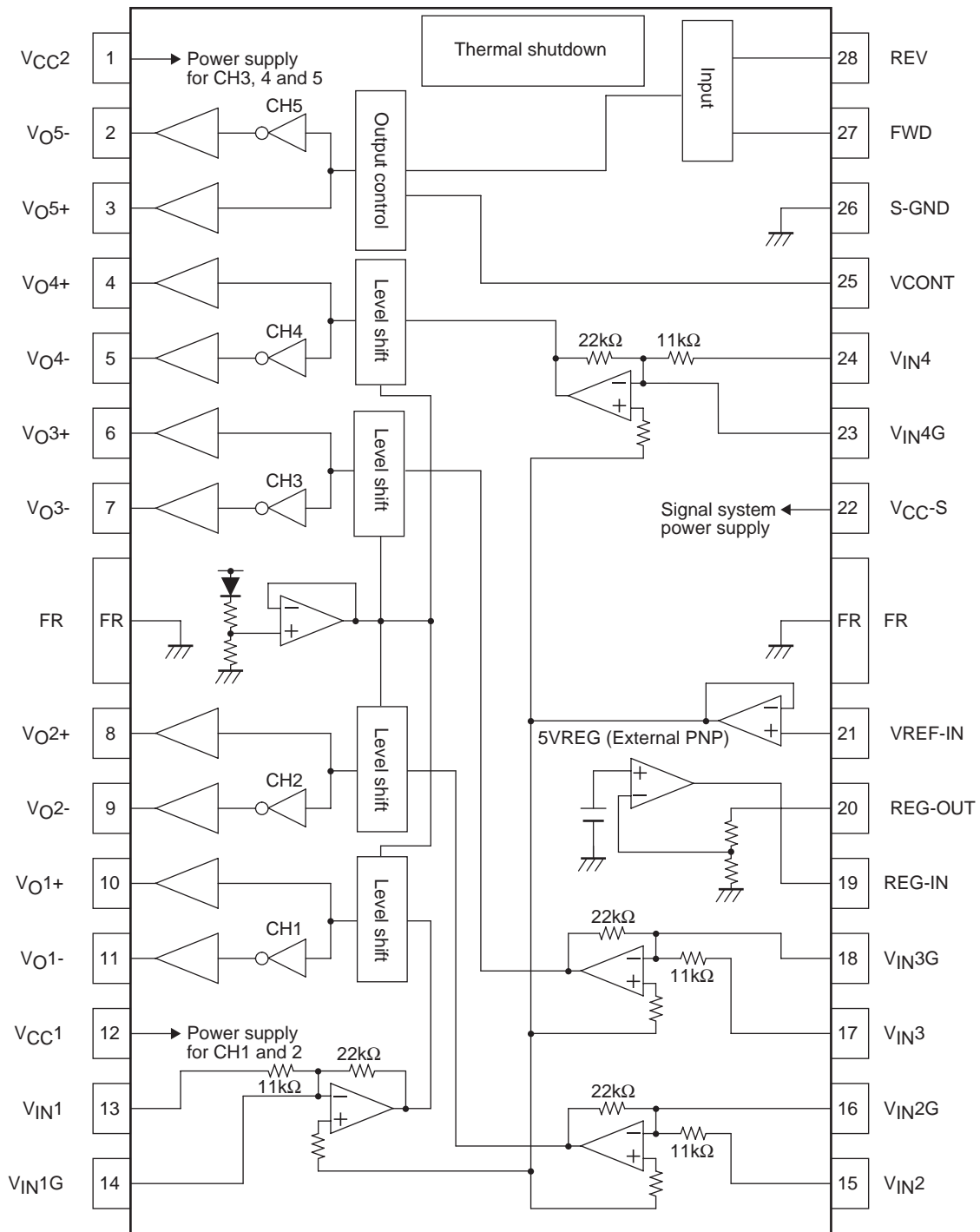
Note *1 : Current dissipation that is a sum of V_{CC}1 and V_{CC}2 at no load.
 *2 : Voltage difference between both ends of load (8Ω). Output saturated.
 *3 : Design guarantee value

Package Dimensions

unit : mm (typ)
 3234B



Block Diagram



Pin Functions

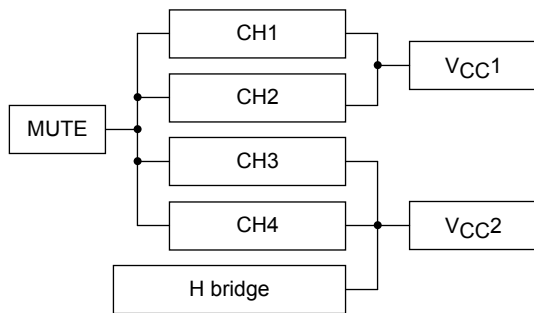
Pin No.	Symbol	Pin descriptions
1	V _{CC2}	CH3, 4, and 5 power supplies (Used while being short-circuited to V _{CC1} and V _{CC-S})
2	V _{O5-}	Loading output (-)
3	V _{O5+}	Loading output (+)
4	V _{O4+}	Output pin (+) for channel 4
5	V _{O4-}	Output pin (-) for channel 4
6	V _{O3+}	Output pin (+) for channel 3
7	V _{O3-}	Output pin (-) for channel 3
8	V _{O2+}	Output pin (+) for channel 2
9	V _{O2-}	Output pin (-) for channel 2
10	V _{O1+}	Output pin (+) for channel 1
11	V _{O1-}	Output pin (-) for channel 1
12	V _{CC1}	CH1 and 2(BTL) power supplies (Used while being short-circuited to V _{CC-S} and V _{CC2})
13	V _{IN1}	Input pin for channel 1
14	V _{IN1G}	Input pin for channel 1 (for gain adjustment)
15	V _{IN2}	Input pin for channel
16	V _{IN2G}	Input pin for channel 2 (for gain adjustment)
17	V _{IN3}	Input pin for channel 3
18	V _{IN3G}	Input pin for channel 3 (for gain adjustment)
19	REG-IN	Regulator pin (external PNP base)
20	REG-OUT	Regulator pin (external PNP collector)
21	VREF-IN	Reference voltage input pin
22	V _{CC-S}	Signal system supply (Used while being short-circuited to V _{CC1} and V _{CC2})
23	V _{IN4G}	Input pin for channel 4 (for gain adjustment)
24	V _{IN4}	Input pin for channel 4
25	VCONT	5CH (VLO) output voltage setting pin
26	S-GND	Signal system GND
27	FWD	5CH(VLO) Output change pin (FWD), logic input for loading block.
28	REV	5CH(VLO) Output change pin (REV), logic input for loading block.

Note : • Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

- Short-circuit power system pins, V_{CC-S}, V_{CC1}, and V_{CC2} externally for use.

Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
13 14 15 16 17 18 23 24	V_{IN} V_{ING}	Input	Each input pin	
4 5 6 7 8 9 10 11	V_O	Output	Each output	
2 3 25	V_{O5+} V_{O5-} VCONT	V_{O5} Output set for loading block	H bridge output Output setting voltage pin	
27 28	FWD	FWD	H bridge input	

Relation of MUTE and Power (V_{CC}*)

* Connect V_{CC1} and V_{CC2} externally.

H bridge block

FWD	REV	V _{O5+}	V _{O5-}	Mode
L	L	OFF	OFF	Open *1
L	H	H	L	Forward
H	L	L	H	Reversed
H	H	L	L	Break *2

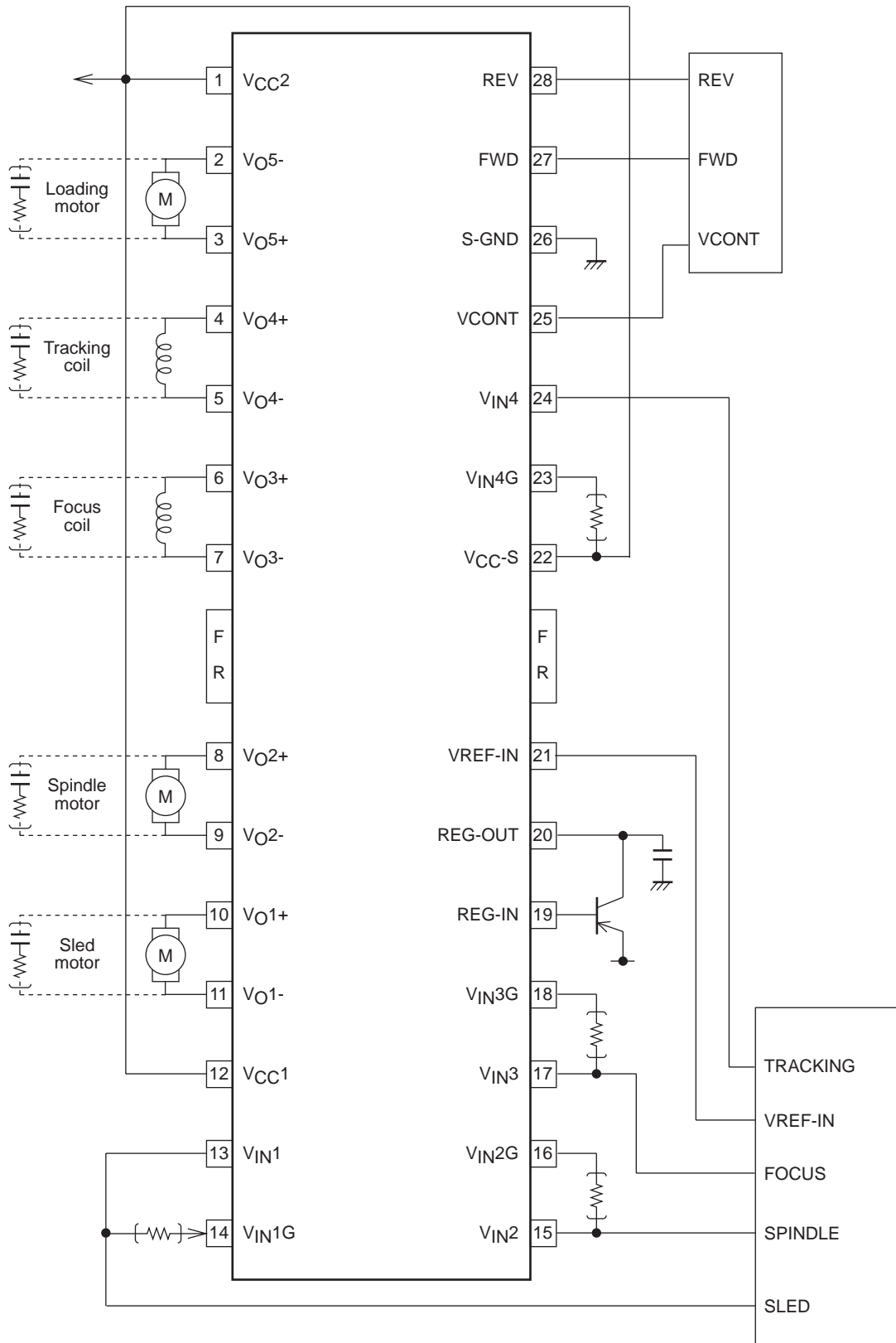
Note *1 : The output has a high Impedance.

*2 : At brake, the SINK side transistor is ON (short brake).

V_{LO+} and V_{LO-} are approximately on the GND level.

*3 : V_{CONT} (output setting voltage pin) and V_{LO} can be related as V_{LO} = V_{CONT}-1V (typ).

Sample Application Circuit



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