## Description

The VM13218165B and VM23218165B are 1M × 32-bit and 2M × 32-bit dynamic RAM modules. It is mounted by 2/4 pieces of 1M × 16 DRAM (VG2618165BB), and each in a standard 42 pin plastic SOJ packages. The VM13218165B and VM23218165B makes high density possible without utilizing the surface mount technology on the printed circuit board. Decoupling capacitors are mounted adjacent to each DRAM for noise reduction.

## Features

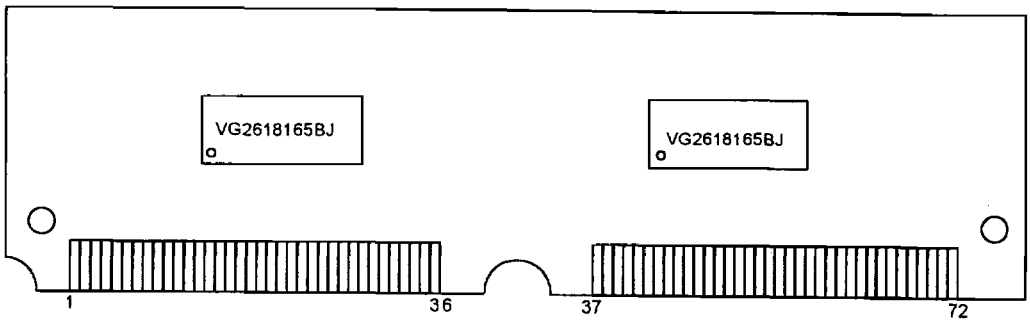
**VM13218165B:**

- 1,048,576 word by 32 bits organization
- Single 5V (±10%) power supply
- High speed $t_{RAC}$ access time : 60/70ns(max)
- Low power dissipation
  - Active mode : 1.98/1.87 W(Max)
  - Standby mode : 11mW(Max)
- Extended-data-out (EDO) page mode capability
- TTL compatible I/O levels
- 1024 refresh cycles during a 16 ms period
- Multiple refresh modes capability
  $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh
- 72 pin single in-line memory module
- JEDEC Standard pinout

**VM23218165B:**

- 2,097,152 word by 32 bits organization
- Single 5V (±10%) power supply
- High speed $t_{RAC}$ access time : 60/70ns(max)
- Low power dissipation
  - Active mode : 2.0/1.89 W(Max)
  - Standby mode : 22mW(Max)
- Extended-data-out (EDO) page mode capability
- TTL compatible I/O levels
- 1024 refresh cycles during a 16 ms period
- Multiple refresh modes capability
  $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh
- 72 pin single in-line memory module
- JEDEC Standard pinout

**Pin assignment (Front View)**




**Pin Out**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 13 | A1 | 25 | DQ23 | 37 | NC | 49 | DQ9 | 61 | DQ14 |
| 2 | DQ1 | 14 | A2 | 26 | DQ8 | 38 | NC | 50 | DQ25 | 62 | DQ31 |
| 3 | DQ17 | 15 | A3 | 27 | DQ24 | 39 | $V_{SS}$ | 51 | DQ10 | 63 | DQ15 |
| 4 | DQ2 | 16 | A4 | 28 | A7 | 40 | $\overline{CAS0}$ | 52 | DQ26 | 64 | DQ32 |
| 5 | DQ18 | 17 | A5 | 29 | NC | 41 | $\overline{CAS2}$ | 53 | DQ11 | 65 | DQ16 |
| 6 | DQ3 | 18 | A6 | 30 | $V_{CC}$ | 42 | $\overline{CAS3}$ | 54 | DQ27 | 66 | NC |
| 7 | DQ19 | 19 | NC | 31 | A8 | 43 | $\overline{CAS1}$ | 55 | DQ12 | 67 | PD1 |
| 8 | DQ4 | 20 | DQ5 | 32 | A9 | 44 | $\overline{RAS0}$ | 56 | DQ28 | 68 | PD2 |
| 9 | DQ20 | 21 | DQ21 | 33 | NC/*$\overline{RAS3}$ | 45 | NC/*$\overline{RAS1}$ | 57 | DQ13 | 69 | PD3 |
| 10 | $V_{CC}$ | 22 | DQ6 | 34 | $\overline{RAS2}$ | 46 | NC | 58 | DQ29 | 70 | PD4 |
| 11 | NC | 23 | DQ22 | 35 | NC | 47 | $\overline{WE}$ | 59 | $V_{CC}$ | 71 | NC |
| 12 | A0 | 24 | DQ7 | 36 | NC | 48 | NC | 60 | DQ30 | 72 | $V_{SS}$ |

* : 2M×32 Version

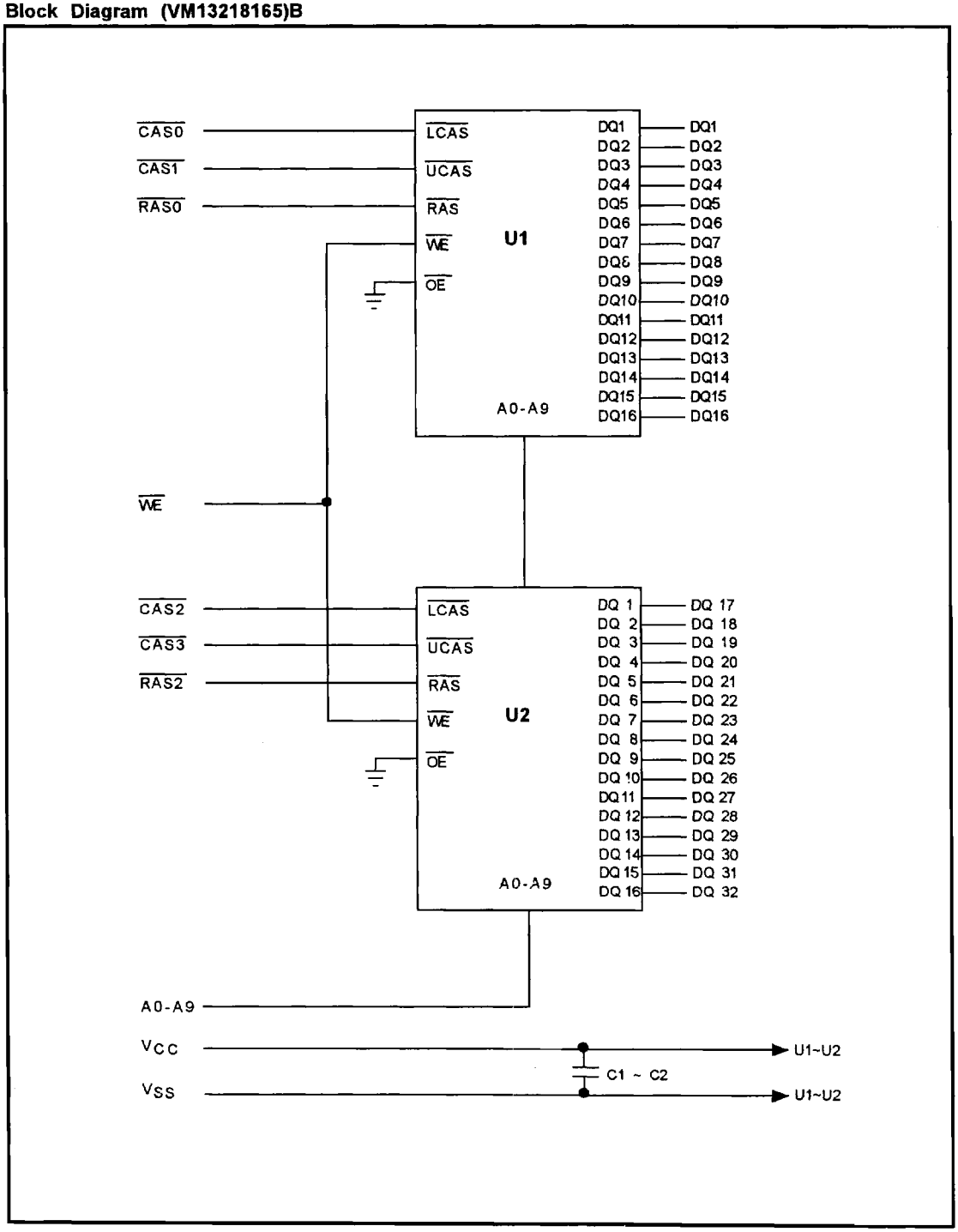
**Presence-detect (1M×32)**

| Name | Pin No | 60ns | 70ns |
|---|---|---|---|
| PD1 | 67 | $V_{SS}$ | $V_{SS}$ |
| PD2 | 68 | $V_{SS}$ | $V_{SS}$ |
| PD3 | 69 | NC | $V_{SS}$ |
| PD4 | 70 | NC | NC |

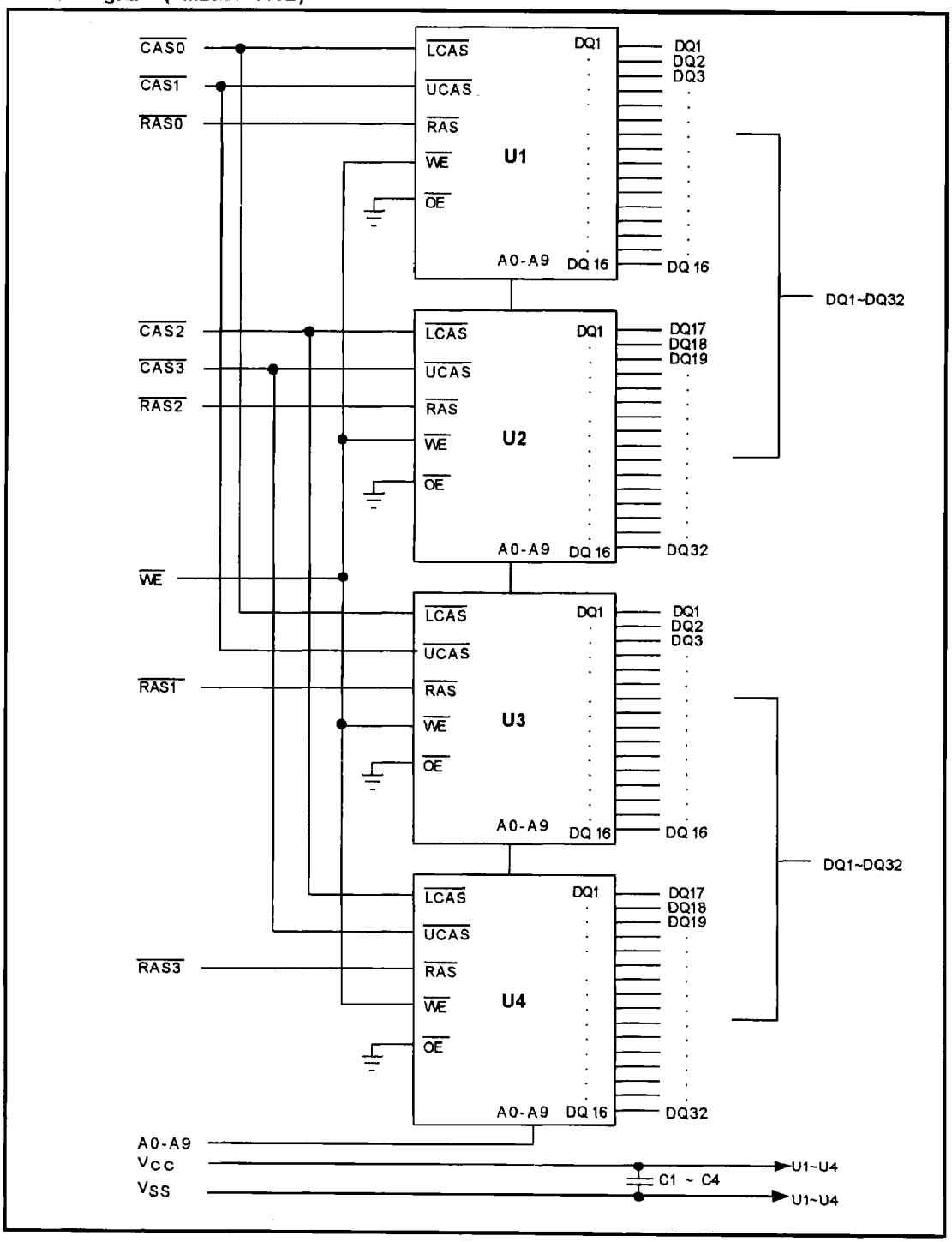
**Presence-detect (2M×32)**

| Name | Pin No | 60ns | 70ns |
|---|---|---|---|
| PD1 | 67 | NC | NC |
| PD2 | 68 | NC | NC |
| PD3 | 69 | NC | $V_{SS}$ |
| PD4 | 70 | NC | NC |

**Block Diagram (VM13218165)B**



**Block Diagram (VM23218165B)**



**Truth Table**

| FUNCTION | | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESSES | | $DQ_S$ |
|---|---|---|---|---|---|---|---|
| | | | | | ROW | COL | |
| STANDBY | | H | H→X | X | X | X | High-Z |
| READ | | L | L | H | ROW | COL | Data-Out |
| WRITE (EARLY WRITE) | | L | L | L | ROW | COL | Data-In |
| EDO PAGE | 1st Cycle | L | H→L | H | ROW | COL | Data-Out |
| MODE READ | 2nd Cycle | L | H→L | H | n/a | COL | Data-Out |
| EDO PAGE | 1st Cycle | L | H→L | L | ROW | COL | Data-In |
| MODE WRITE | 2nd Cycle | L | H→L | L | n/a | COL | Data-In |
| HIDDEN | READ | L→H→L | L | H | ROW | COL | Data-Out |
| REFRESH | WRITE | L→H→L | L | L | ROW | COL | Data-In |
| $\overline{RAS}$ ONLY REFRESH | | L | H | X | ROW | n/a | High-Z |
| CBR REFRESH | | H→L | L | X | X | X | High-Z |

**Absolute Maximum Ratings**

| Parameter | NAME | Value | | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_T$ | -1.0 to +7.0 | | V |
| Supply voltage relative to Vss | $V_{CC}$ | -1.0 to +7.0 | | V |
| Short circuit output current | $I_{OUT}$ | 50 | | mA |
| Power dissipation | $P_D$ | 1M×32 | 2 | W |
| | | 2M×32 | 4 | |
| Operating temperature | $T_{OPT}$ | 0 to +70 | | ℃ |
| Storage temperature | $T_{STG}$ | -55 to +125 | | ℃ |

**Recommended DC Operating Conditions**

| Parameter/Condition | NAME | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage, all inputs | $V_{IH}$ | 2.4 | – | Vcc+1.0 | V |
| Input Low Voltage, all inputs | $V_{IL}$ | -1.0 | – | 0.8 | V |

**Capacitance**

Ta=25℃,$V_{CC}$=5V±10% , f=1MHZ

| Parameter | | Symbol | Size | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input capacitance(Address) | | $C_{I1}$ | 1M×32 | - | 32 | pF | 1 |
| | | | 2M×32 | - | 42 | | |
| Input capacitance | ($\overline{RAS0}$, $\overline{RAS2}$) | $C_{I2}$ | 1M×32 | - | 21 | pF | 1 |
| | ($\overline{RAS0}$ ~ $\overline{RAS3}$) | | 2M×32 | - | 23 | | |
| Input capacitance ($\overline{CAS0}$ ~ $\overline{CAS3}$) | | $C_{I3}$ | 1M×32 | - | 20 | pF | |
| | | | 2M×32 | - | 27 | | |
| Input Capacitance ($\overline{WE}$) | | $C_{I4}$ | 1M×32 | - | 32 | pF | |
| | | | 2M×32 | - | 46 | | |
| Output capacitance (Data-in,Data-out) | | $C_{I/O}$ | 1M×32 | - | 17 | pF | 1,2 |
| | | | 2M×32 | - | 24 | | |

Note : 1. Capacitance measured with effective capacitance measuring method.

2. $\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$ to disable Dout.

**DC Characteristics ;**
(Ta=0 to 70℃, $V_{CC}$=+5V±10%, $V_{SS}$=0V)

| Parameter | Symbol | Test Conditions | size | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | | |
| Operating current | $I_{CC1}$ | $\overline{RAS}$ cycling<br>$\overline{CAS}$ cycling<br>$t_{RC}$=min. | 1M×32<br>2M×32 | -<br>- | 360<br>364 | -<br>- | 340<br>344 | mA | 1,2 |
| Standby Current | $I_{CC2}$ | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$=$V_{IH}$<br>Dout=High-Z | 1M×32<br>2M×32 | -<br>- | 4<br>8 | -<br>- | 4<br>8 | mA | |
| | | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≧Vcc-0.2V<br>Dout=High-Z | 1M×32<br>2M×32 | -<br>- | 2<br>4 | -<br>- | 2<br>4 | mA | |
| $\overline{RAS}$-only refresh current | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CAS}$=$V_{IH}$<br>$t_{RC}$=min. | 1M×32<br>2M×32 | -<br>- | 360<br>364 | -<br>- | 340<br>344 | mA | 1,2 |
| EDO page mode current | $I_{CC4}$ | $t_{PC}$=min. | 1M×32<br>2M×32 | - | 220<br>224 | - | 200<br>204 | mA | 1,3 |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC5}$ | $t_{RC}$=min.<br>$\overline{RAS}$, $\overline{CAS}$ cycling | 1M×32<br>2M×32 | -<br>- | 360<br>364 | -<br>- | 340<br>344 | mA | 1,2 |
| Input leakage current | $I_{LI}$ | 0V≦Vin≦7V | 1M×32<br>2M×32 | -10<br>-20 | 10<br>20 | -10<br>-20 | 10<br>20 | μA | |
| Output leakage current | $I_{LO}$ | 0V≦Vout≦7V<br>Dout=Disable | 1M×32<br>2M×32 | -10<br>-20 | 10<br>20 | -10<br>-20 | 10<br>20 | μA | |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-5mA | 1M×32<br>2M×32 | 2.4<br>2.4 | -<br>- | 2.4<br>2.4 | -<br>- | V | |
| Output low voltage | $V_{OL}$ | $I_{OL}$=+4.2mA | 1M×32<br>2M×32 | -<br>- | 0.4<br>0.4 | -<br>- | 0.4<br>0.4 | V | |

**Notes :**

1. $I_{CC}$ is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ =$V_{IL}$.
3. For $I_{CC4}$ , address can be changed once or less within one EDO page mode cycle time.

**AC Characteristics**

(Ta =0 to +70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V)Notes*1,*2,*3

Test conditions

- Input rise and fall times:2ns
- Input timing reference levels :
  $V_{IH}$=2.4V, $V_{IL}$=0.8V

**Read,Write and Refresh Cycles**
**(Common Parameters)**

| Parameter | Symbol | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | $t_{RC}$ | 110 | - | 124 | - | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 40 | - | 50 | - | ns | |
| $\overline{CAS}$ precharge time in normal mode | $t_{CPN}$ | 10 | - | 10 | - | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 60 | 10000 | 70 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 10 | 10000 | 12 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | - | 0 | - | ns | |
| Row address hold time | $t_{RAH}$ | 10 | - | 10 | - | ns | |
| Column address setup time | $t_{ASC}$ | 0 | - | 0 | - | ns | 4 |
| Column address hold time | $t_{CAH}$ | 10 | - | 15 | - | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 42 | 20 | 50 | ns | 5 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns | 6 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | - | 35 | - | ns | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | - | 18 | - | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 50 | - | 60 | - | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | - | 5 | - | ns | 7 |
| Transition time (rise and fall) | $t_T$ | 1 | 50 | 1 | 50 | ns | 8 |
| Refresh period | $t_{REF}$ | - | 16 | - | 16 | ms | |
| $\overline{CAS}$ to output in Low-Z | $t_{CLZ}$ | 0 | - | 0 | - | ns | |
| $\overline{OE}$ to Din delay time | tOED | 15 | | 18 | | ns | |

**Read Cycle**

| Parameter | Symbol | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | - | 60 | - | 70 | ns | 9 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | - | 18 | - | 20 | ns | 10,11 |
| Access time from column address | $t_{AA}$ | - | 30 | - | 35 | ns | 11,12 |
| Read command setup time | $t_{RCS}$ | 0 | - | 0 | - | ns | 4 |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | - | 0 | - | ns | 7,13 |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 10 | - | 10 | - | ns | 13 |
| Output buffer turn-off time | $t_{OFF}$ | 0 | 15 | 0 | 18 | ns | 14 |
| Access time from $\overline{OE}$ | tOEA | - | 15 | - | 18 | ns | |
| Output buffer turn-off time from $\overline{OE}$ | tOEZ | 0 | 15 | 0 | 18 | ns | 14 |

**Write Cycle**

| Parameter | Symbol | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Write command setup time | $t_{WCS}$ | 0 | - | 0 | - | ns | 4 |
| Write command hold time | $t_{WCH}$ | 10 | - | 10 | - | ns | |
| Write command pulse width | $t_{WP}$ | 10 | - | 10 | - | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 15 | - | 18 | - | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 15 | - | 18 | - | ns | |
| Data-in setup time | $t_{DS}$ | 0 | - | 0 | - | ns | |
| Data-in hold time | $t_{DH}$ | 10 | - | 15 | - | ns | |
| $\overline{WE}$ to Data-in delay | $t_{WED}$ | 10 | - | 10 | - | ns | |

**Refresh Cycle**

| Parameter | Symbol | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $\overline{CAS}$ setup time(CBR refresh ) | $t_{CSR}$ | 10 | - | 10 | - | ns | |
| $\overline{CAS}$ hold time (CBR refresh ) | $t_{CHR}$ | 10 | - | 10 | - | ns | 7 |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | - | 5 | - | ns | 4 |

**EDO Page Mode Cycle**

| Parameter | Symbol | -6 | | -7 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| EDO page mode cycle time | $t_{PC}$ | 25 | - | 30 | - | ns | |
| EDO page mode $\overline{CAS}$ precharge time | $t_{CP}$ | 10 | - | 10 | - | ns | |
| EDO page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | 60 | $10^5$ | 70 | $10^5$ | ns | 15 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | - | 35 | - | 40 | ns | 7,11 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 35 | - | 40 | - | ns | |
| $\overline{OE}$ high hold time from $\overline{CAS}$ high | $t_{OEHC}$ | 5 | - | 5 | - | ns | |
| $\overline{OE}$ high pulse width | $t_{OEP}$ | 10 | - | 10 | - | ns | |
| Data Output hold after $\overline{CAS}$ low | $t_{COH}$ | 5 | - | 5 | - | ns | |
| Out disable delay from $\overline{WE}$ | $t_{WHZ}$ | 3 | 10 | 3 | 10 | ns | |
| $\overline{WE}$ pulse width for output disable when $\overline{CAS}$ high | $t_{WPZ}$ | 7 | - | 7 | - | ns | |

Notes :

1.AC measurements assume $t_T$=2ns.

2.An initial pause of 100 $\mu$s is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

3.All the $V_{CC}$ and $V_{SS}$ pins shall be supplied with the same voltages.

4.$t_{ASC}$(min) ‧ $t_{RCS}$ (min) ‧ $t_{WCS}$(min) and $t_{RPC}$ are determined by the falling edge of $\overline{CAS}$ .

5.Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$(max) can be met, $t_{RCD}$(max) is specified as a reference point only,if $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.

6.Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$(max) can be met, $t_{RAD}$(max) is specified as a reference point only,if $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit, then access time is controlled exclusively by $t_{AA}$.

7.$t_{CRP}$, $t_{CHR}$, $t_{RCH}$ and $t_{CPA}$ are determined by the rising edge of $\overline{CAS}$ .

8.$V_{IH}$(min) and $V_{IL}$ (max) are reference levels for measuring timing or input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.

9.Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table,$t_{RAC}$ exceeds the value shown.

10.Assumes that $t_{RCD} \geqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max).

11.Access time is determined by the longer of $t_{AA}$, $t_{CAC}$, $t_{CPA}$.

12.Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \geqq t_{RAD}$(max).

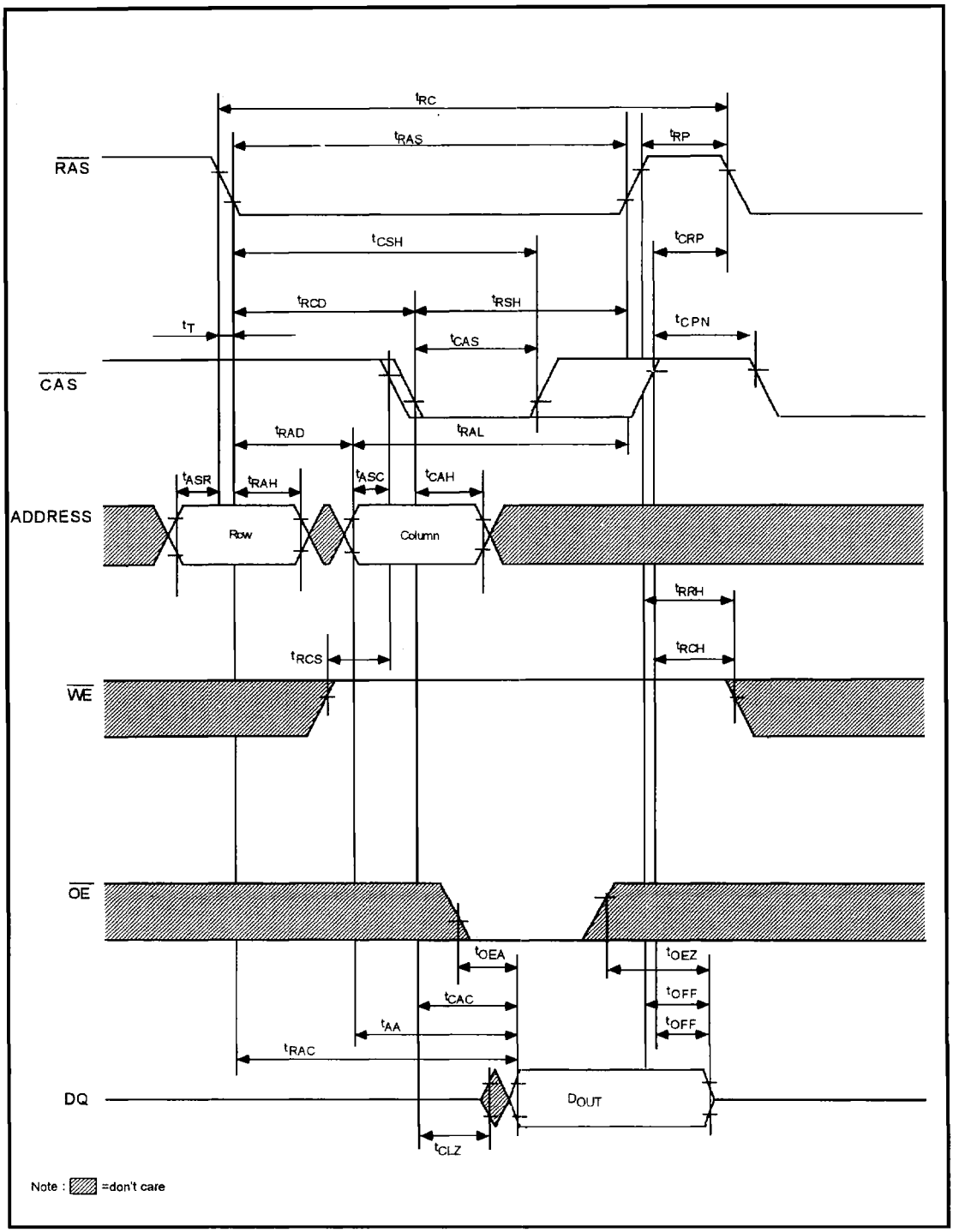
13.Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

14.$t_{OFF}$(max) and $t_{OEZ}$(max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. $t_{OFF}$ is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

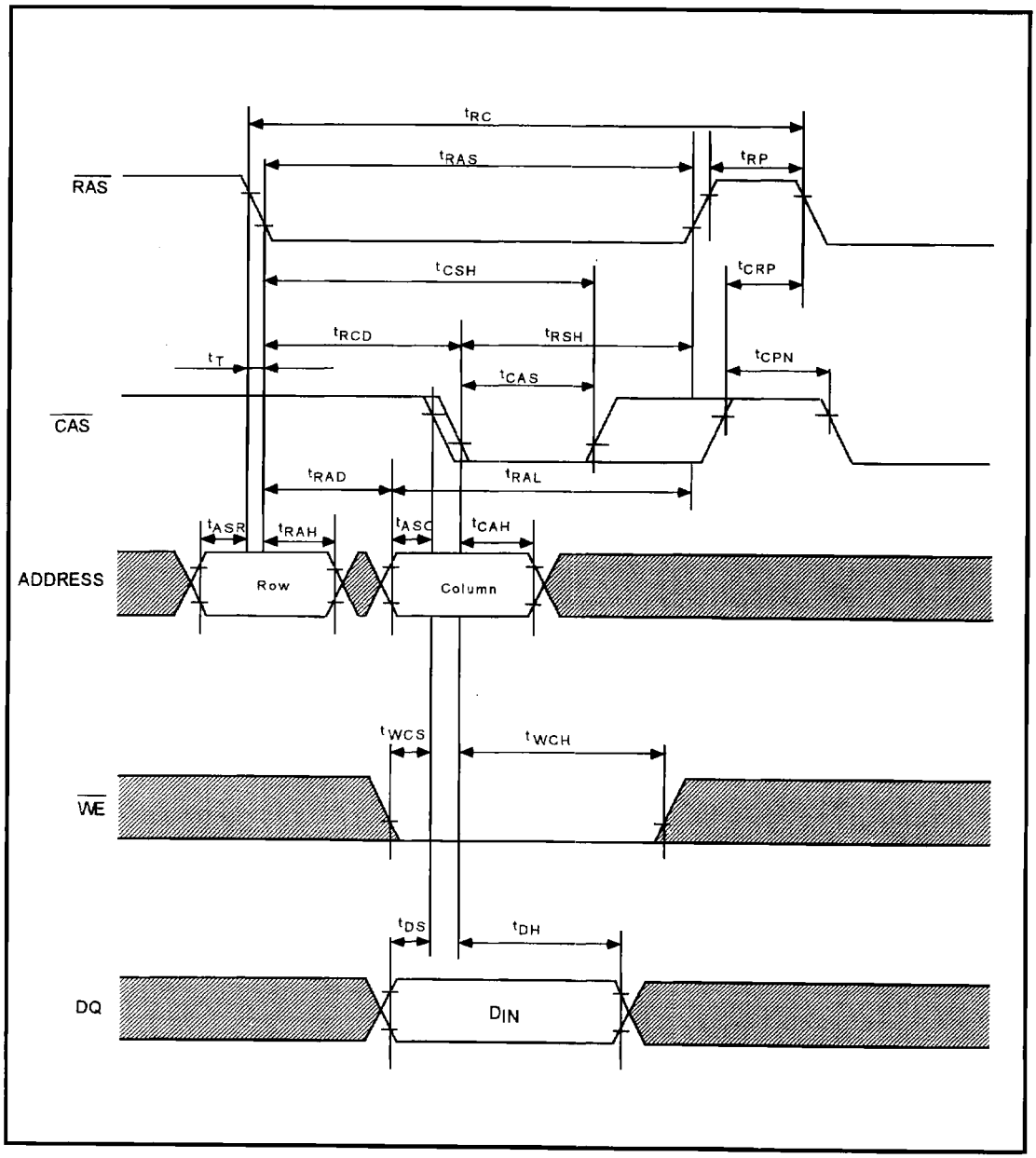
15.$t_{RASP}$ defines $\overline{RAS}$ pulse width in EDO page mode cycles.

## Timing Waveforms

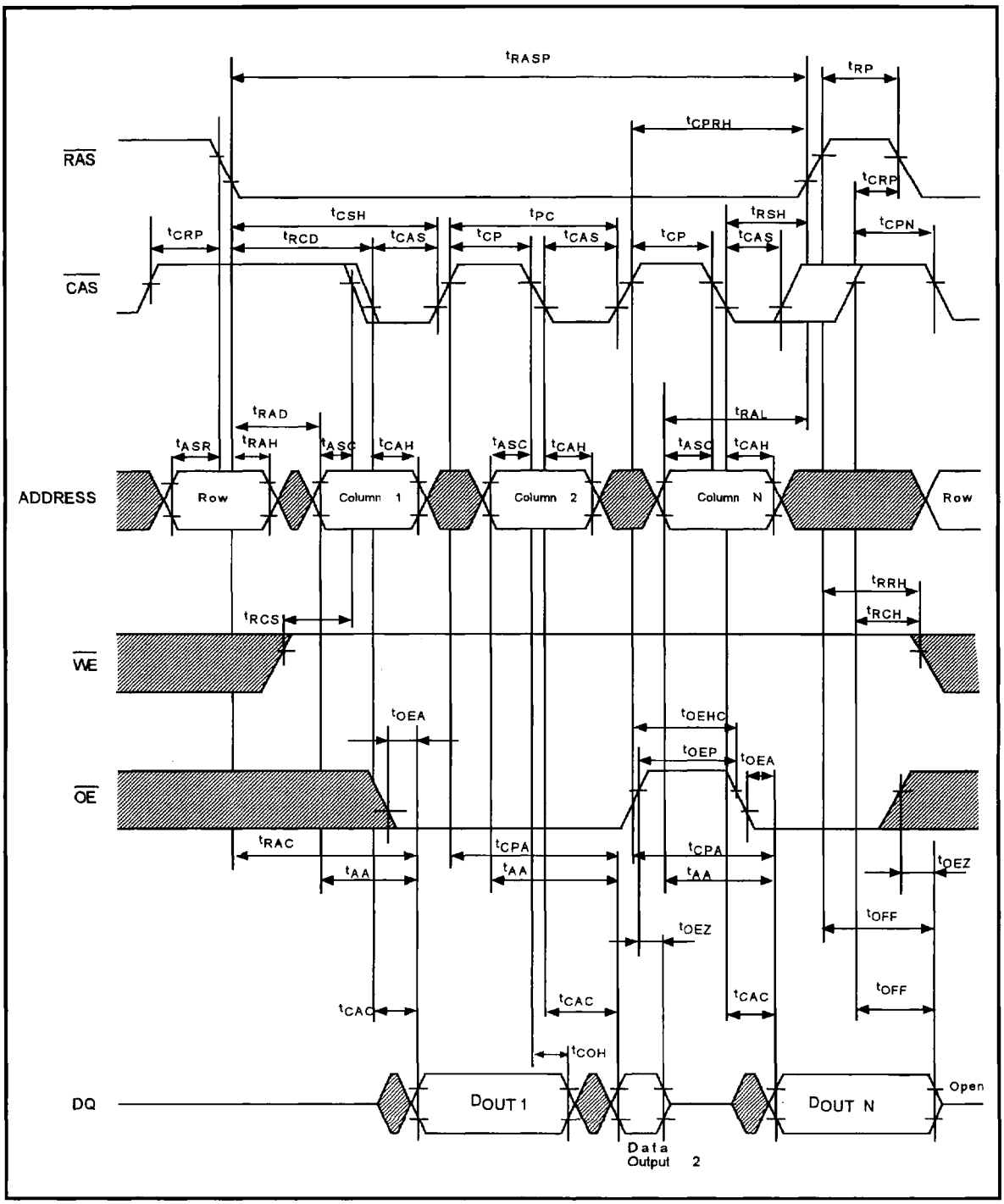
### • Read Cycle



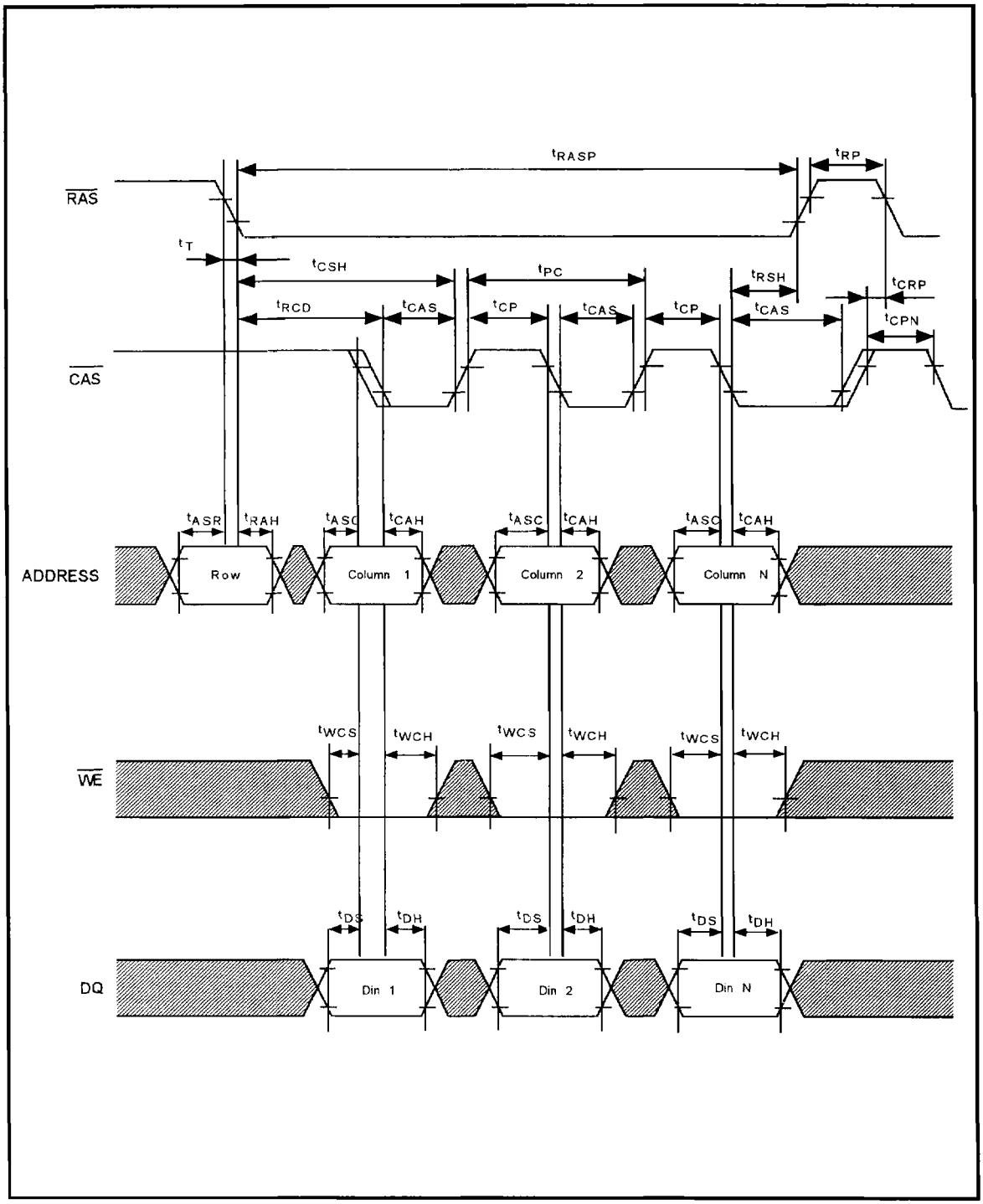
· **Early Write Cycle**



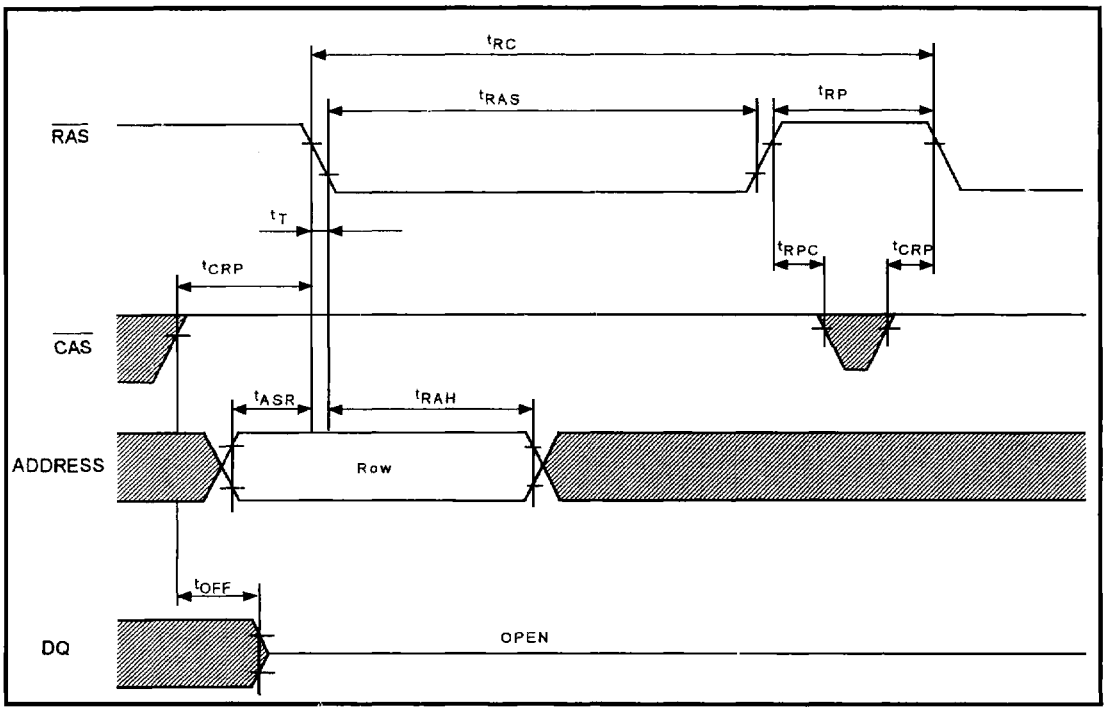
## • EDO Page Mode Read Cycle



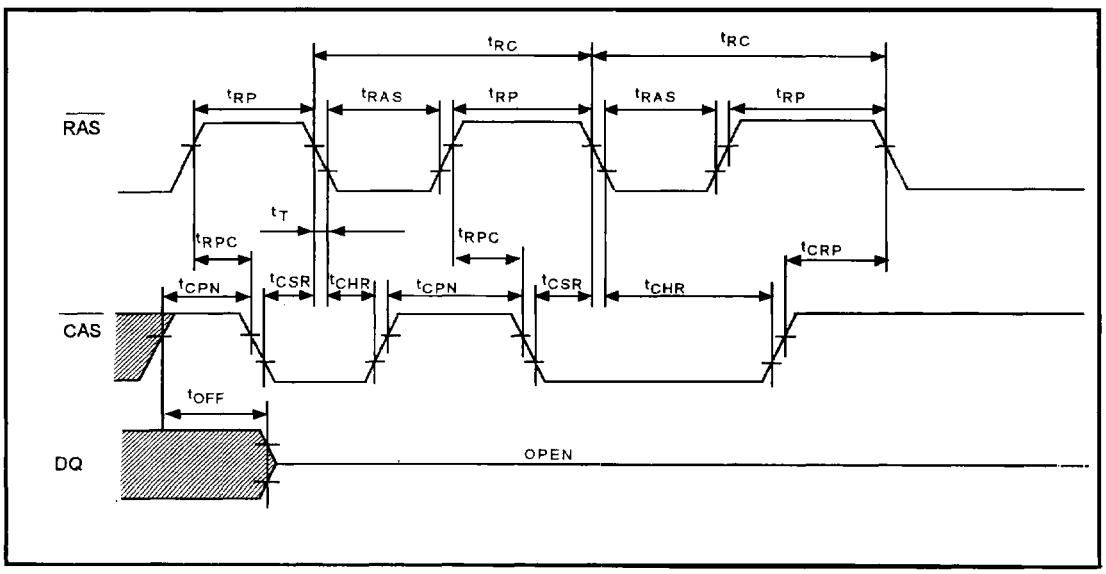
## · EDO Page Mode Early Write Cycle



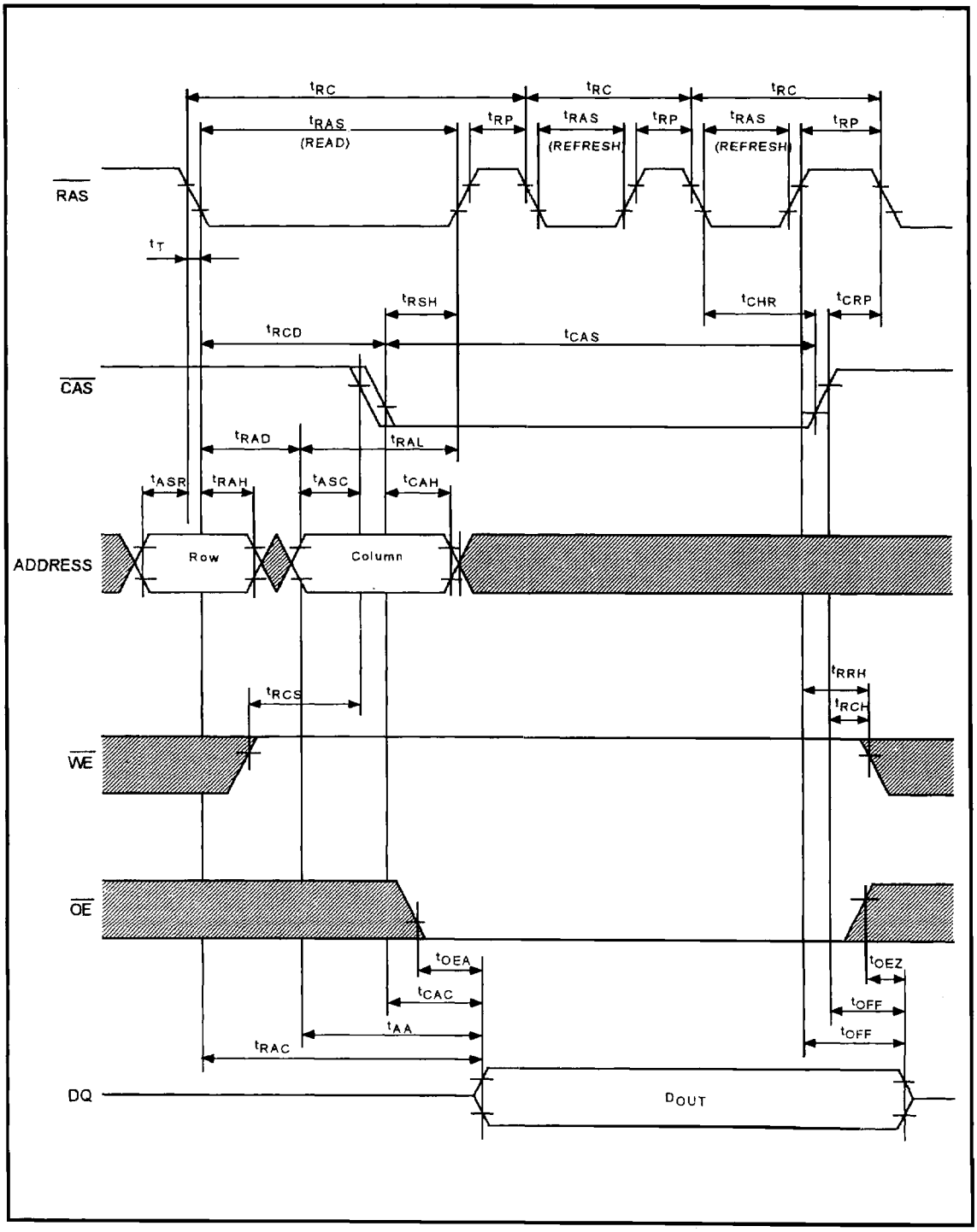
• **$\overline{RAS}$-Only Refresh Cycle**




• **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



## • Hidden Refresh Cycle



**Ordering Information**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| V | X | X | XX | XXXXX | X | X | X | X | X | -X |

V : VIS Product

1 : RAM Family
- M : DRAM SIMM (72pin)
- D : DRAM DIMM(168 pin)

2 : Memory density (word)
- 1 : 1M
- 2 : 2M
- 4 : 4M
- 8 : 8M

3 : I/O width
- 32 : x32
- 64 : x64

4 : Operating mode and refresh with different density
- 17800 : Fast page, 2K ref.,2MX8 DRAM
- 17805 : EDO, 2K ref. 2MX8 DRAM
- 18160 : Pass Page, 1K ref. 1MX16 DRAM
- 18165B : EDO, 1K ref. 1MX16 DRAM

5 : Component revision
- Blank : None
- A : A revision
- B : B revision

6: Component Package
- J : SOJ
- T : TSOP

7 : PC board finger plating
- G : Gold
- S : Tin/lead

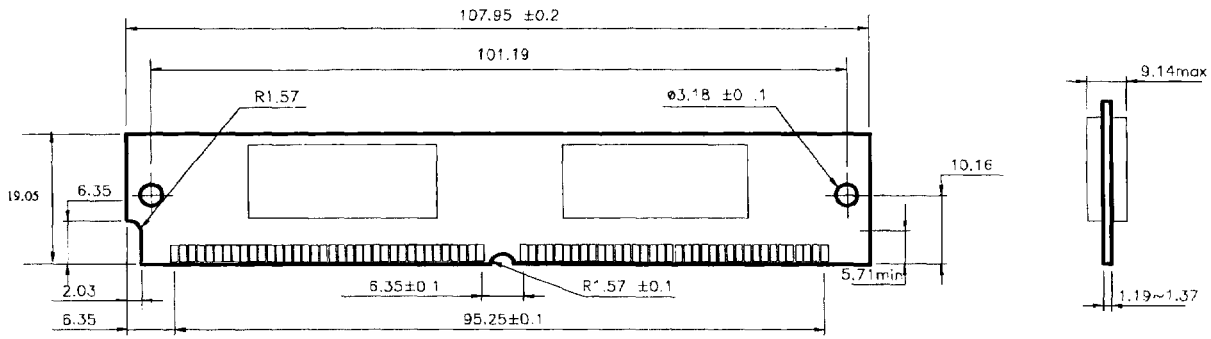
8 : PC board revision
- Blank : none
- A : A revision

9 : Low Power, Customer specific
- Blank : none
- L : Low Power

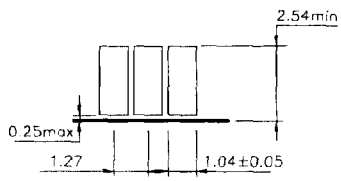
10 : Speed
- -6 : 60 ns
- -7 : 70ns

## Packaging Information

UNITS: mm
Tolerances: ±0.13 Unless otherwise specified




**Golder & Solder Plating Lead**




**NOTE: PCB Model No. M116C**

**The use device is 1Mx16 SOJ DRAM**